

# Design change considerations for input protection of the CBM TOF FEE

Jochen Frühauf

GSI Helmholtzzentrum für Schwerionenforschung GmbH(GSI)

# Outline

- 1<sup>st</sup> PADI damage @ STAR Experiment
- 2<sup>nd</sup> PADI damage @ STAR Experiment
- Simulation
- Outlook

# First PADI damage @ STAR 2019/2020

- no additional ESD protection diodes on FEE
- we lost a substantial amount of PADI channels (50%)
- this was the first time we observed such an issue

# First ESD Protection: ESD113-B1

placed before coupling C

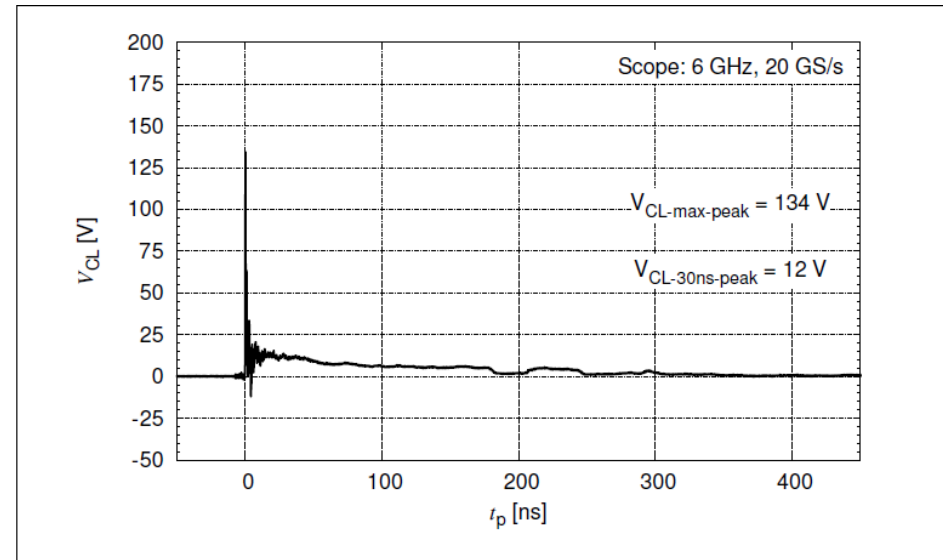
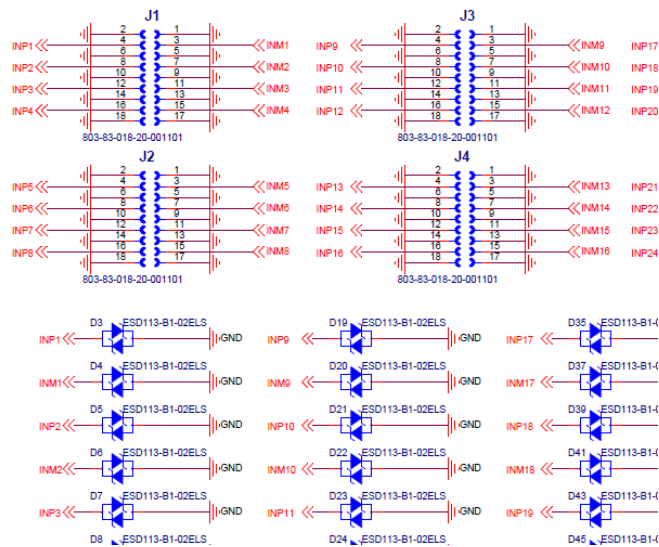


Figure 4-5 Clamping voltage (ESD):  $V_{CL} = f(t)$ , 8 kV positiv pulse from pin 1 to pin 2

# Destructive Test

- pulses with an adjustable output voltage up to 400V and pulse-width between 25ns and 100ns were injected
- analogue and digital output of PADI were checked
  - PADI with ESD protection can handle
    - 400V / 25ns / 10KHz (~800nC)
    - 400V / 100ns / 1Hz (~3,2uC)
    - 400V / 100ns / 10Hz => damaged
  - PADI without ESD protection can handle
    - 40V / 25ns / 1Hz (~80nC)
    - 63V / 25ns / a few pulses => damaged (126nC)
- since only 50% of the FEE channels were damaged, we assumed the injected charge was just on the threshold level
- we **suspected** our new protection scheme is sufficient

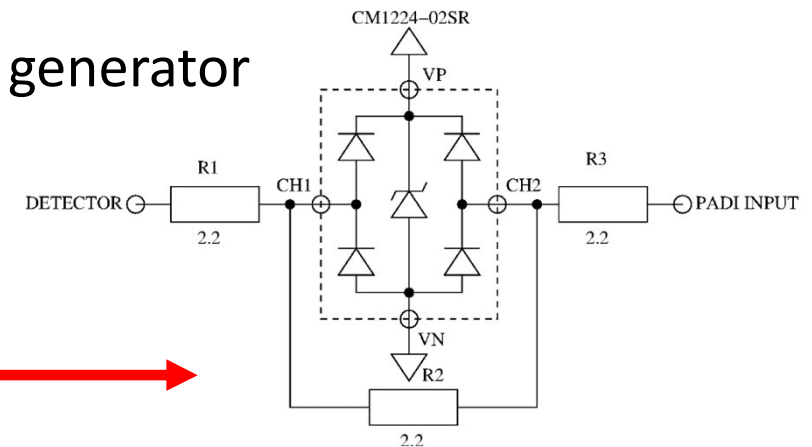
# Second PADI damage @ STAR 2020/2021

- with the new protection no complete losses of PADI channels were observed
- an unexplained loss of efficiency was detected during the data inspection
- the result of further investigation:
  - positive side of PADI has a low impedance to GND
  - high threshold value is applied due to leakage current inside the ASIC
  - **ESD protection was presumably not sufficient enough**

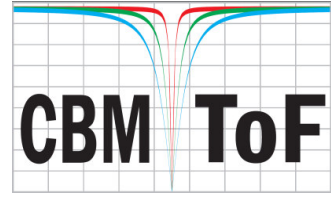
# Simulation

- for the internal ESD Protection Diodes of PADI a maximum current of **+/-1.26A** was evaluated.
- we (Dr. Mircea Ciobanu) simulated the input current for different type of input protection schema:
  - no protection / PADI + ESD113 / PADI + CM1224
- in simulation the FEE is connected to a 8kV-IEC generator

protection	I @ PADI Input
PADI	+/- 26A
PADI + ESD113	+/- 1.3A
PADI + CM1224	+2mA /-0.5mA



- simulation indicates that with the current solution (PADI + CM1224) no more improvement is needed



# CM1224 is approved by other groups

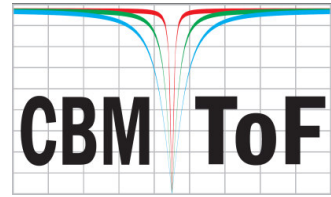
- literature search has revealed that the same protection mechanism was selected for
  - the NINO FEE @ STAR (MRPC)
  - the SAMPA FEE @ ALICE (TPC)



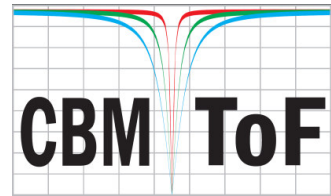
# New PCBs available soon

- PCBs with new protection schema available soon
  - components are already delivered
  - PCB will arrive within the next week
  - equipping planned for December (latest January)
- Test:
  - performance tests @ laboratory Dec 21/ Jan 22
    - destruction test with 400V pulser
    - destruction test with “ESD Pistol”
  - performance tests @ mCBM Feb / Mar 22
- preparation for preproduction of ~20000 Channel launched Nov. 21
  - includes the possibility for STAR upgrade late summer 2022

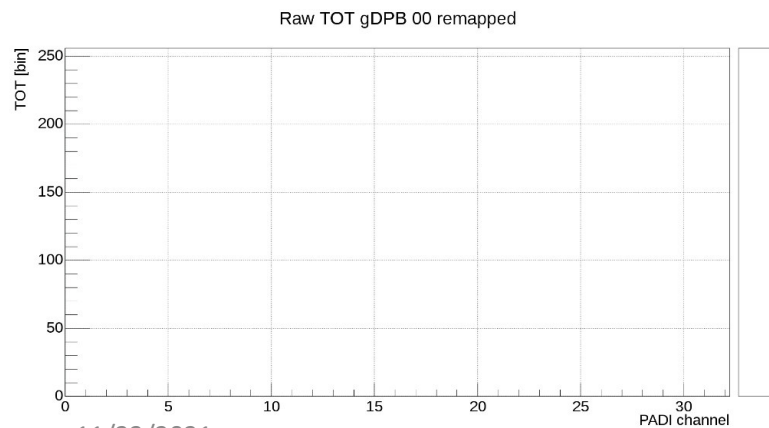
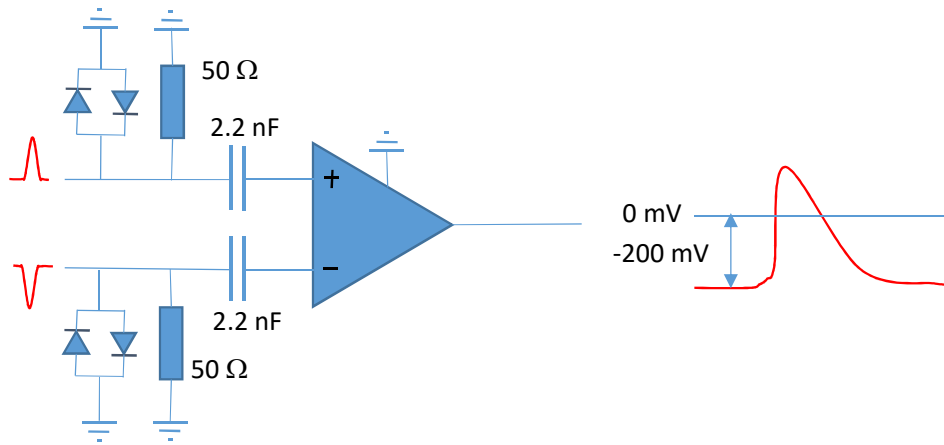
Thank You



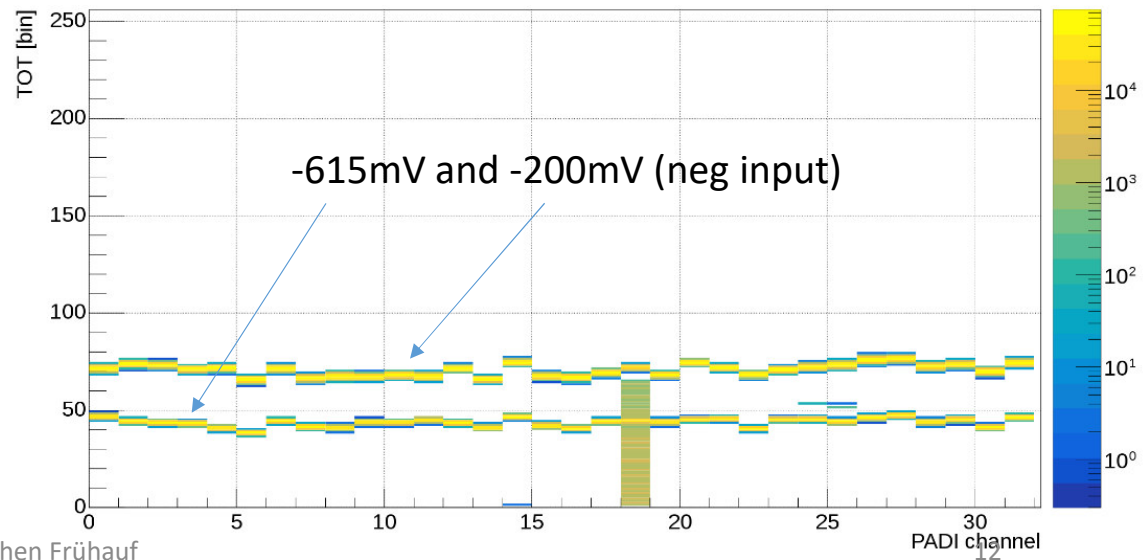
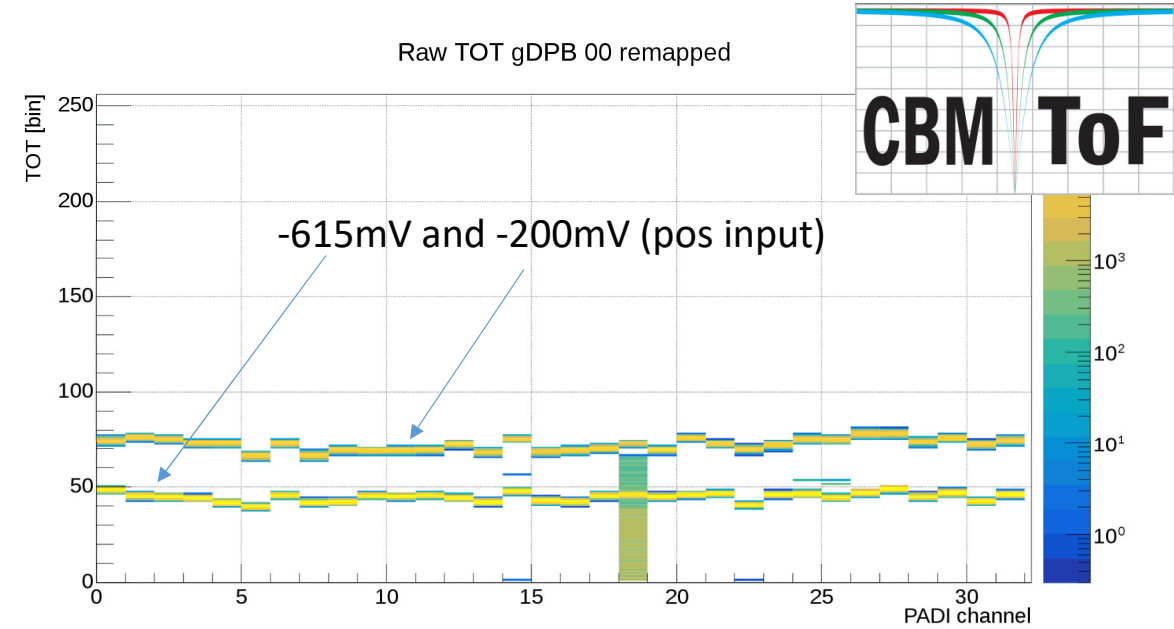
# Backup



# TOT Measurements: Example of a good PCB



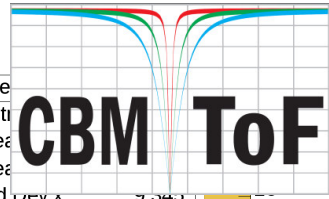
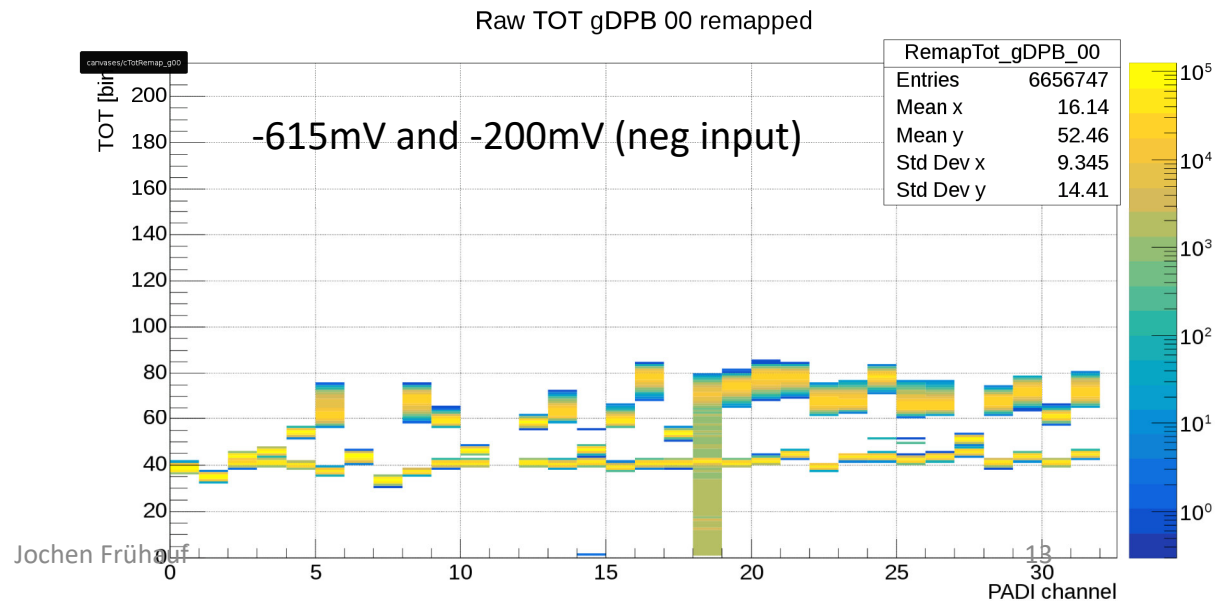
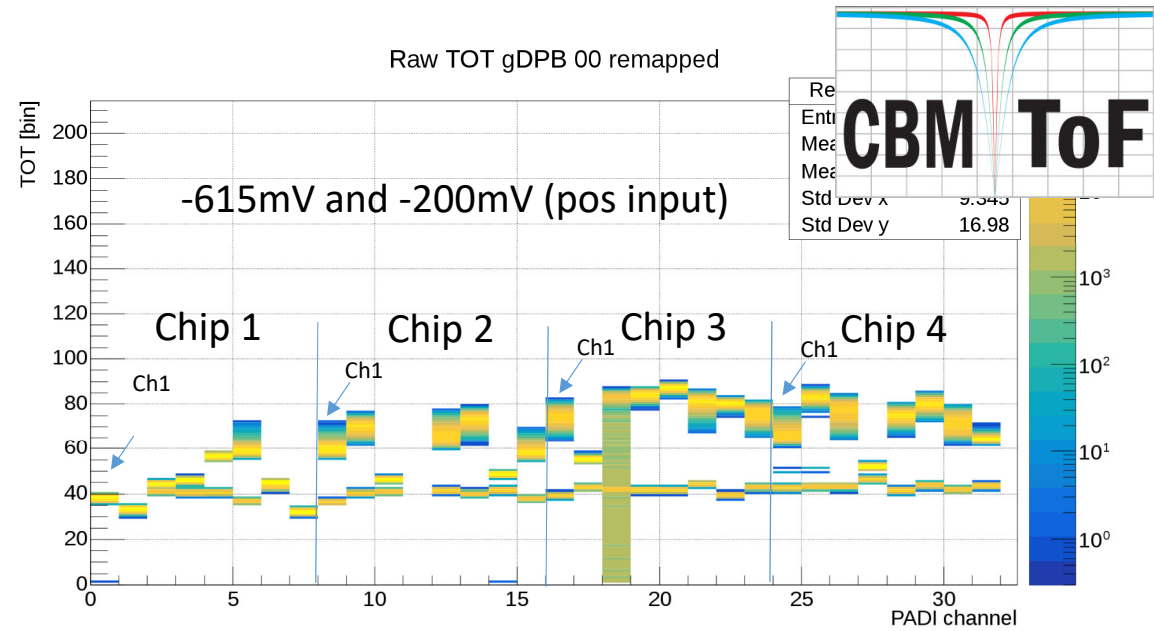
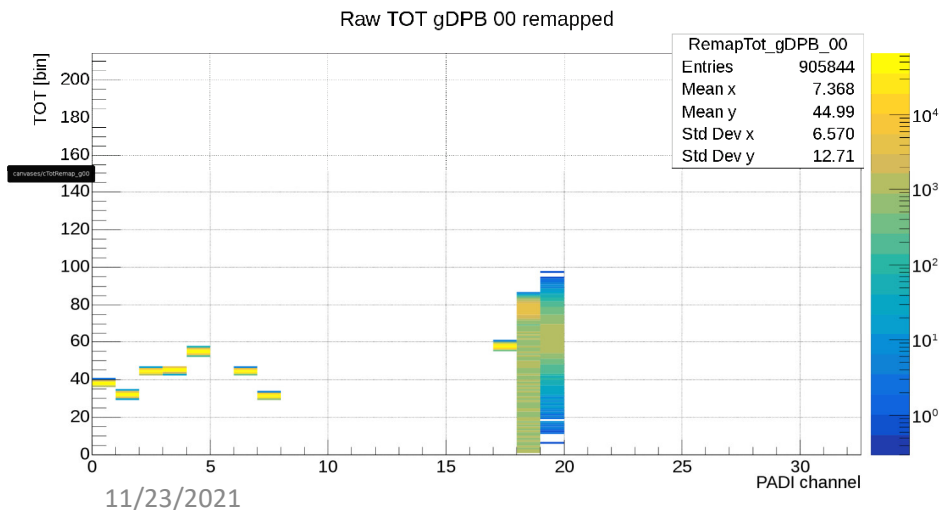
11/23/2021 +615mV (has no entries)



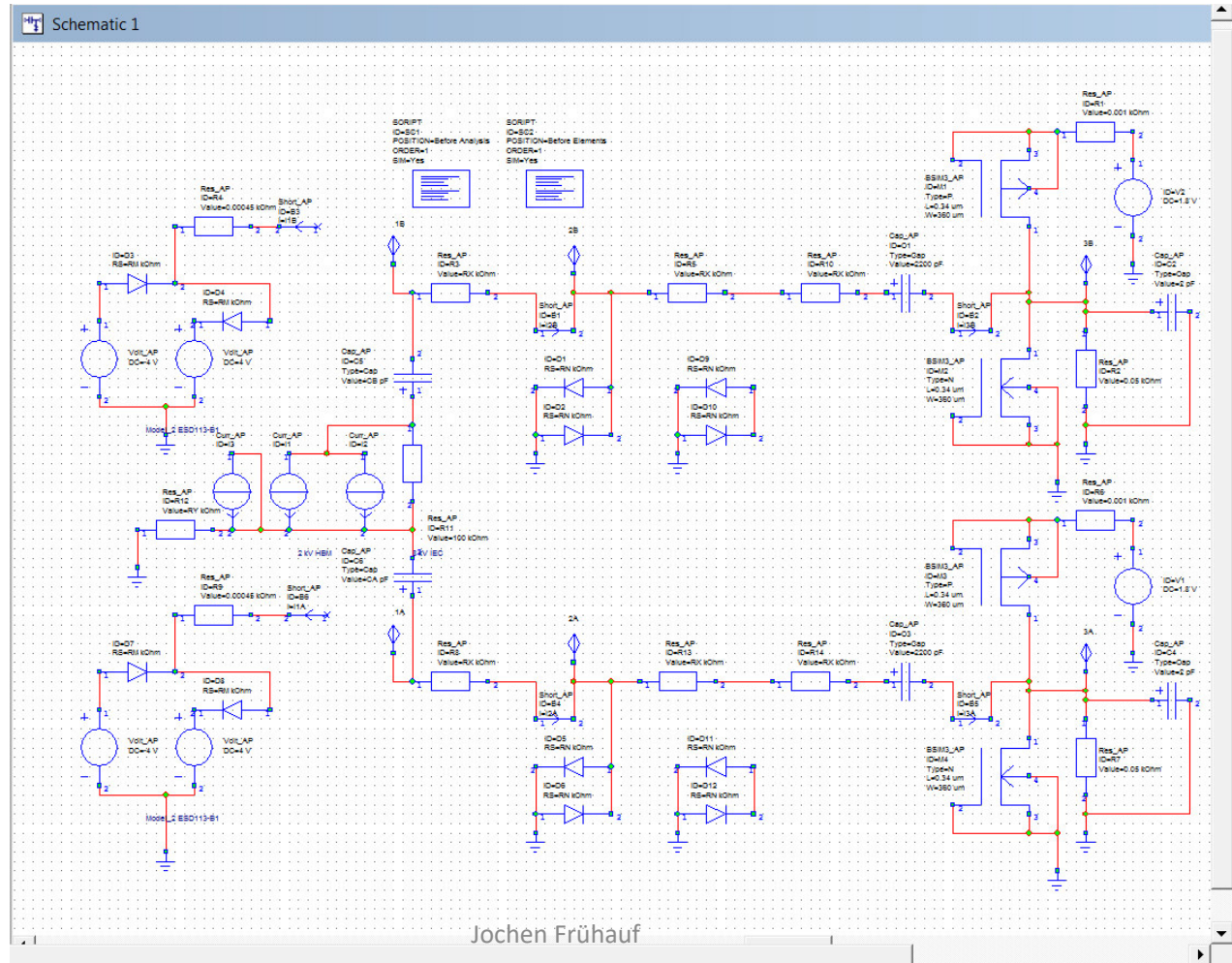
Jochen Frühauf

# TOT Measurements: example of PADI PCB #2 right

+615mV (should have no entries)



# Schematics of Simulation



# Simulation Results

connection	V1A,V1B (V)	I1A, I1B (A)	V3A,V3B (V)	I3A, I3B, (A)
PADI	+/- 400	+/- 26	+35 / -8	+/- 26
PADI+ESD113	+/- 16	+/- 26	+4 /-1	+/- 1.3
PADI+ESD113+CM1124	+/- 16	+/- 26	+/- 0.6	+2m/-0.5m
PADI+CM1224	+/- 300	+/- 26	+/- 0.6	+2m/-0.5m
PADI+CM1224mod.	+/- 300	+/- 26	+/- 0.6	+2m/-8m
PADI+CM1224mod.+ESD113	+/- 16	+/- 26	+/- 0.6	+3m/-4m