Verification of front-end electronics boards for the FT and STT detectors

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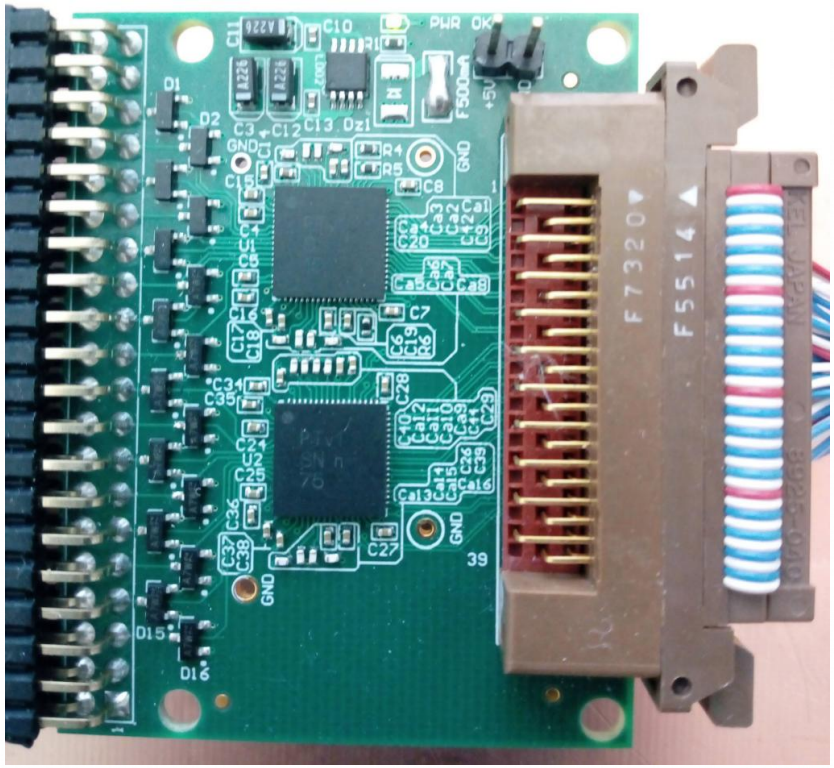
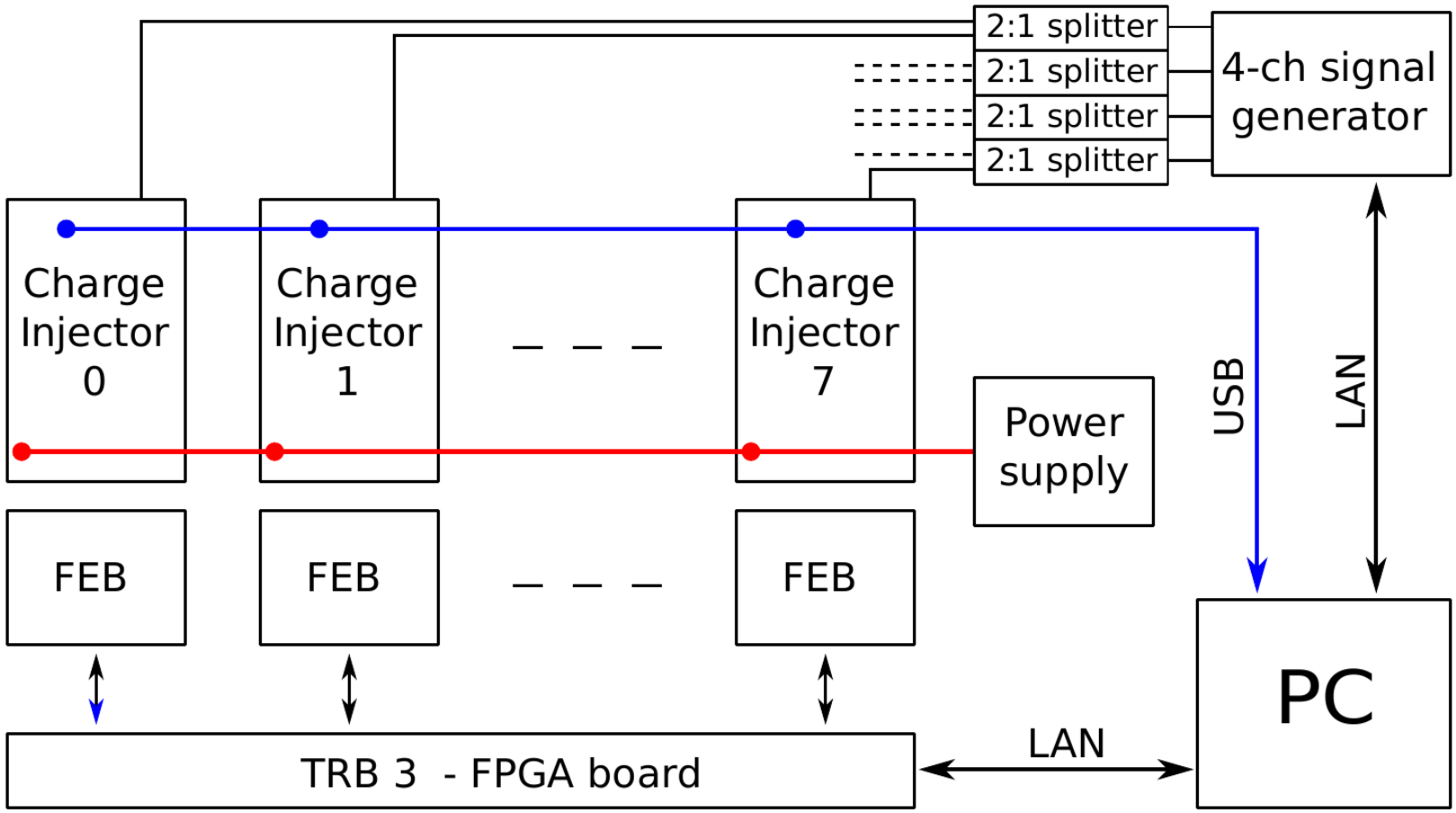
Outline

- Test setup
- Test measurements and procedures
- Measurements reports and status
- Summary and future plans

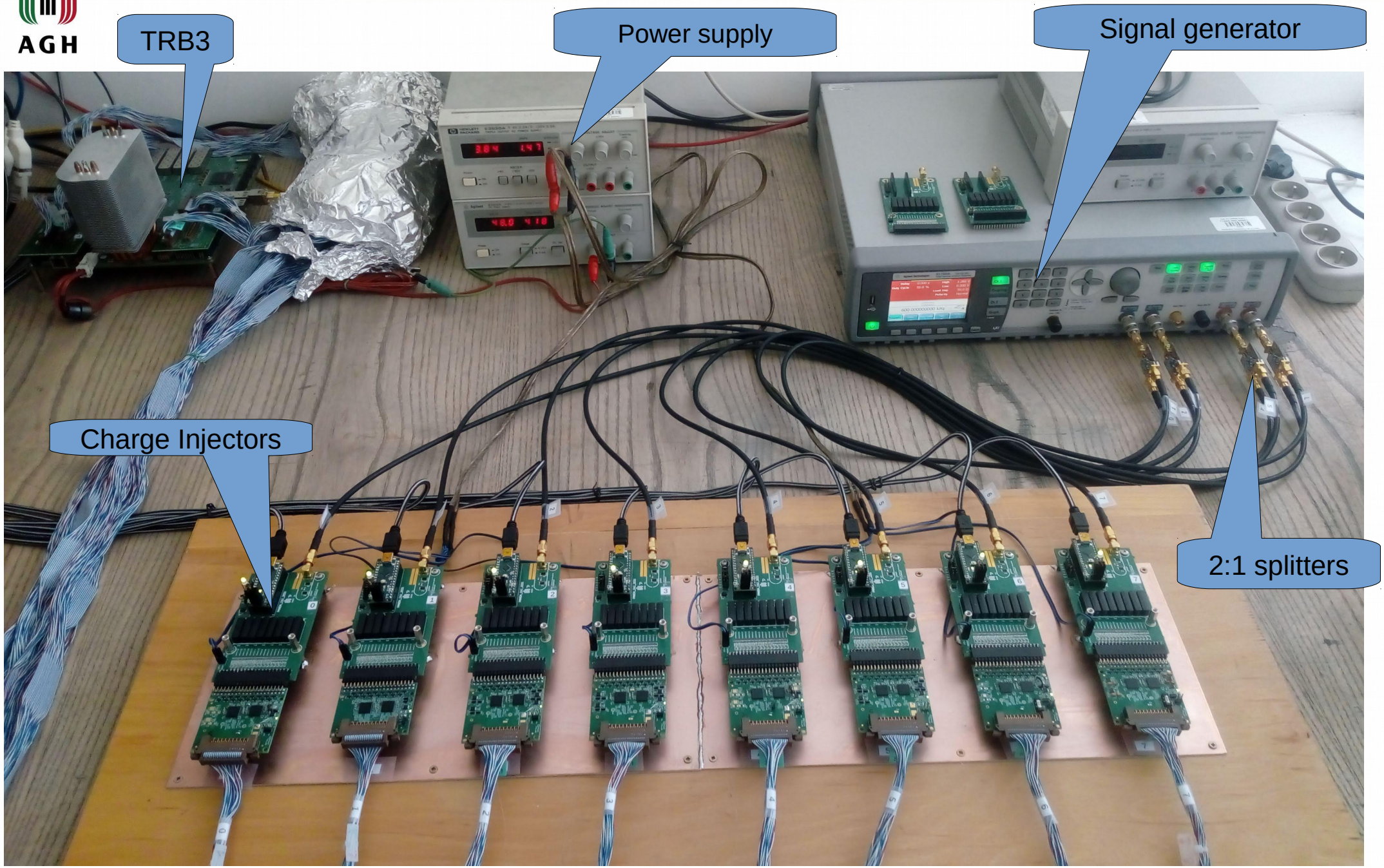


Architecture of the Test System



- 8 FEB boards can be tested in parallel (16 PASTTRECs)
- Test signals during S-curve measurements come from Charge Injector boards
- System controlled by PC via python scripts – fully automatic

Test Measurement Setup



Test Setup Features

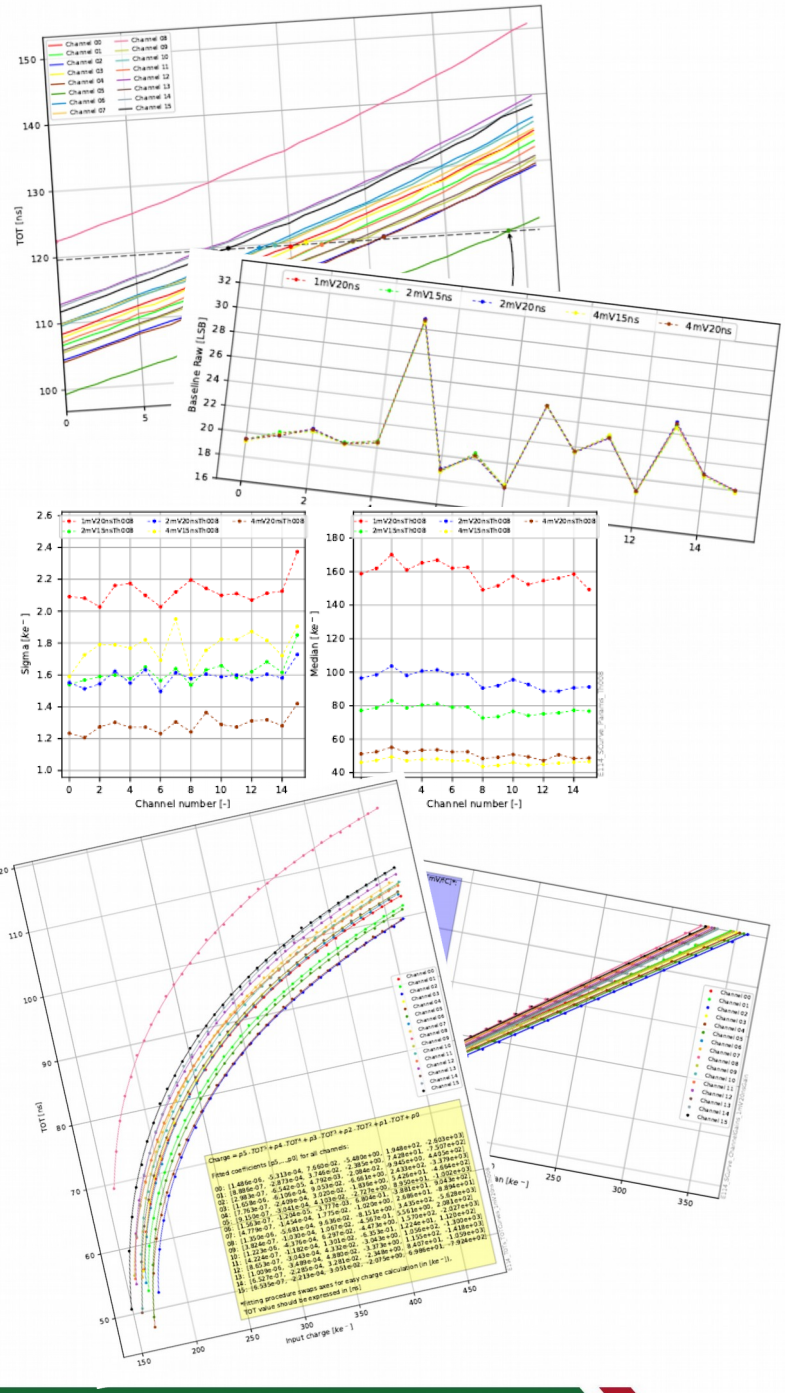
- System measures 8 FEBs (16 PASTTRECs) in parallel
- All FEBs are tested in 5 typical configurations (shown below)
- For each configuration measurements check: DACs quality, baseline of the channels, noise and gains (details on the next slides)
- System automatically fits data and prepares plots (~180 per board)
- Measured data and fitted data are stored in one file (~400kB) using Python's pickle module
- Finally the summary reports with selected plots, tables and additional comments are created

Configuration name	Gain	T_{peak}	TC_{C1}	TC_{R1}	TC_{C2}	TC_{R2}
1mV20ns	1 mV/fC	20 ns	6.0 pF	23 kΩ	0.6 pF	11 kΩ
2mV15ns	2 mV/fC	15 ns	15.0 pF	7 kΩ	0.6 pF	8 kΩ
2mV20ns	2 mV/fC	20 ns	7.5 pF	27 kΩ	0.75 pF	17 kΩ
4mV15ns	4 mV/fC	15 ns	13.5 pF	19 kΩ	1.5 pF	23 kΩ
4mV20ns	4 mV/fC	20 ns	10.5 pF	27 kΩ	0.9 pF	20 kΩ

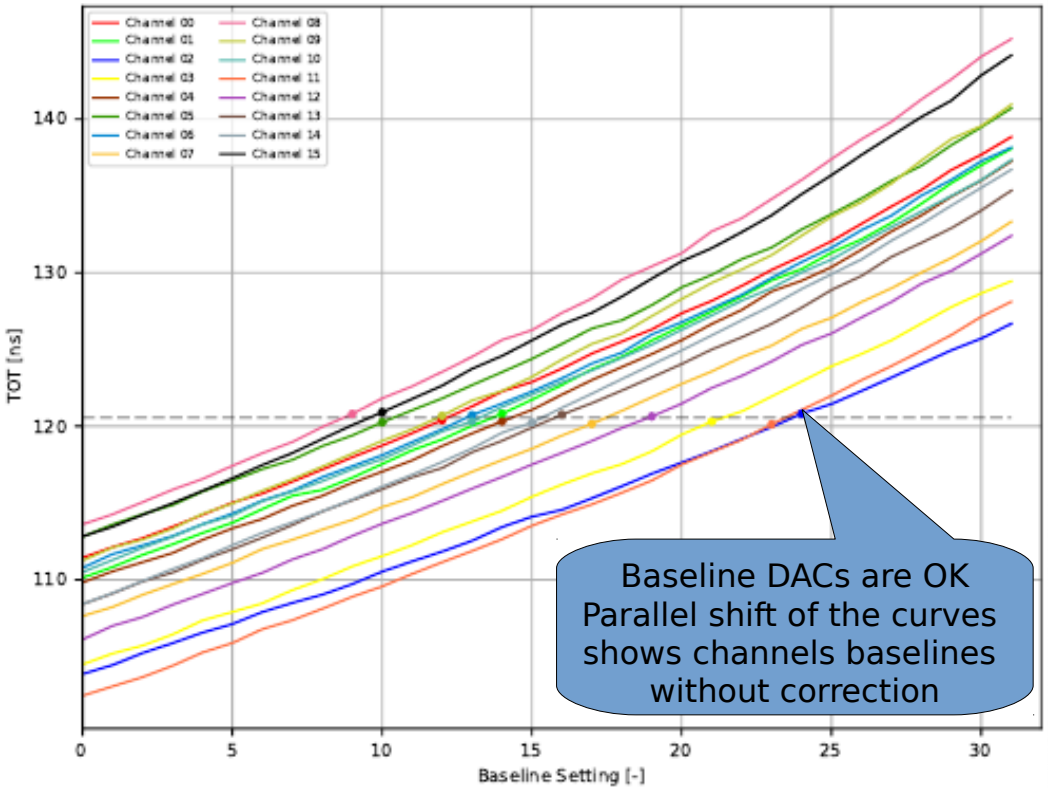
Full test procedure takes around 23h

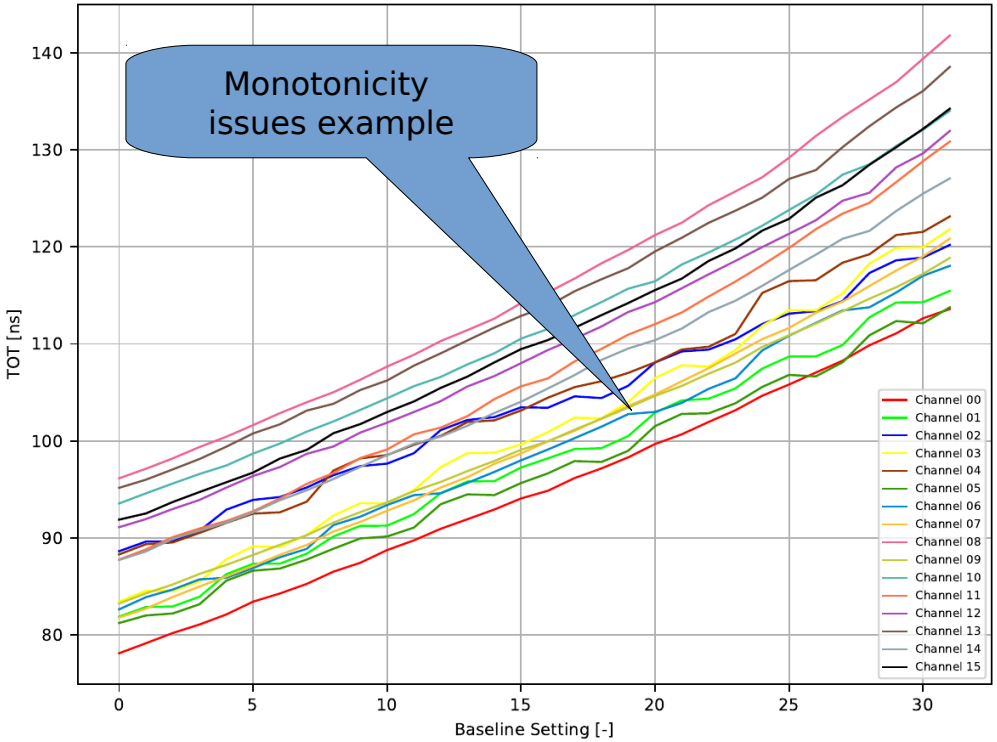
Measurements: Types and Procedures

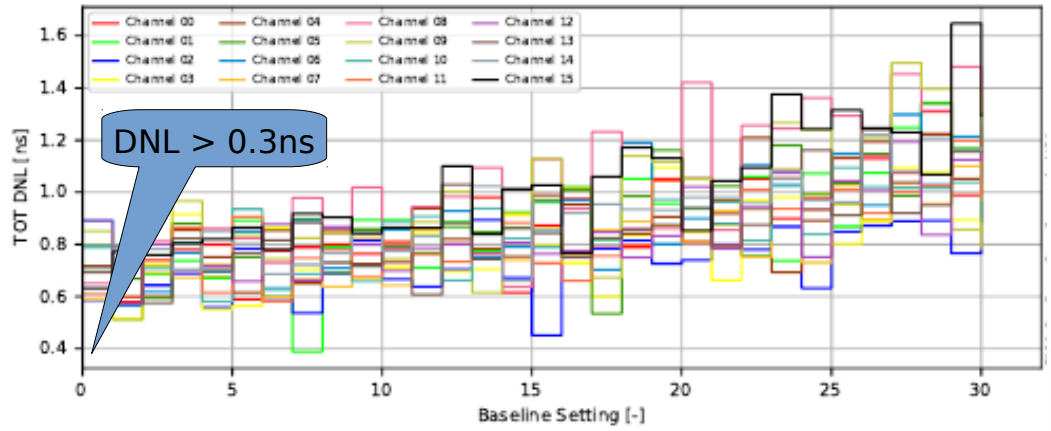
- **Baseline DACs test** (for 4mV20ns only)
  - checks DACs monotonicity with DAC scan and TOT measurements
- **Threshold DAC test** (for 4mV20ns only)
  - checks DAC monotonicity with DAC scan and TOT measurements
- **Baseline measurements** (all configurations)
  - find baseline settings/corrections for all channels
- **Threshold scan** (all configurations)
  - verification of the baseline settings, shows differences between channels after baseline correction
- **Quick channels test** (for 4mV20ns only)
  - checks whether channels give right response for small and big input charges (further measurements possible only when all channels are good)
- **S-curve measurements** (all configurations)
  - measure the number of counts versus input charge for selected thresholds, to calculate noise, gains, etc.
- **TOT Scan** (all configurations)
  - measure the TOT value versus input charge for selected thresholds - allows to calculate charge from TOT value for specific threshold



Baseline DAC monotonicity with TOT



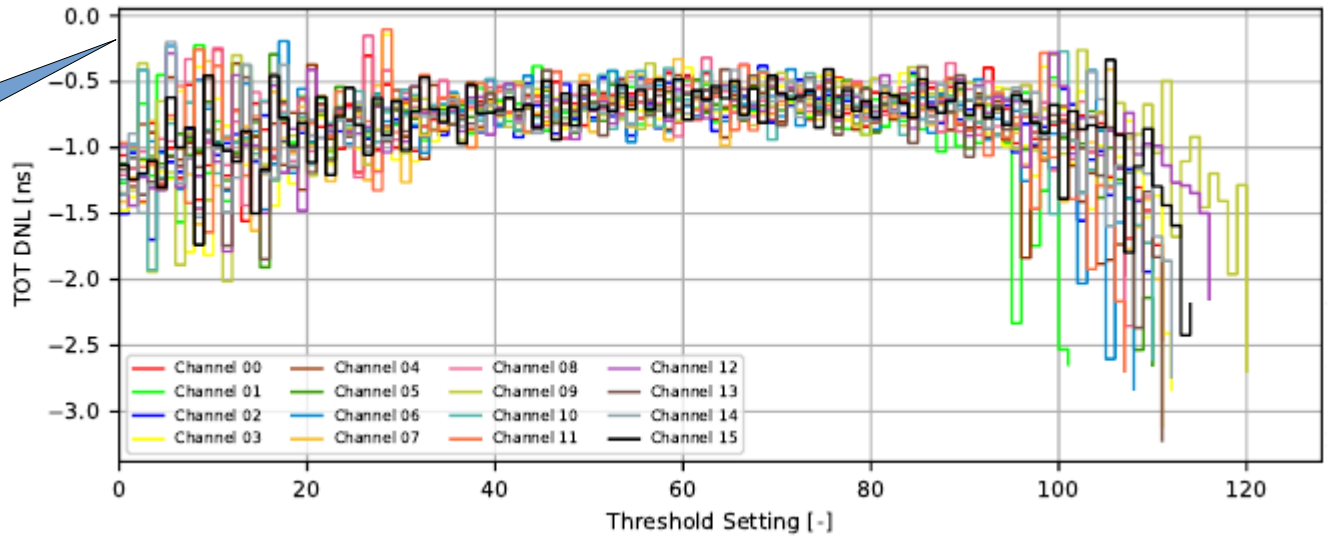




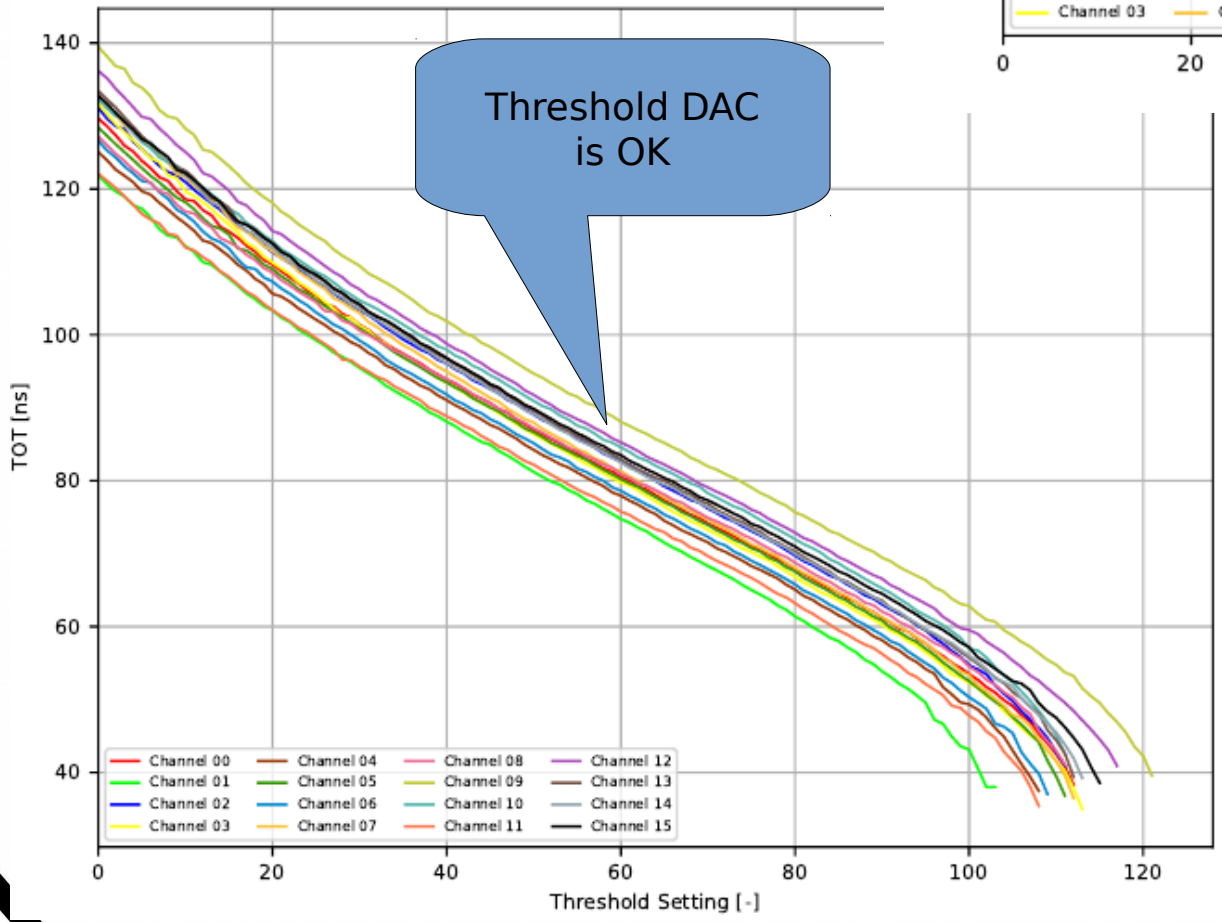
- Measurement done only for configuration 4mV20ns - DACs operation does not depend on gain/Tpeak
- Measurements done with threshold = 24 (baseline settings should be always below threshold)
- Signal is injected to one channel of each ASIC at a time (high amplitude, always above threshold)
- The TOT values versus baseline settings are collected

Threshold DAC monotonicity with TOT

DNL > -0.2ns



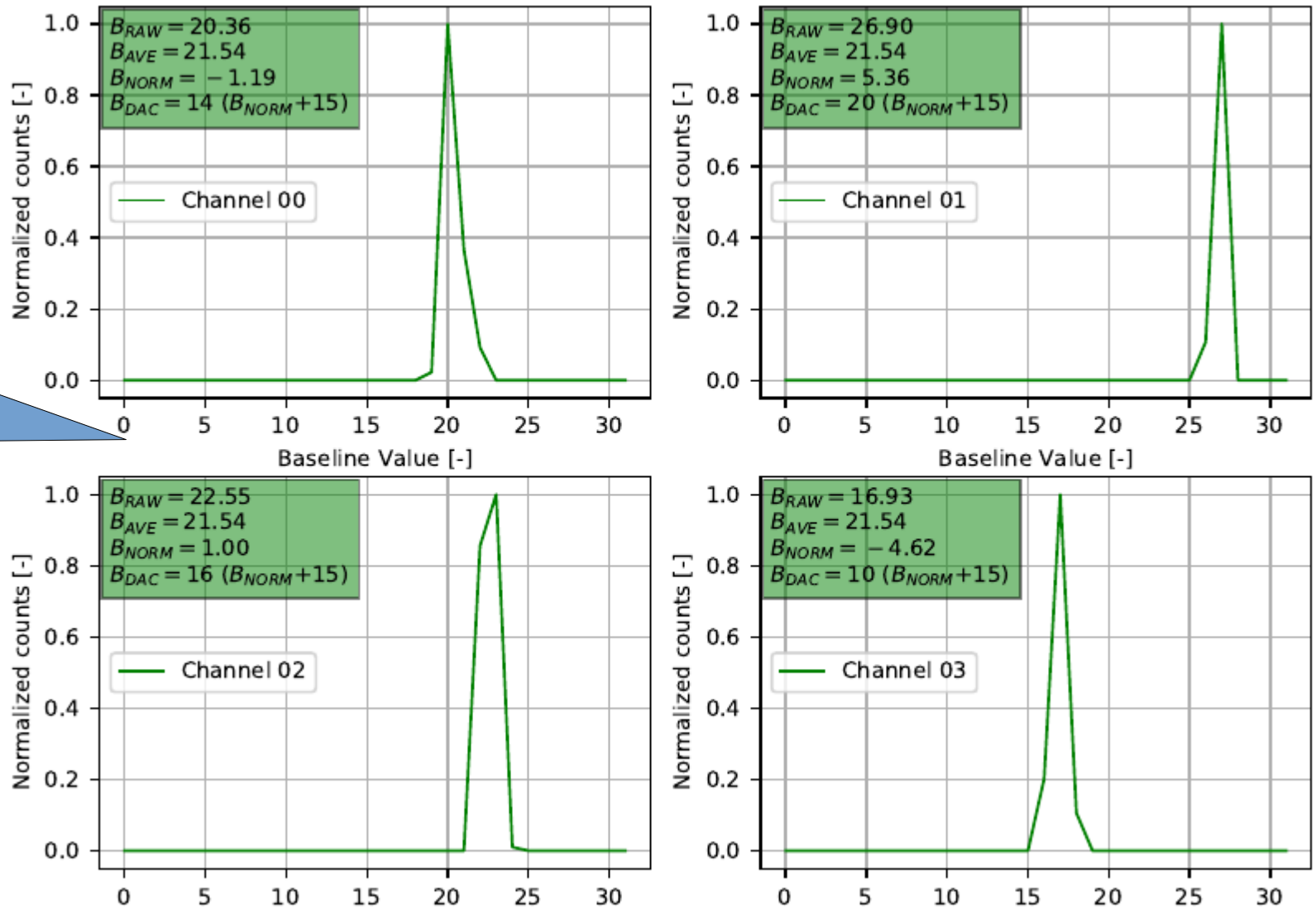
Threshold DAC is OK



- Measurement done only for configuration 4mV20ns - DAC operation does not depend on gain/Tpeak
- Measurement done with baselines setting = 0 (baseline should be always below threshold)
- Signal is injected to one channel of each ASIC at a time (high amplitude, always above threshold)
- The TOT values versus threshold setting are collected

Baseline scan measurements

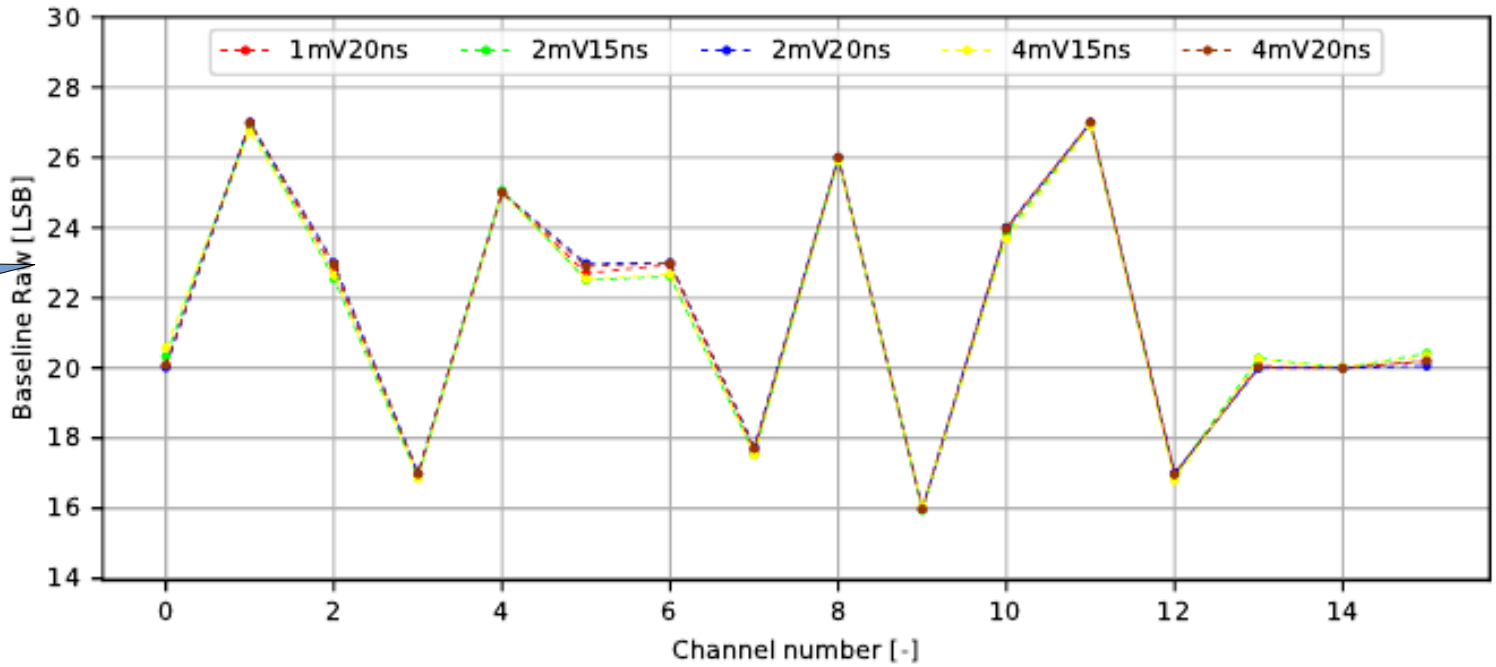
Example measurements for few channels in one configuration



- Measurements done with threshold = 0, for each typical configuration
- Small signal at high frequency (10MHz) is additionally injected to all channels to increase overall noise of the system (noise should be higher than DAC LSB to get counts for at least one of the baseline settings)
- Baseline corrections B_{NORM}, calculated as B_{RAW} - B_{AVE}, are shifted to the center of the possible baseline setting

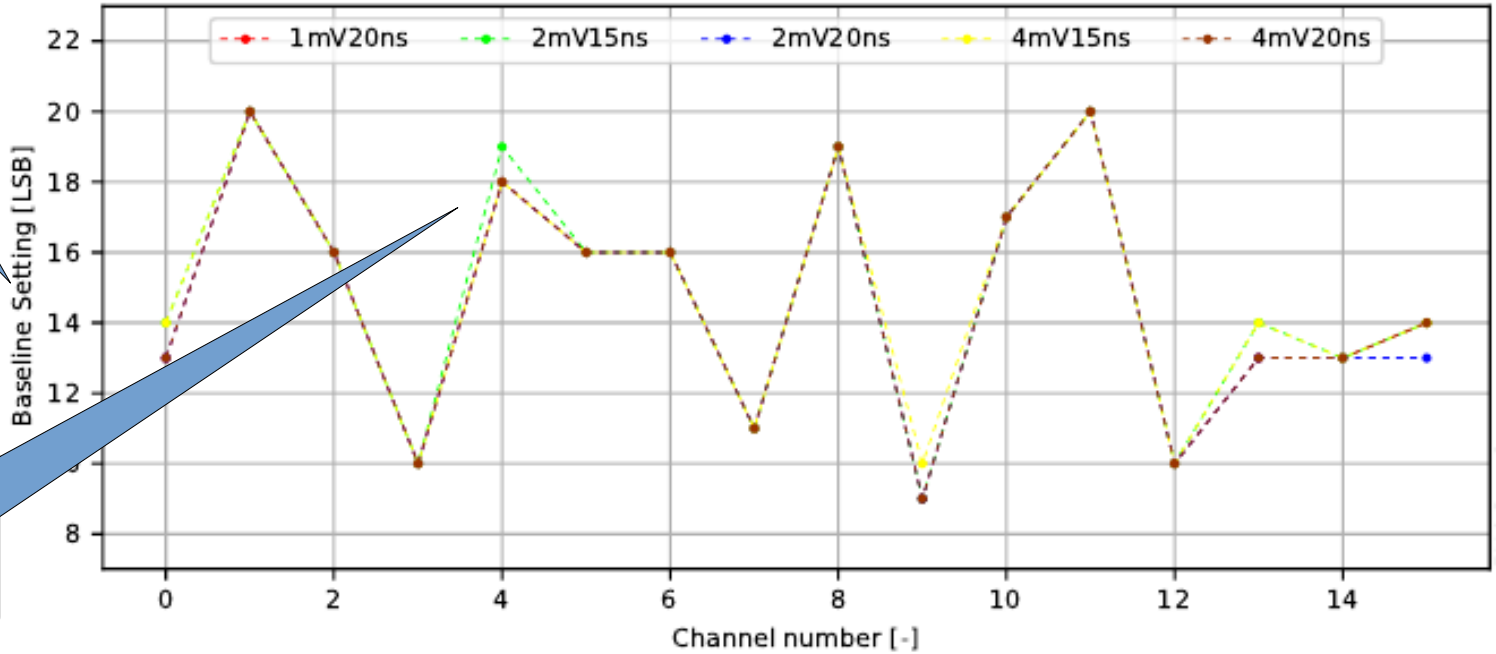
Baseline scan measurements - parameters

Raw baseline value from baseline scan procedure



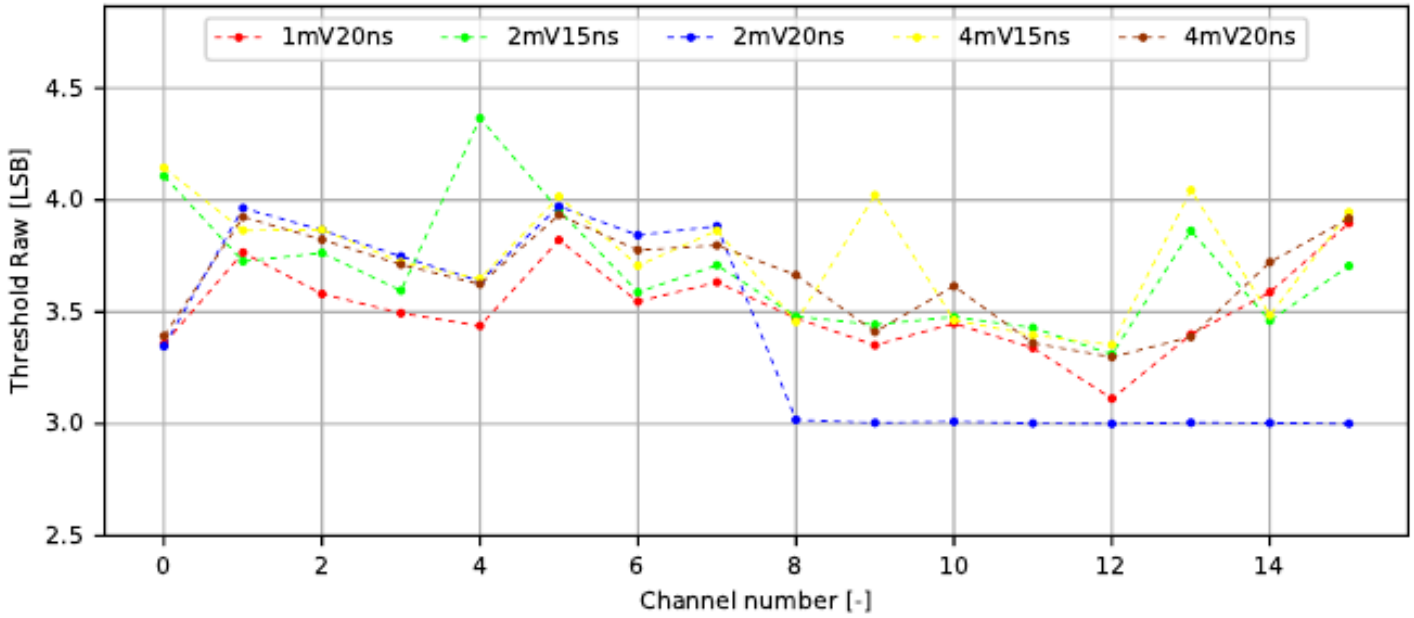
Baseline settings values which should be set in baseline registers to get proper baseline corrections

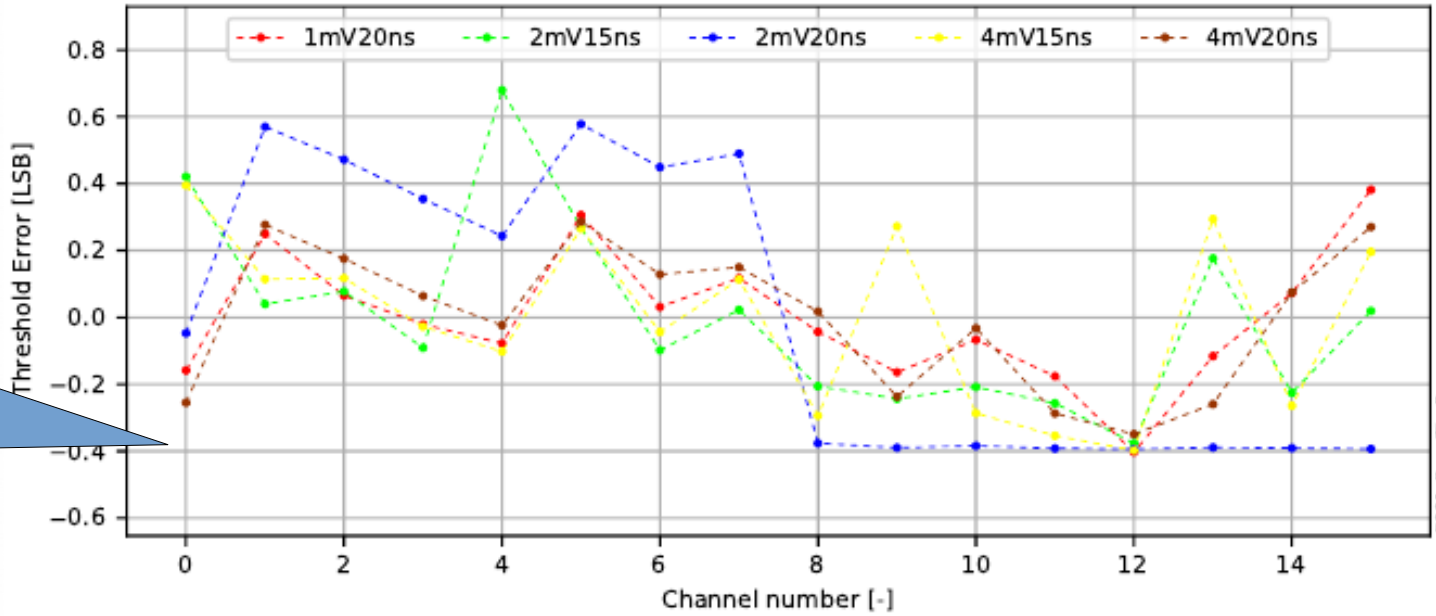
Usually the corrections are the same or very similar for all configurations



Threshold scan – baseline verification

- Measurements done after baseline correction shifted to the highest possible values (channel with highest baseline is set to 31)
- Threshold is changing from 0 to ~20 and the average value of threshold setting, based on counts distribution, is measured for each channel
- Threshold errors are obtained as difference from average value for all channels in specific FEB

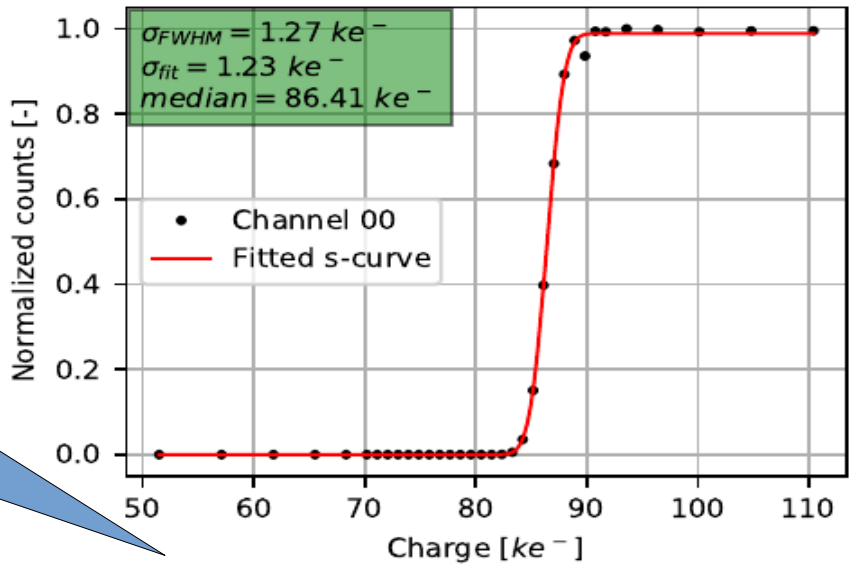


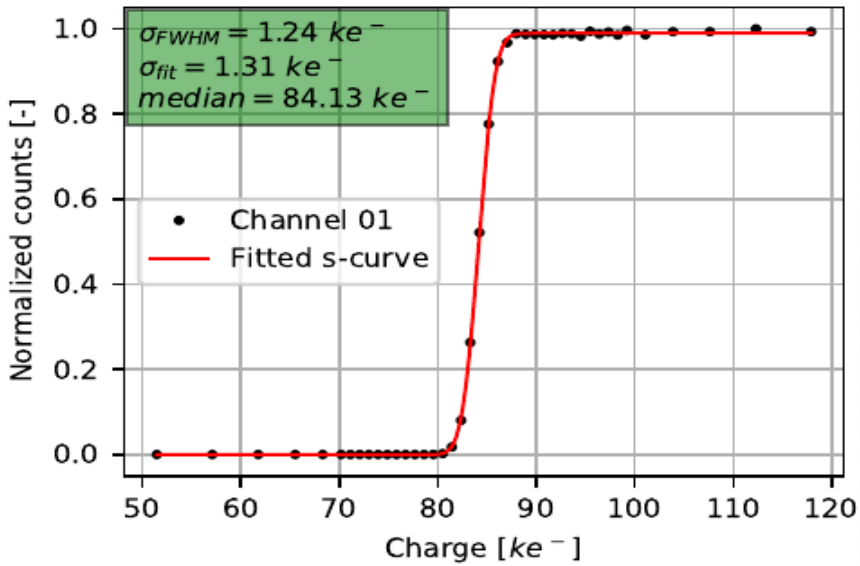


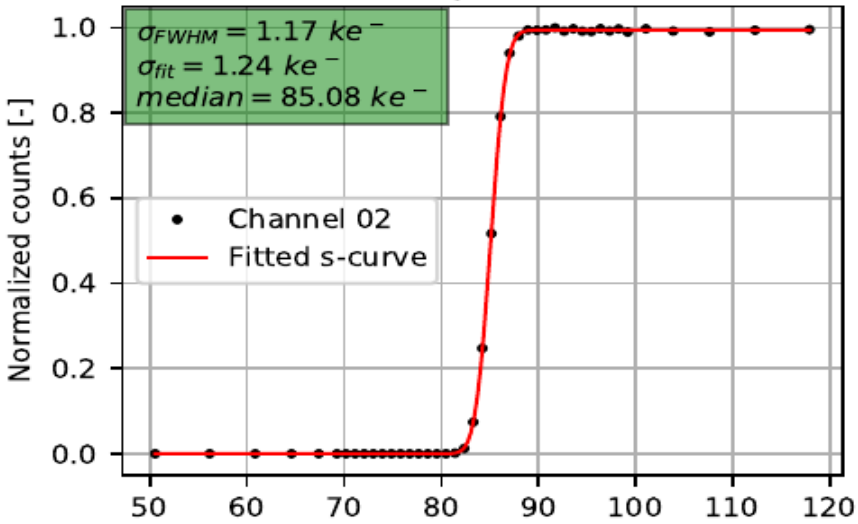
Threshold error in range +/-0.5 means that baseline is successfully corrected. Values +/-0.75 are also acceptable

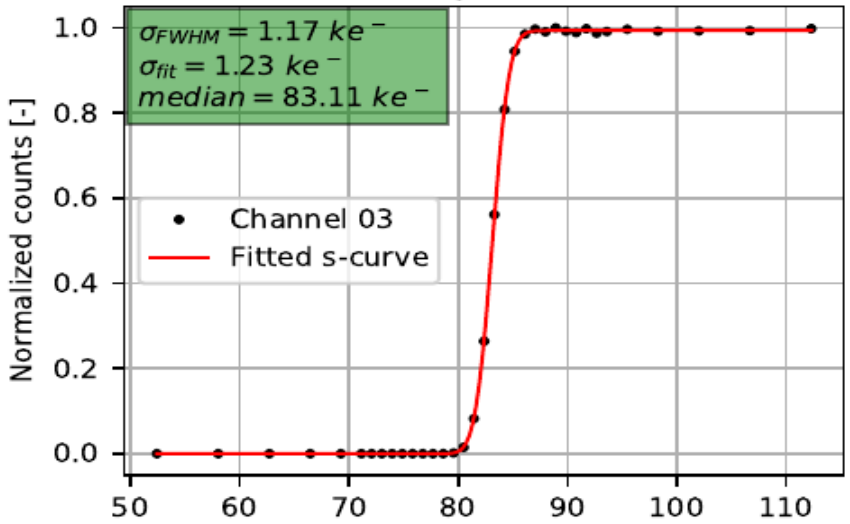
S-curve measurements

Example measurements for first four channels



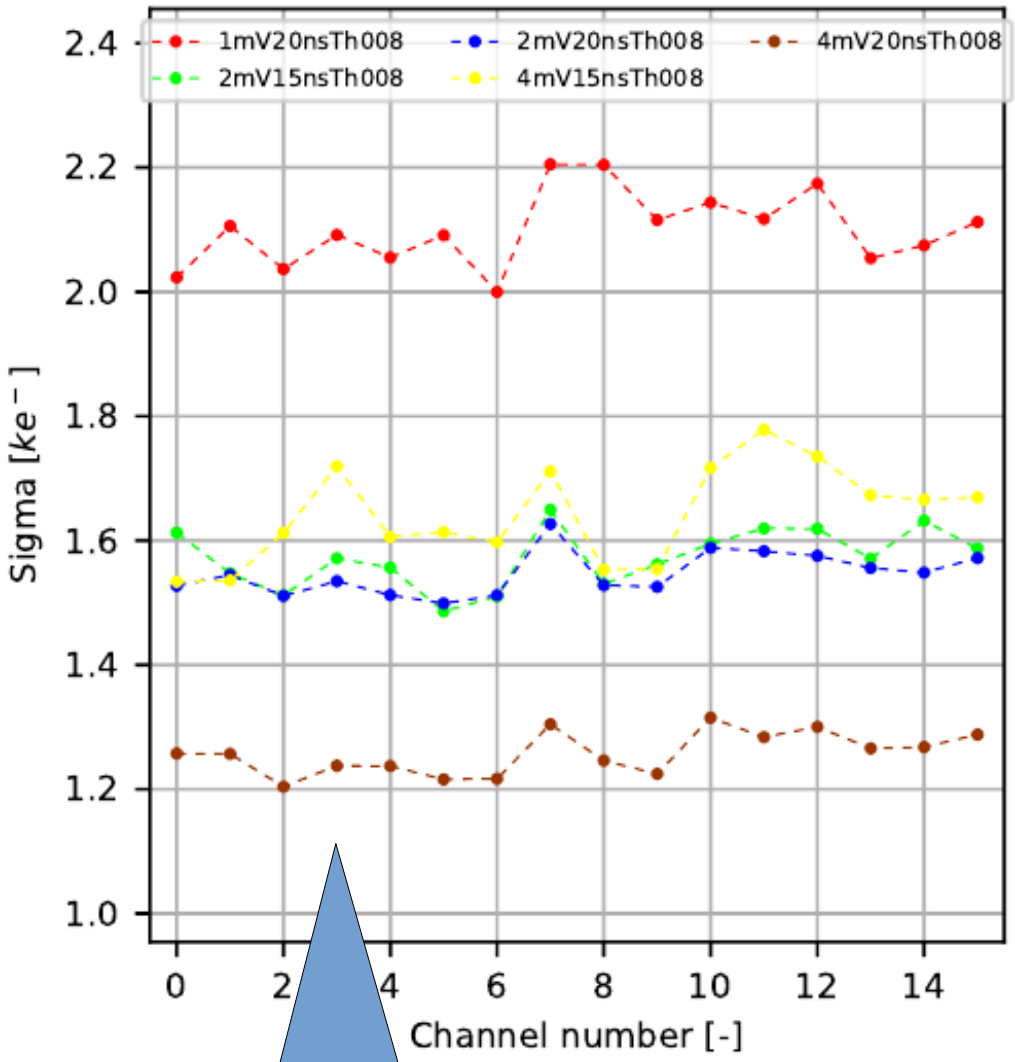


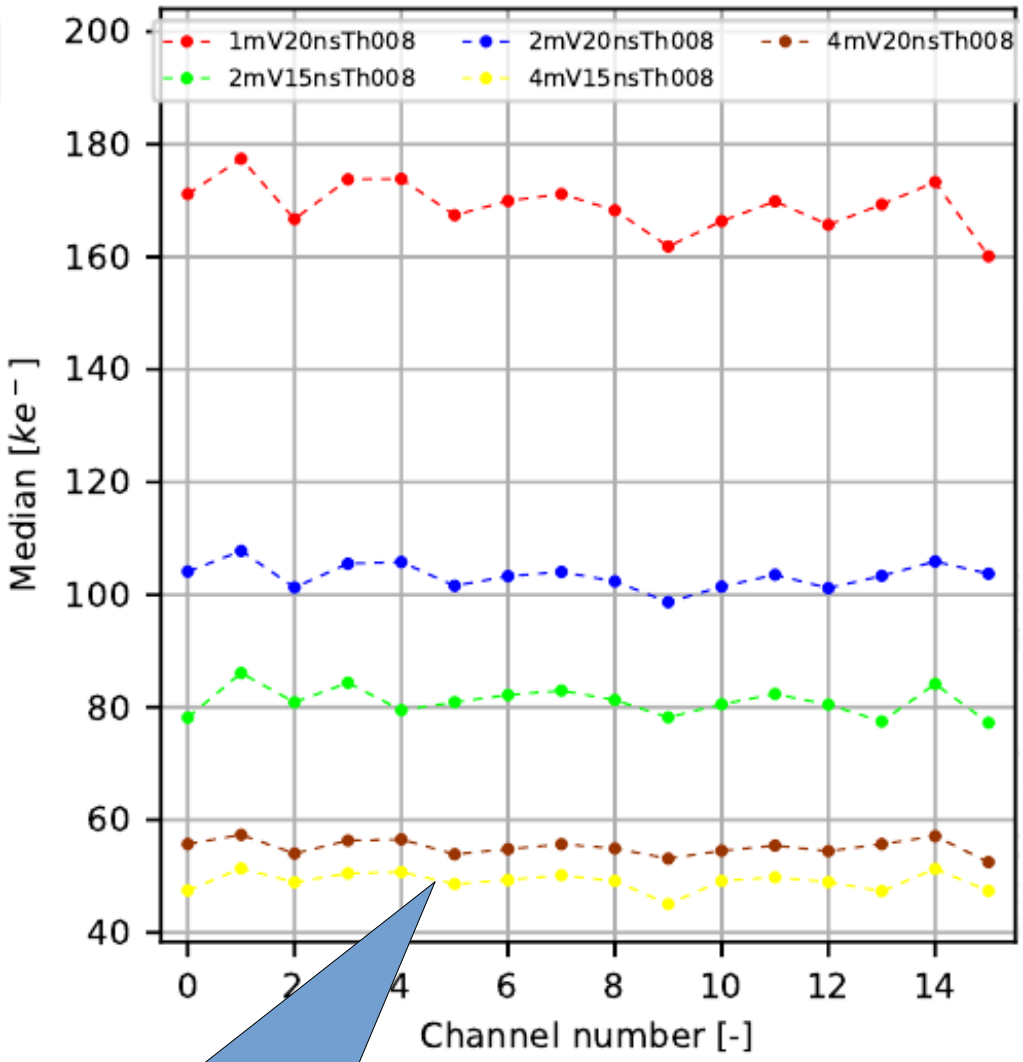




- Measurements done after baseline correction for thresholds 0-25
- Signal is injected to one channel of each ASIC at a time
- Input charge (generator amplitude) step is dynamically adjusted, depending on ASIC configuration and number of currently measured counts

S-curve measurements - parameters



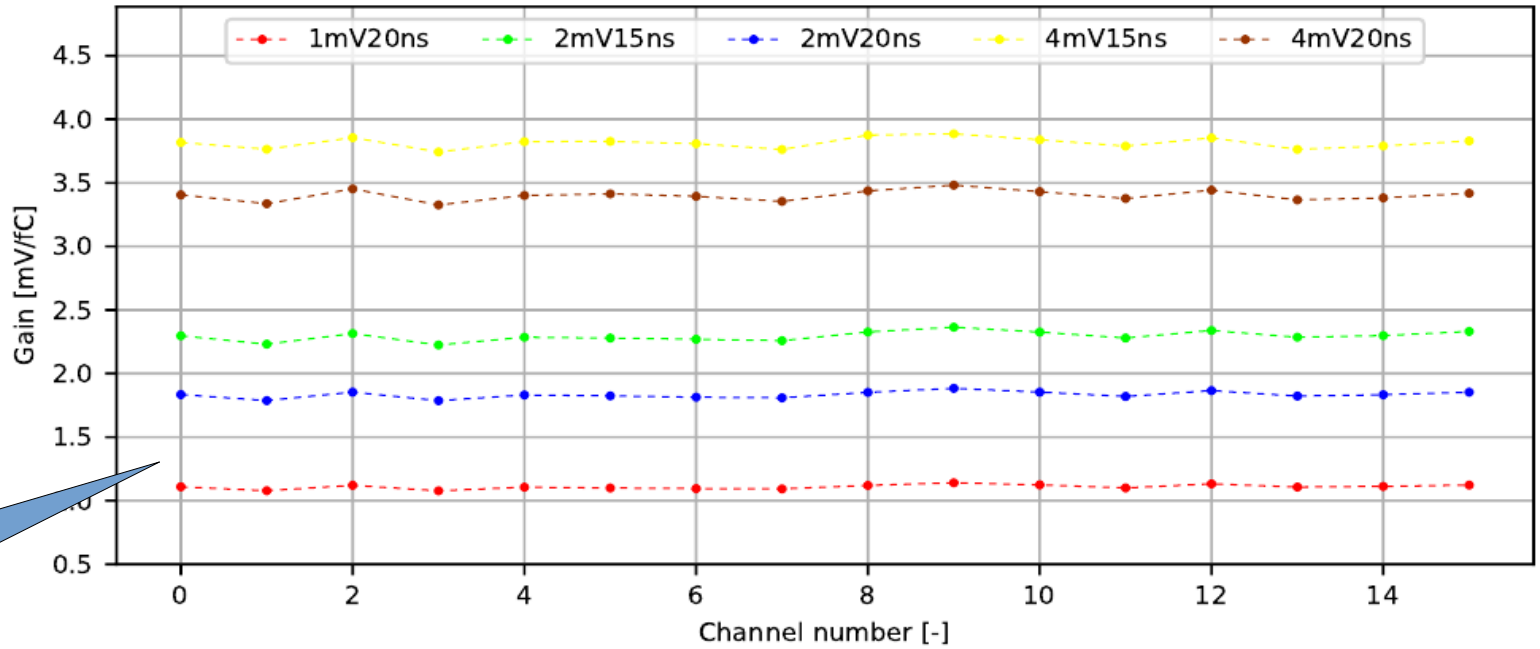


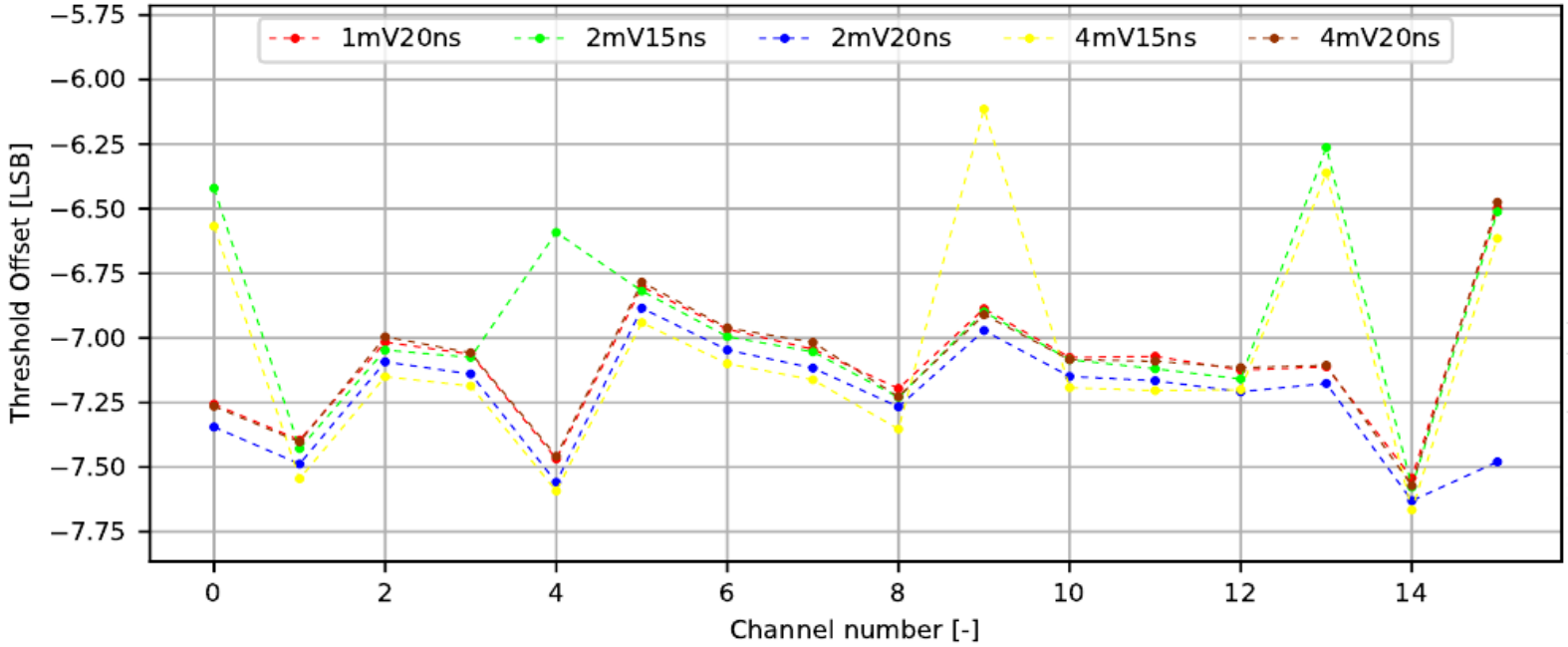
Sigma from S-curve measurements for all configurations

Small variation of median value for all channels proves that baselines are well corrected

S-curve measurements - gain

Gains for all configurations versus channel

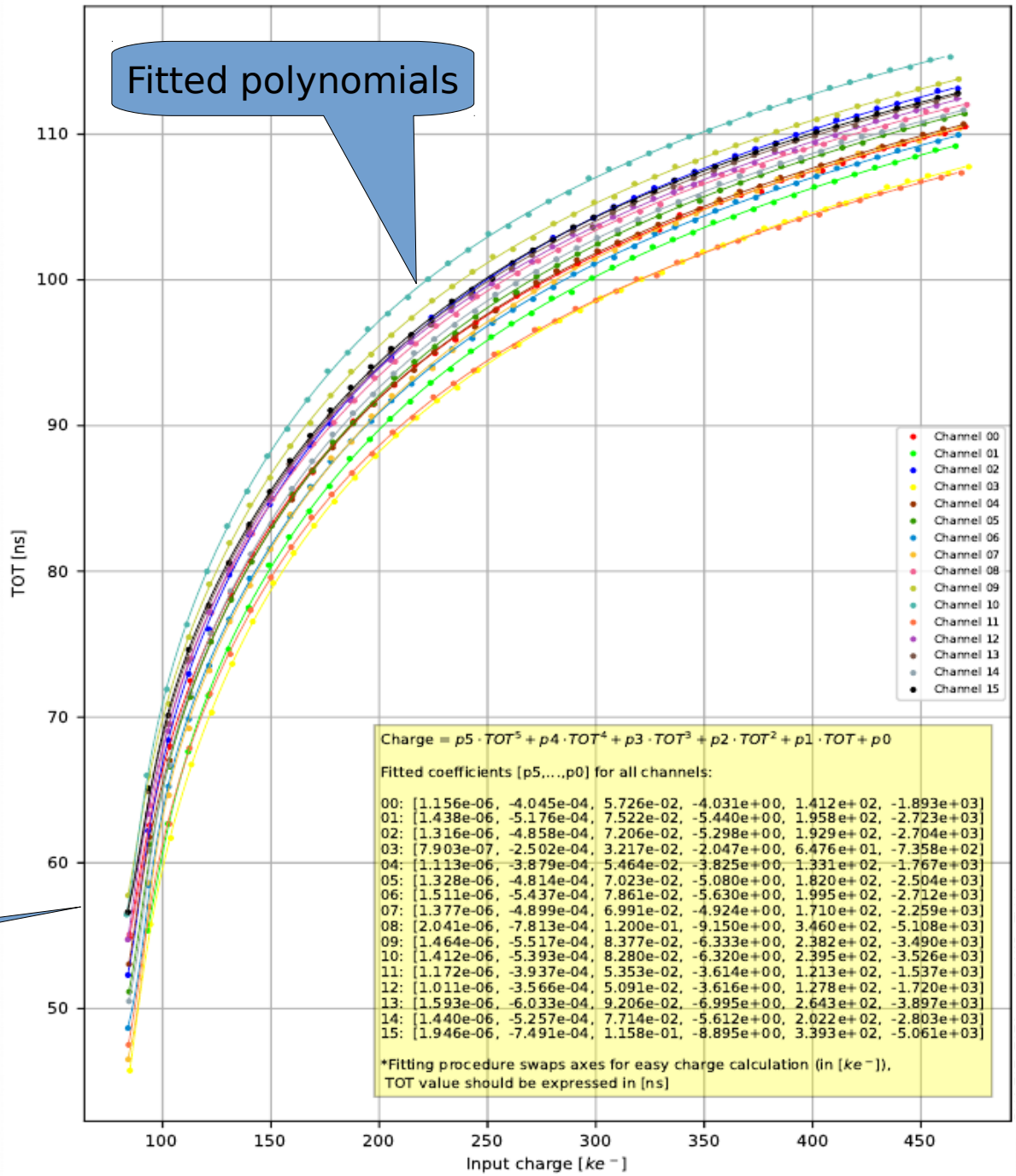




TOT scan

- Measurements done after baseline correction for thresholds: 6, 8, 10, 12, 16, 20
- Signal is injected to one channel of each ASIC at a time
- 5th order polynomial fitted to each of channels
- Input charge in ke^- can be easy calculated based on fitted curves and measured TOT values expressed in ns
- Can such measurement be useful for better amplitude reconstruction?

Example results
Th=8 @ 2mV15ns



Measurements Report

Measurements Report is generated for each FEB separately. It consists of:

- Plots with most important results
- Tables with fitted parameters like: baselines, gains, etc.
- Automatically created comments and notes
- Measurement Status and Summary table with most important numbers

Procedure/Parameter	Value	Status
Comm. with ASIC0 (channels: 0-7), registers (write & read)	-	pass
Comm. with ASIC1 (channels: 8-15), registers (write & read)	-	pass
Minimum DNL[1] of Baseline DACs during TOT mesurements	0.49 ns	pass
Minimum (negative) DNL[1] of Treshold DACs during TOT mesurements	-0.10 ns	near
Minimum raw baseline value	15.9 LSB	pass
Maximum raw baseline value	27.0 LSB	pass
Minimum threshold error after baseline correction	-0.40 LSB	pass
Maximum threshold error after baseline correction	0.68 LSB	pass
Maximum Gain variation (max-min)/average ...		
... at configuration: 1mV20ns	5.7 %	pass
... at configuration: 2mV15ns	6.1 %	pass
... at configuration: 2mV20ns	5.3 %	pass
... at configuration: 4mV15ns	3.7 %	pass
... at configuration: 4mV20ns	4.6 %	pass
Maximim Noise (sigma)...		
... at configuration: 1mV20ns	2.45 ke^-	pass
... at configuration: 2mV15ns	1.73 ke^-	pass
... at configuration: 2mV20ns	1.68 ke^-	pass
... at configuration: 4mV15ns	1.88 ke^-	pass
... at configuration: 4mV20ns	1.37 ke^-	pass

Parameter status: pass, near or fail. Gives fast feedback from measurements

Example report is available on conference site

Tested FEBs summary

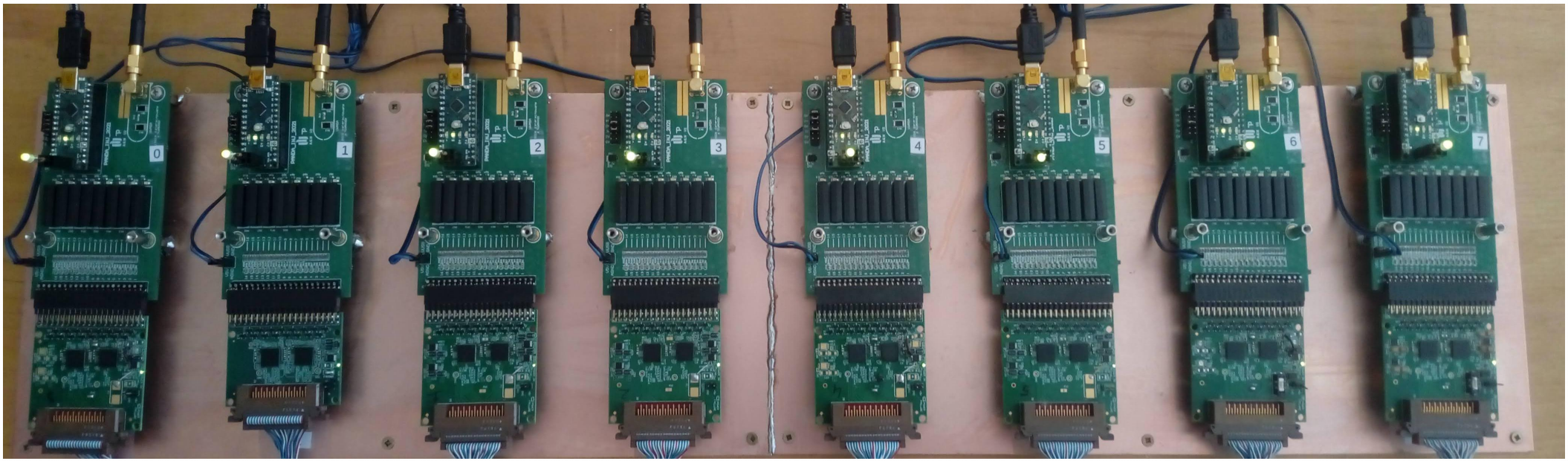
FEBs are named E000-E139

- 132 FEBs are considered good
- 8 FEBs are marked as failed
  - 4 FEBs (E025, E042, E096, E136) work relatively well, but:
    - in one of the two chips too large offset spread
    - threshold DAC cannot set very low thresholds (1-2 LSB) for one channel
  - 1 FEB (E039) has problem with DNL of Threshold DAC
  - 3 FEBs (E024,E081, E129) have communication problem (slow control) in one of two chips.
    - two of them (E024,E081) show reasonable behavior in default settings
    - third FEB (E129) has one chip which does not respond
- Yield estimation – 94% for FEBs, 97% for PASTTRECs – assuming that all FEBs considered presently good, will be verified as good in the experiment

Summary and Future plans

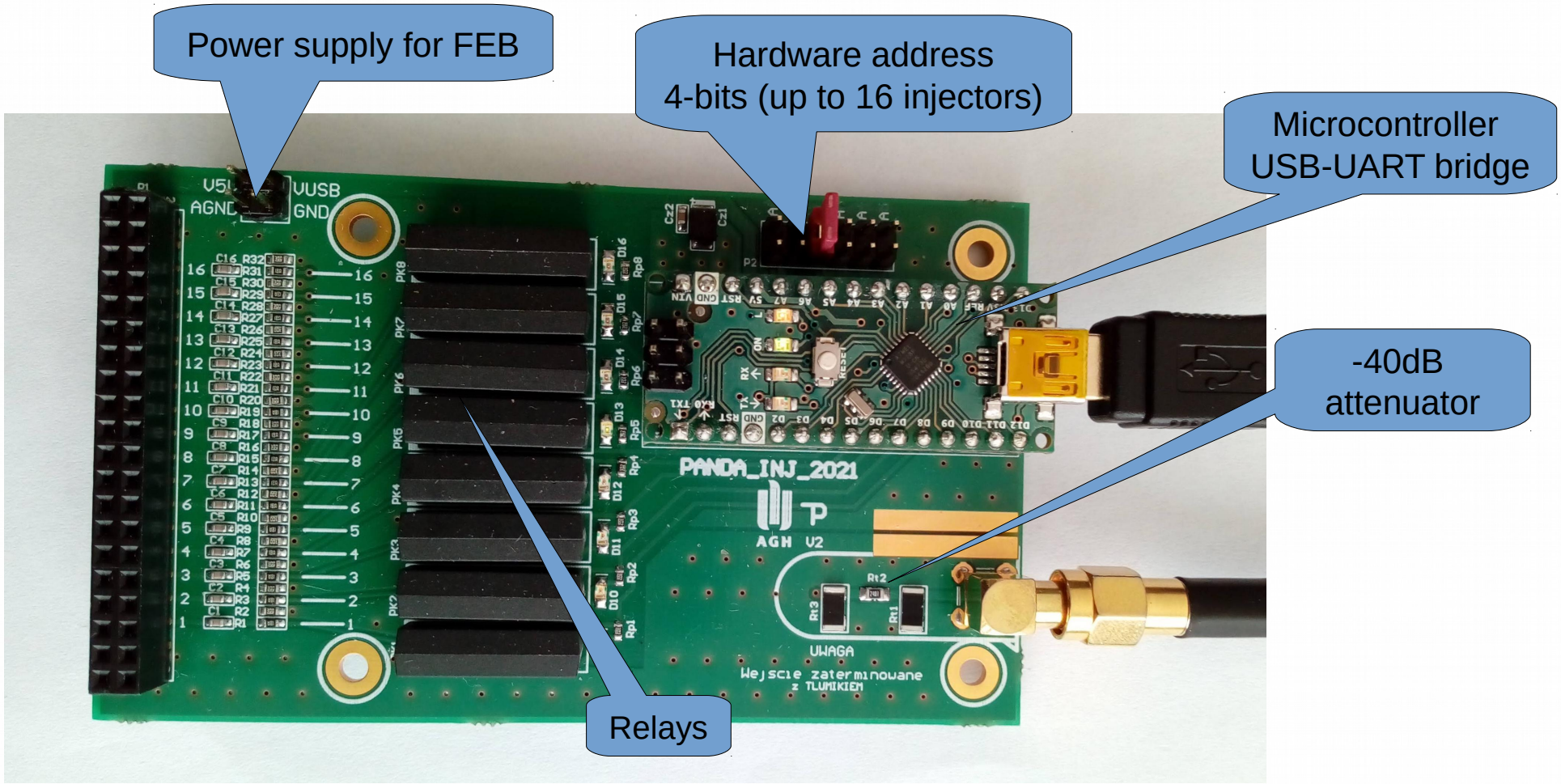
- Setup for mass tests with 8 FEBs – done
- First set of (long) test procedures – done
- First version of software for data analyses and plotting - done
- Tests of 140 prototype FEBs (partially for HADES) – done
- Optimization of test procedures and software - in progress
- Feedback on operation of tested FEBs in FT&STT setups – needed

  to work out the final set of tests for mass production !



BACKUP SLIDES

Charge Injector – compact prototype



Design goals of the charge injector

- Signal from generator delivered to one or more PASTTREC inputs
- All blocks integrated in one, as simple as possible, board
- Separated digital and analogue grounds
- Power supply for FEB delivered via front connector as in final system
- Hardware addresses of injector boards added (important for multi board testing)