PANDA Collaboration Meeting

Sezione di Torino

Pixel readout status report

G.Mazza
on behalf of the MVD Torino group

Pixel specs

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Pixel size	*100 × 100 μm^2*
Chip active area	*11.4 × 11.6 mm^2 (116 rows, 110 cols)*
dE/dx measurement	*ToT, 12 bits dynamic range*
Max input charge	*50 fC*
Noise floor	*<32 aC (200 e^-)*
Clock frequency	*155.52 MHz*
Time resolution	*6.45 ns (1.9 ns r.m.s.)*
Power consumption	*< 750 mW/cm^2*
Max event rate	*$6 \cdot 10^6$*
Total ionizing dose	*< 100 kGy*

Readout scheme

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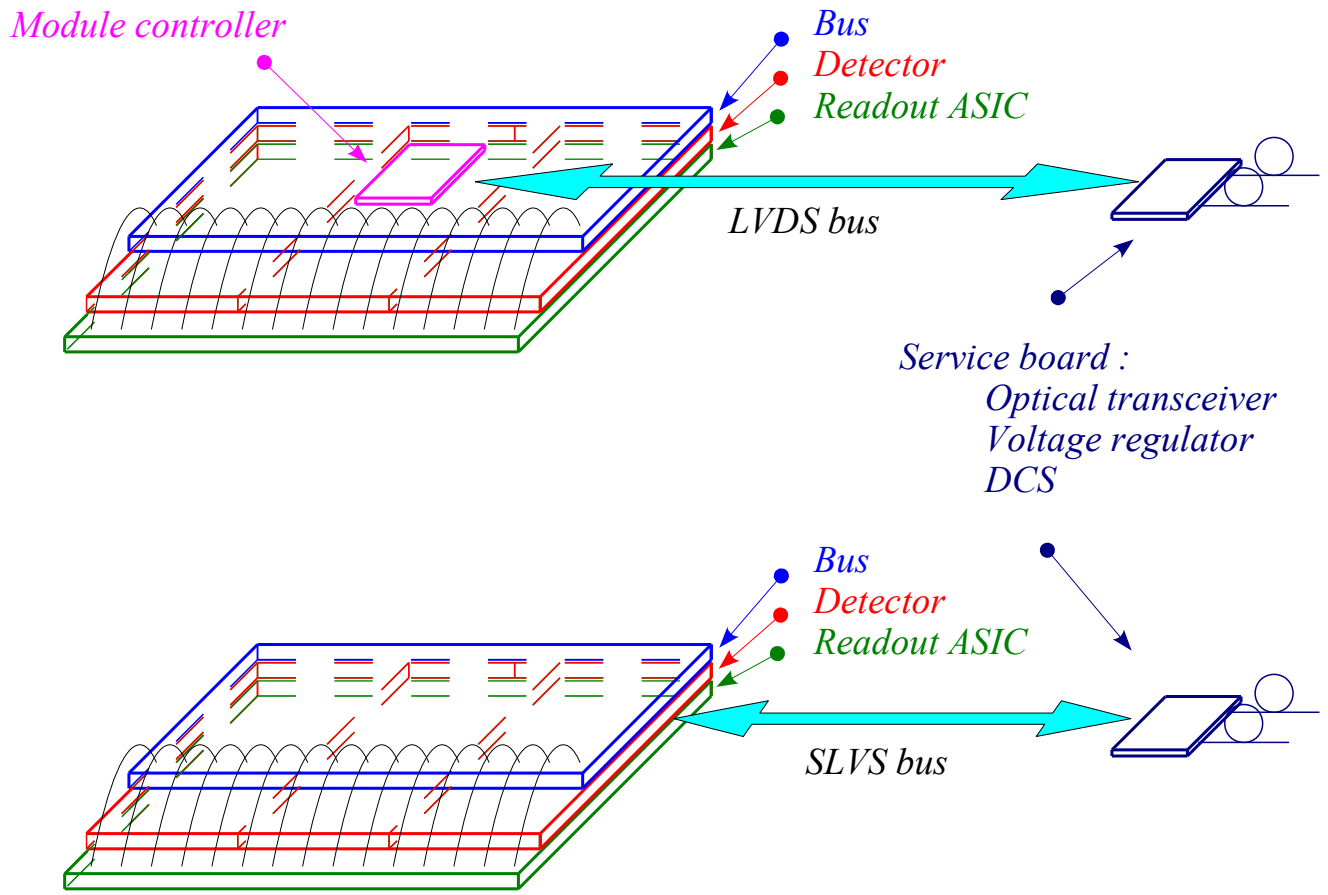

Option 1

Option 2

ToPiX v3

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- Layout submitted on February 7th – received May 16th
- 4.5x4 mm^2 die area
- CMOS 0.13 µm DM technology
- Triple redundancy-based SEU protection
- End of column logic
- 160 Mb/s SLVS serial output
- Pads for bump bonding

Double cell

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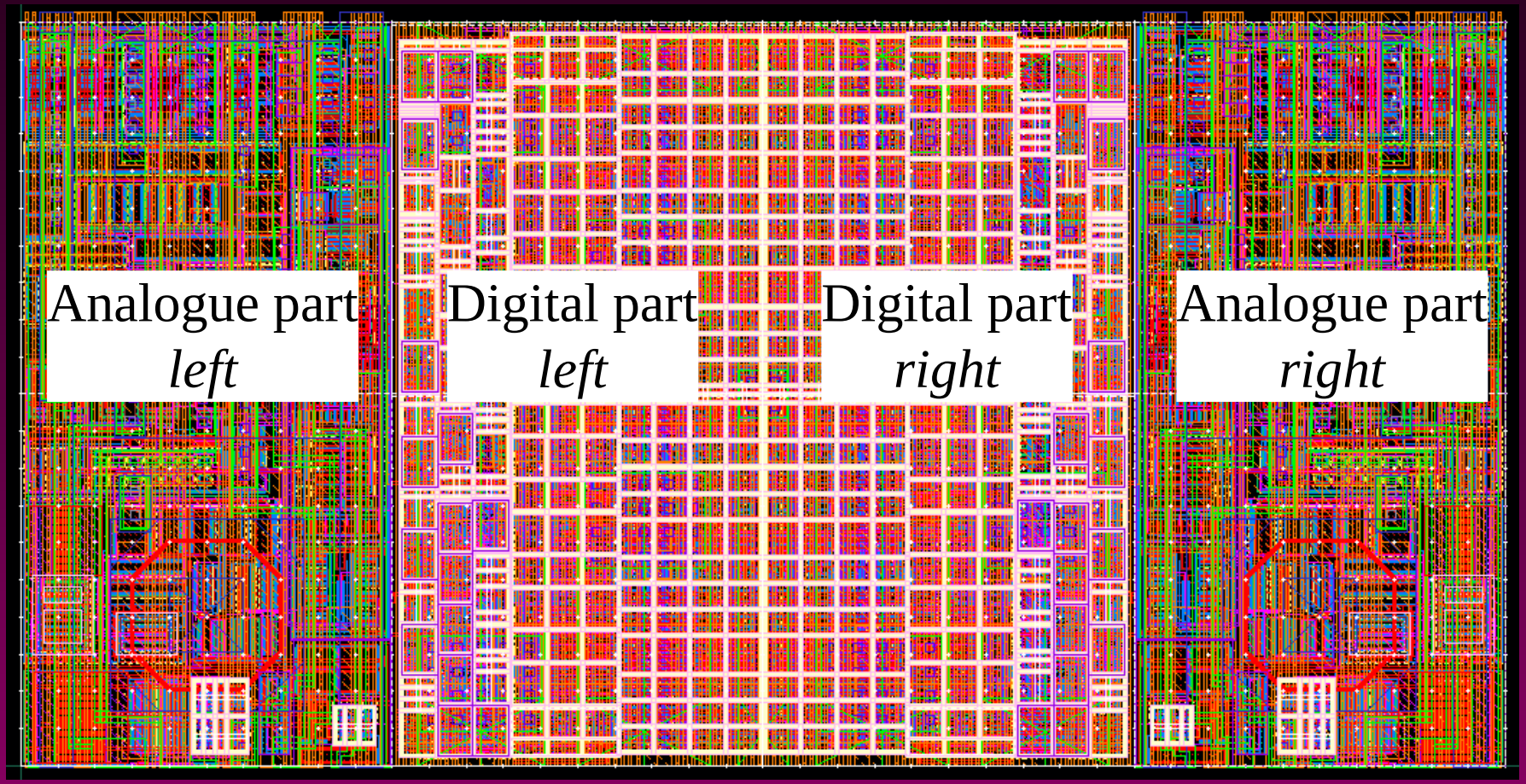

Common bus

End of column

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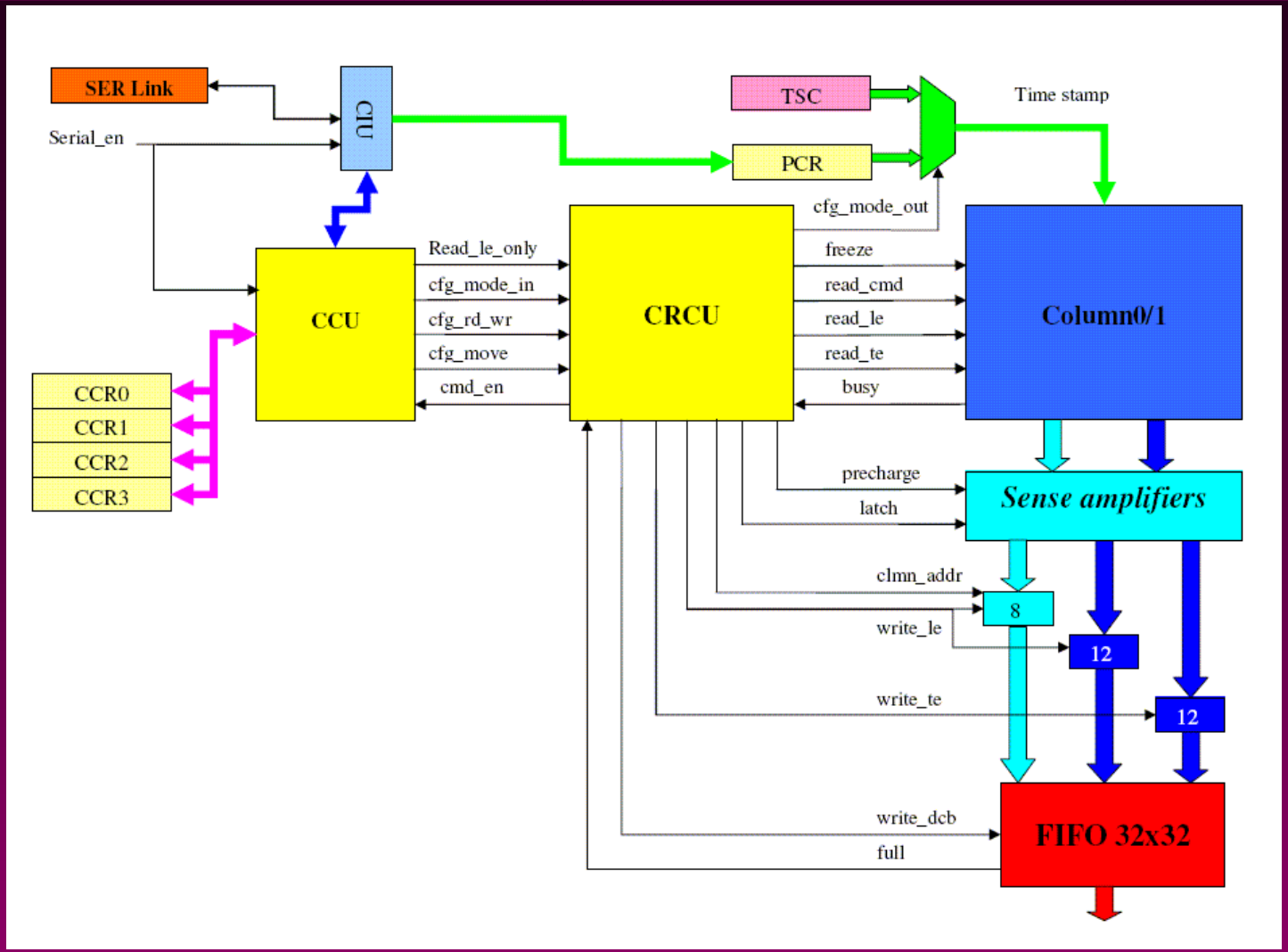

ToPiX v3 layout

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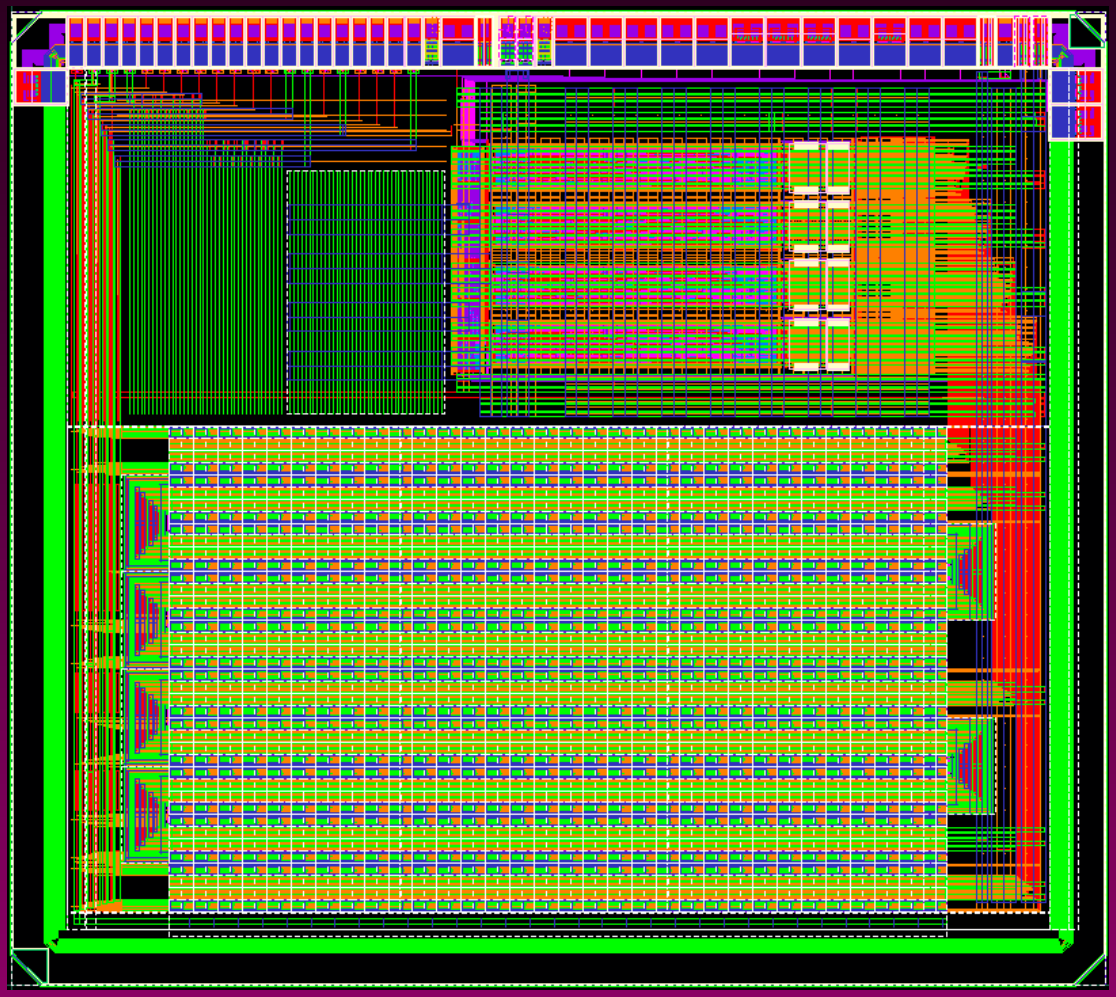

- 4.5 mm × 4 mm
- CMOS 130 nm
- Clock frequency 160 MHz
- bump bonding pads
- 2×2×128 columns
- 2×2×32 columns
- 32 cells EoC FIFO
- SEU protected EoC
- Serial data output
- SLVS I/O

ToPiX v3 test status

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- Four chips (without sensors) mounted
- At 160MHz can only read and program first ~32 pixels of each column
- At 50MHz (with pre-emphasis disabled) full operation
- S-curve working well (programmable internal test pulse)
- Baseline measurements ok
- On-pixel DACs characterised and correction applied
- Optimisation of analogue parameters ongoing but likely to change significantly with sensor assemblies
- Acquisition system is working (4 boards)

Clock frequency problem

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- At 160 MHz only the first 32 pixels of the 128 cells columns work correctly
- Response improves when the frequency is decreased
- Prototype full column has 30% longer bus and 10% more cells than the final chip
  - *unfortunately this is not sufficient*
- better simulation model for the bus is required
- column readout can be slowed down with no significant effects
- new bus driver architecture required ?

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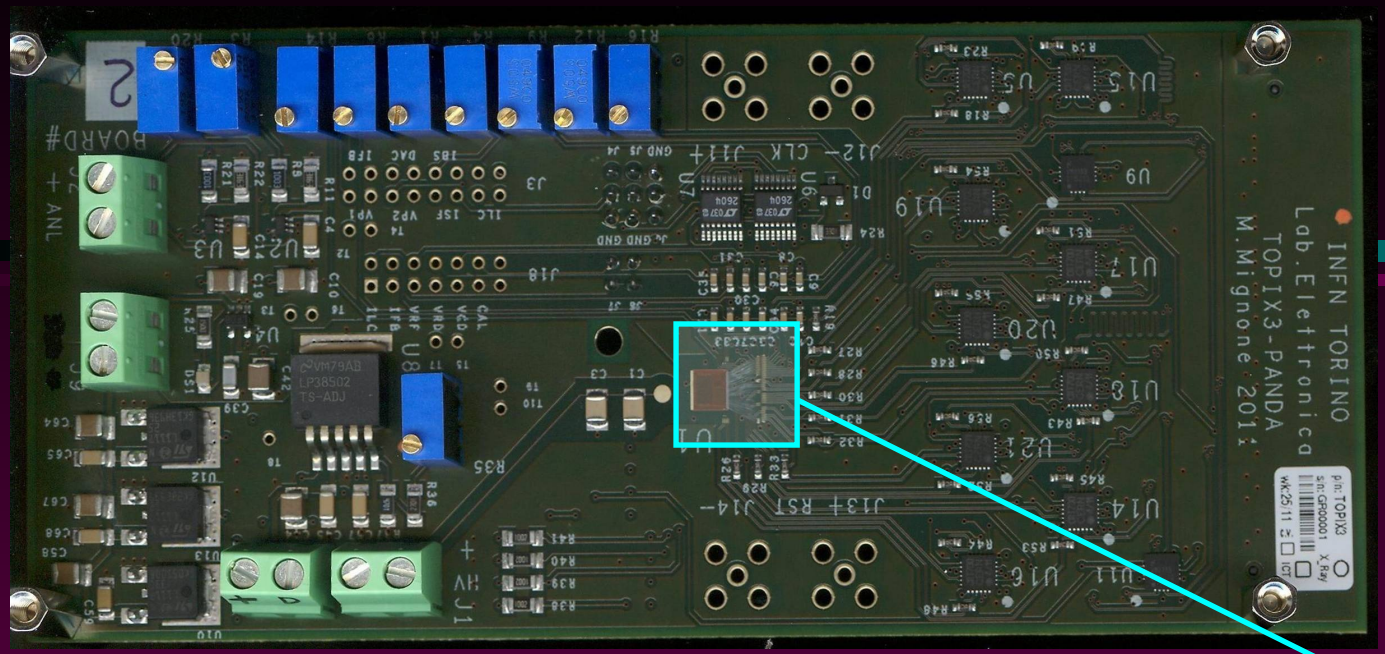
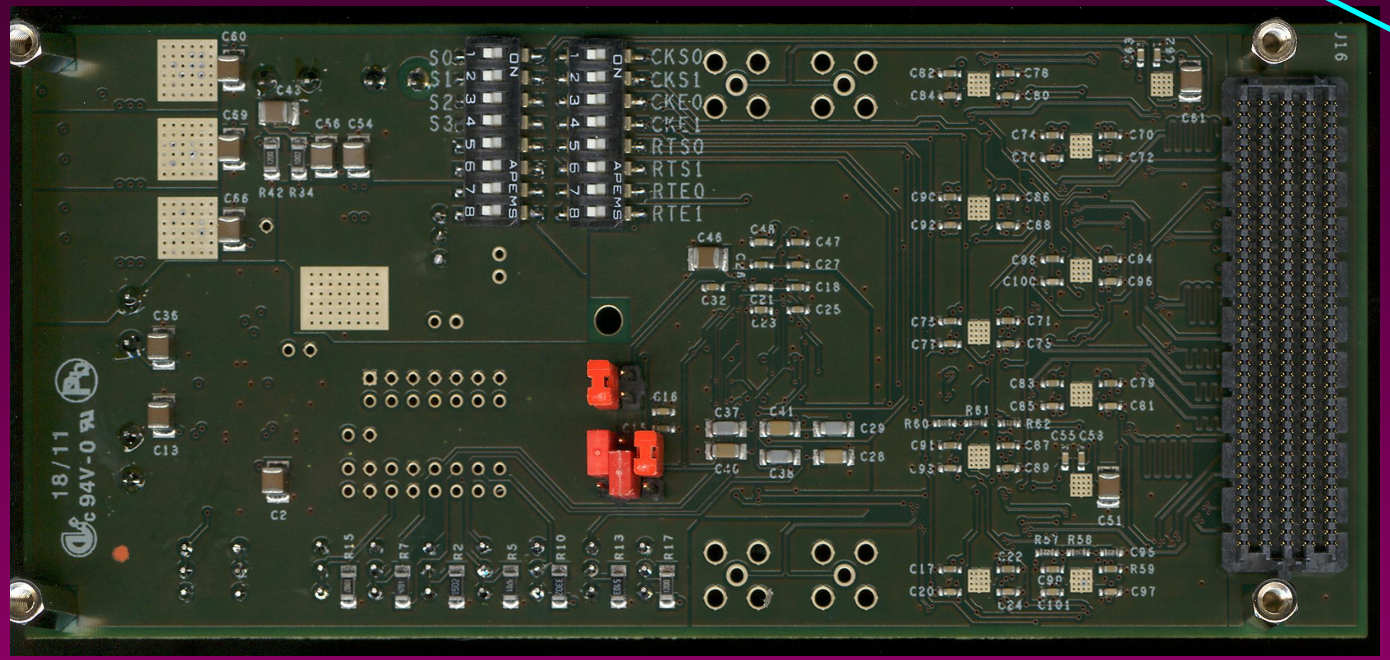
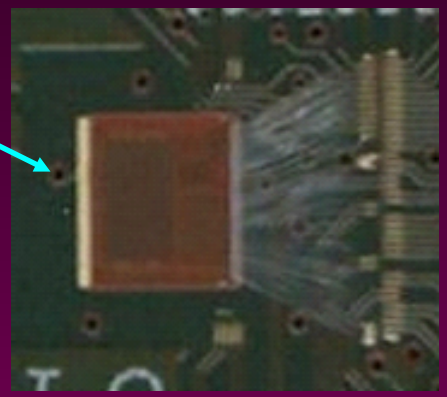
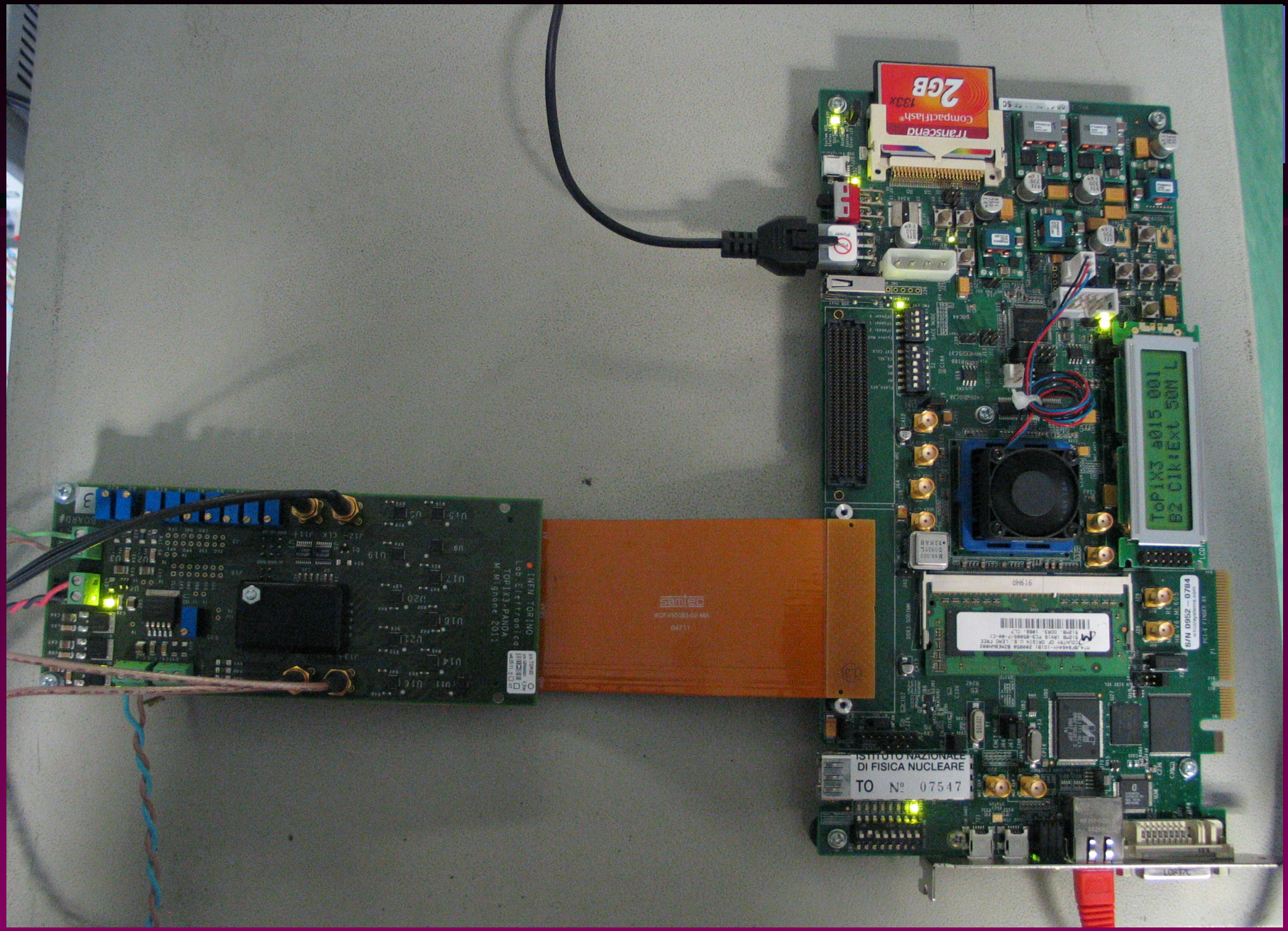
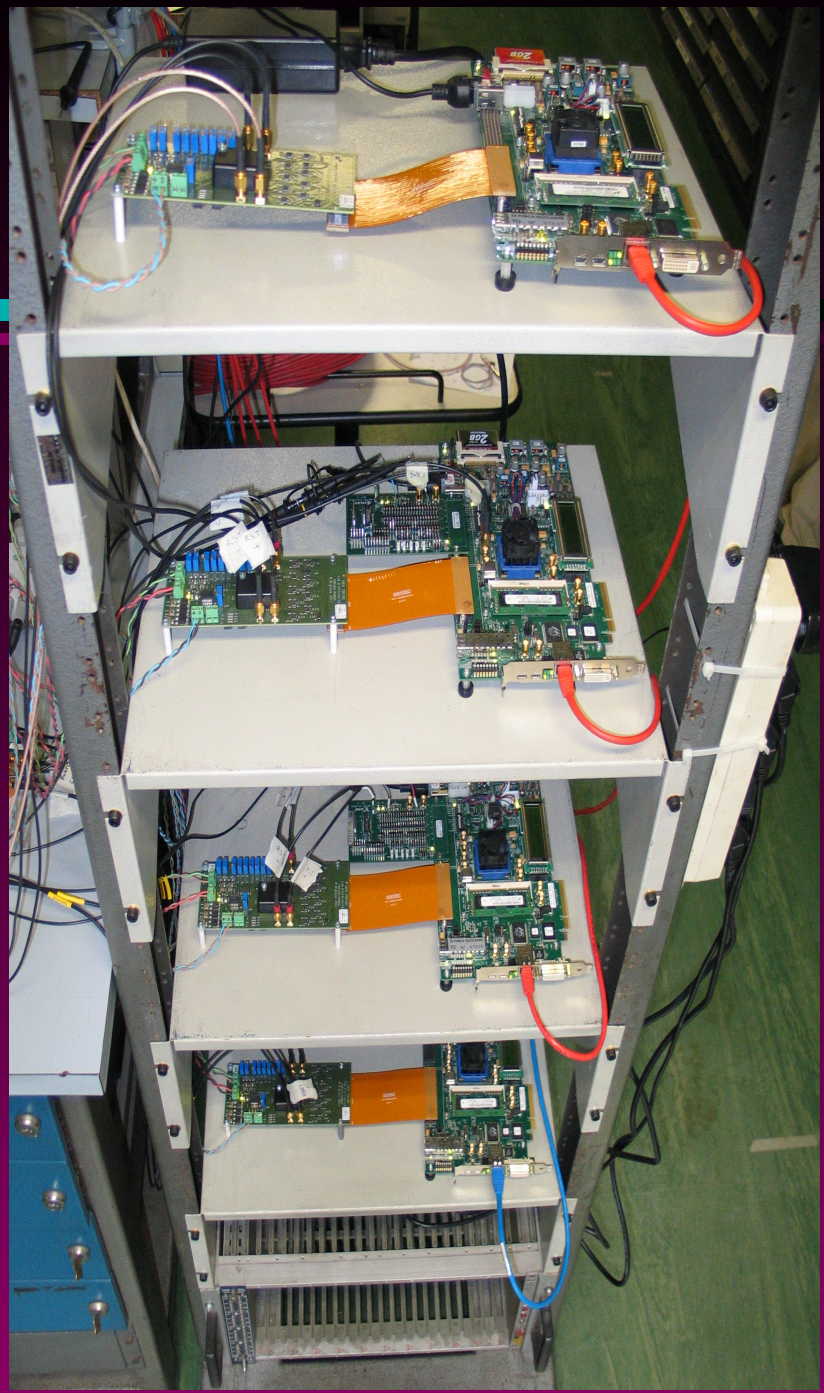




ToPiX v3




2GB
Transcend
CompactFlash
133x
ToPiX3 a015 001
B2 Clk:Ext 50M L
INFN TORINO
Lab. Elettronica
TOPIX3-PANDA
M. Mignone 2011
ISTITUTO NAZIONALE
DI FISICA NUCLEARE
TO Nº 07547



Functional tests @ 50 MHz

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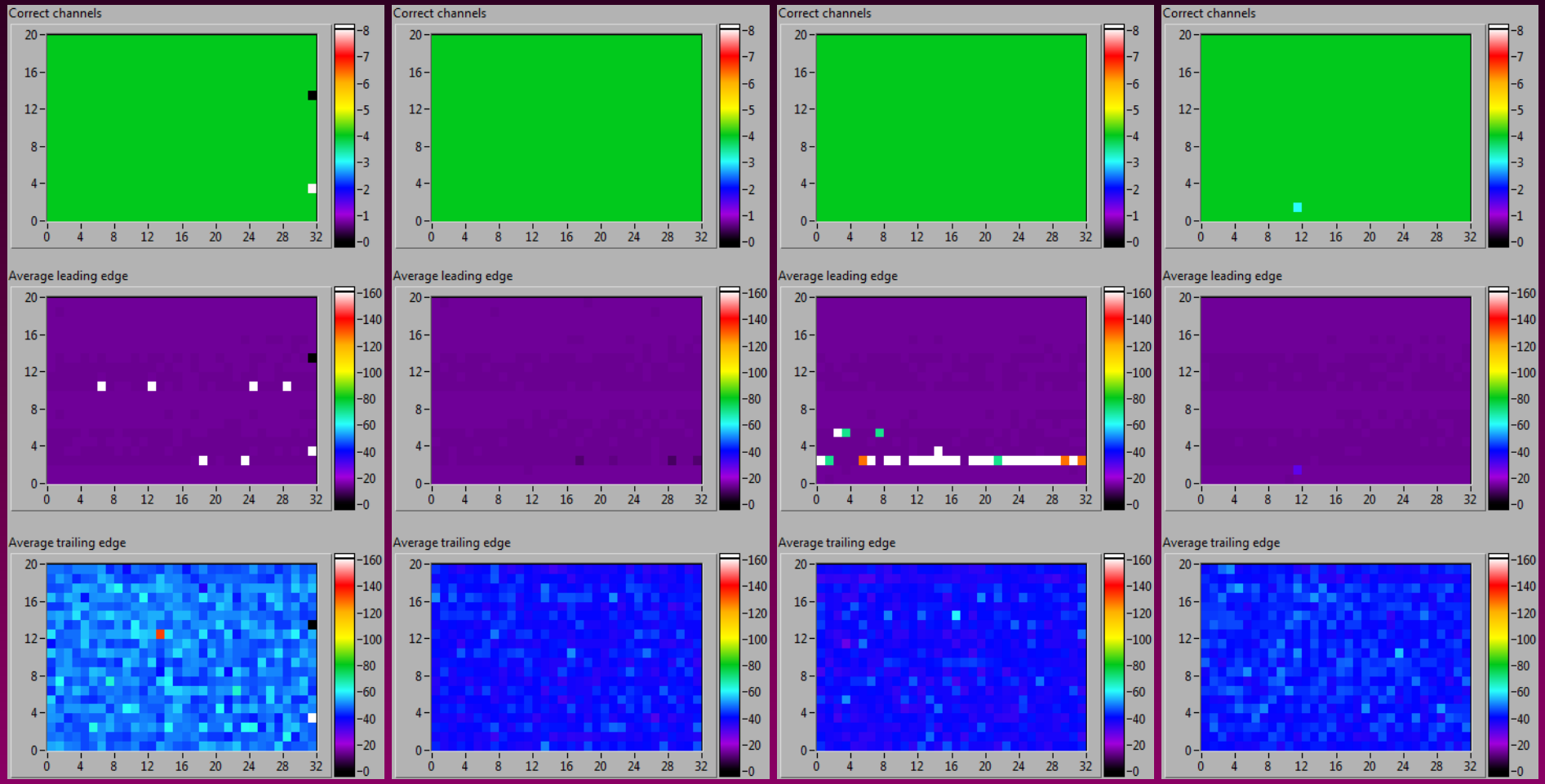
Chip 1	Chip 2	Chip 3	Chip 4



Signal shape

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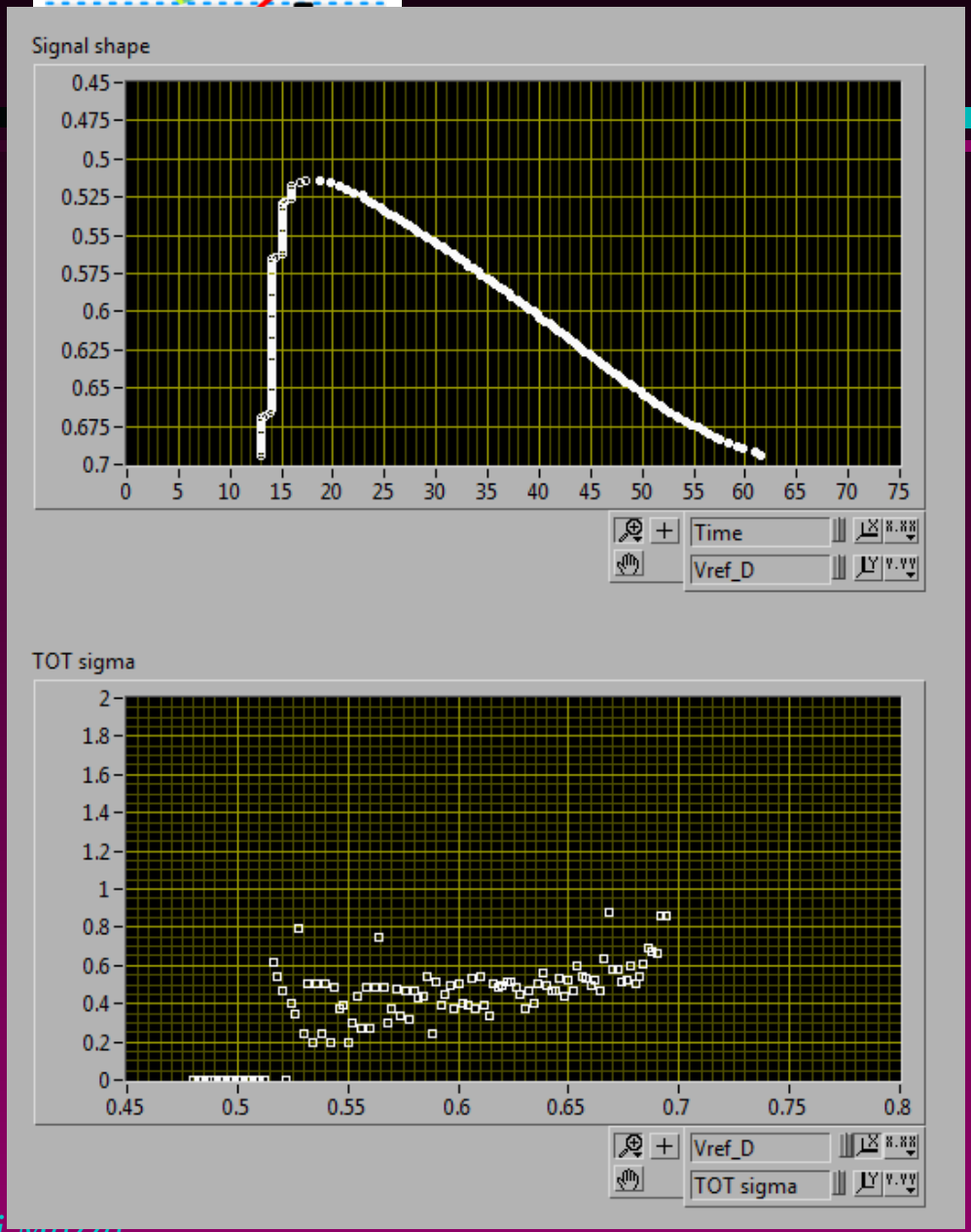

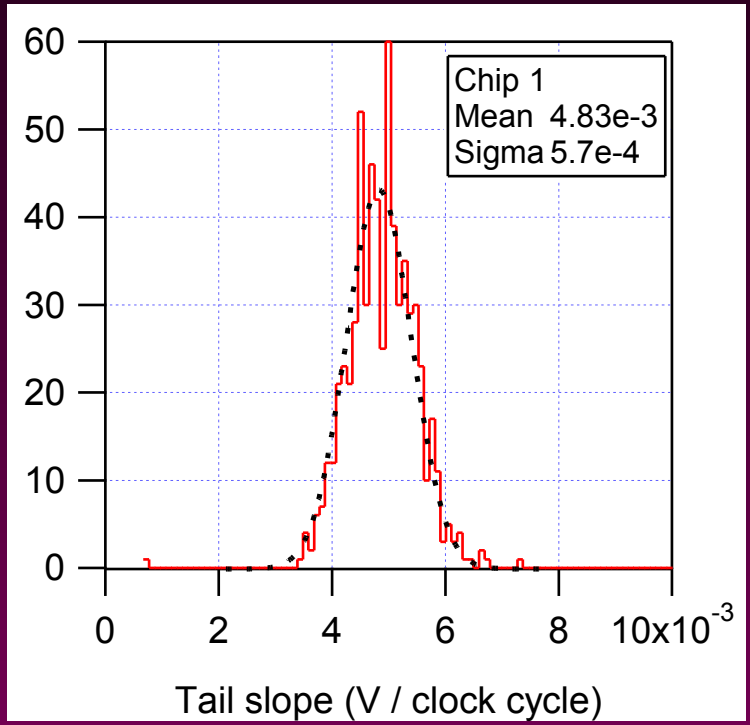

4.14 ns/mV
274 ns/fC

Baseline correction

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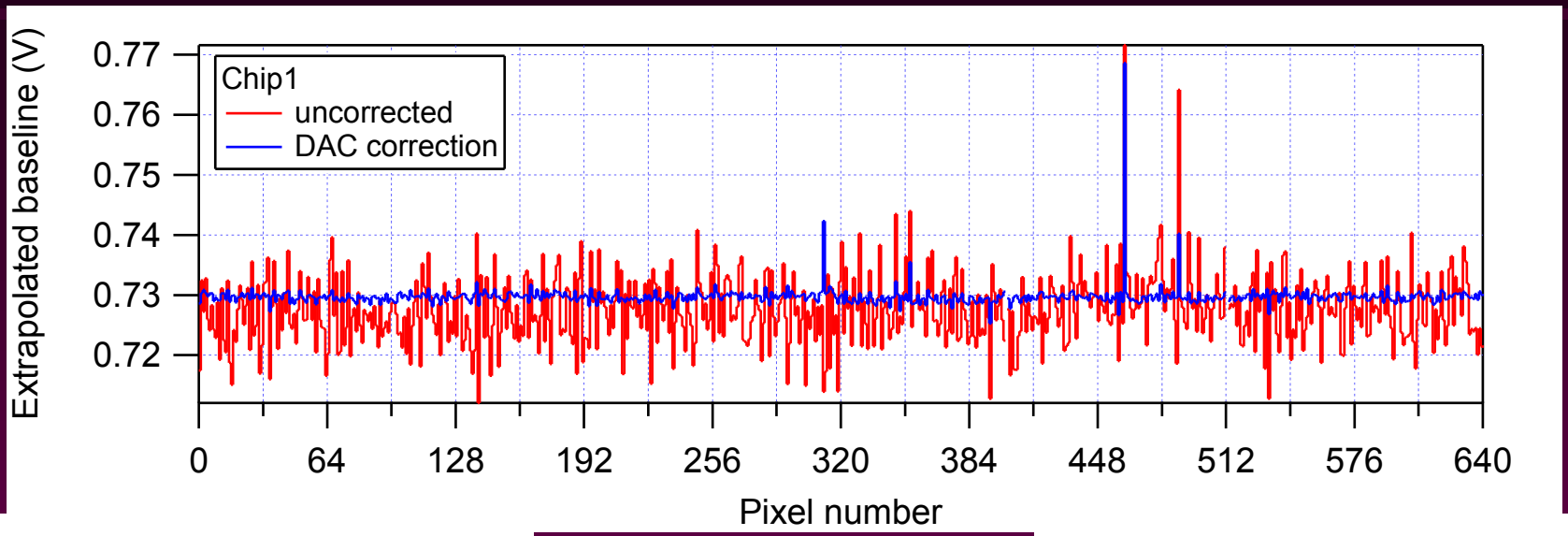
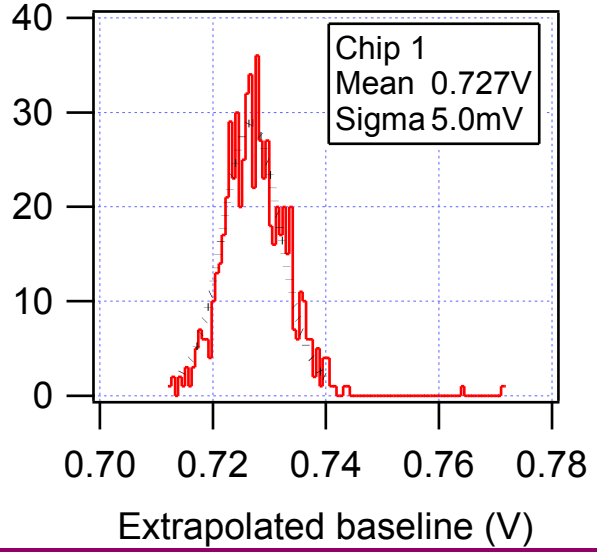
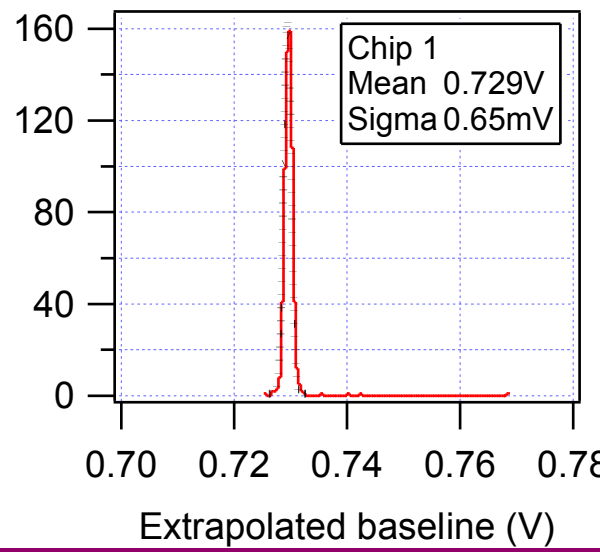
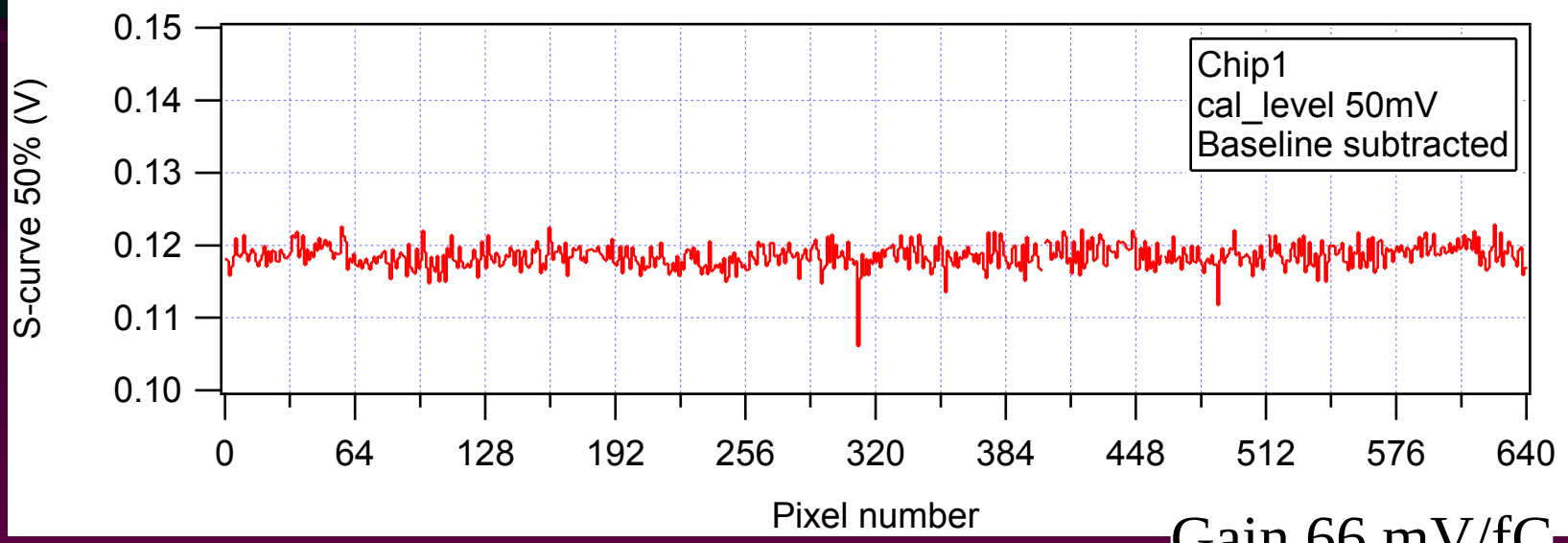




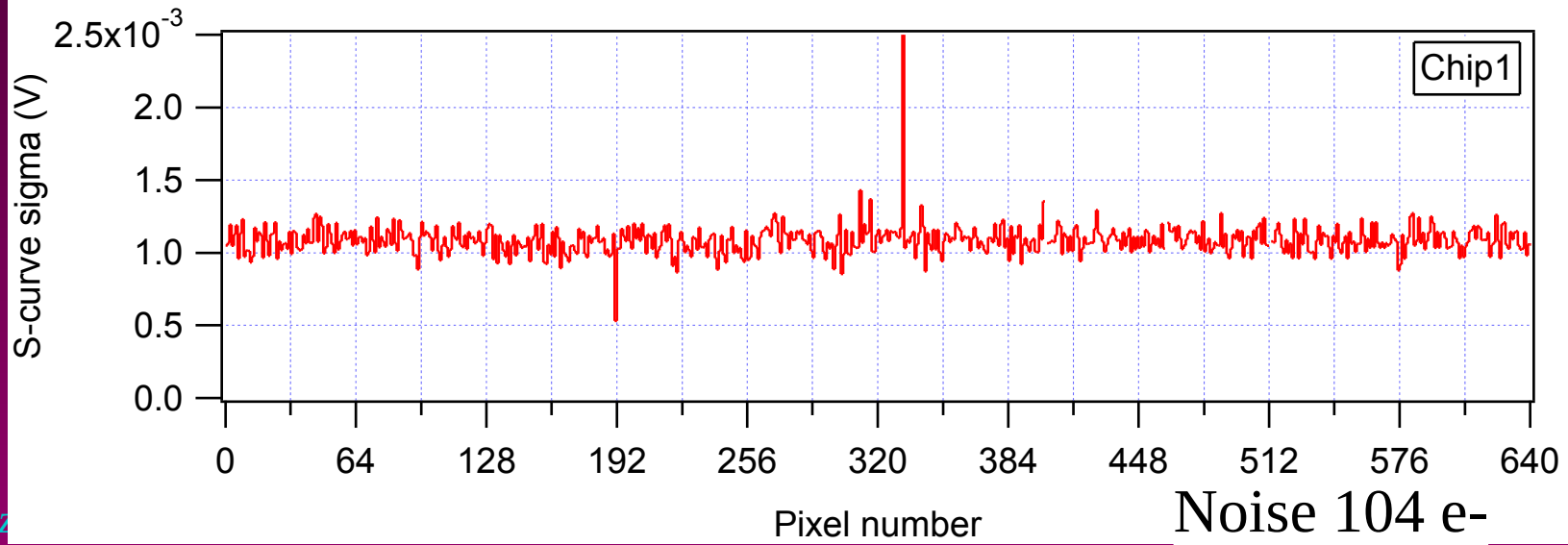
DAC correction



Gain & Noise



Gain 66 mV/fC



Noise 104 e-

GBT

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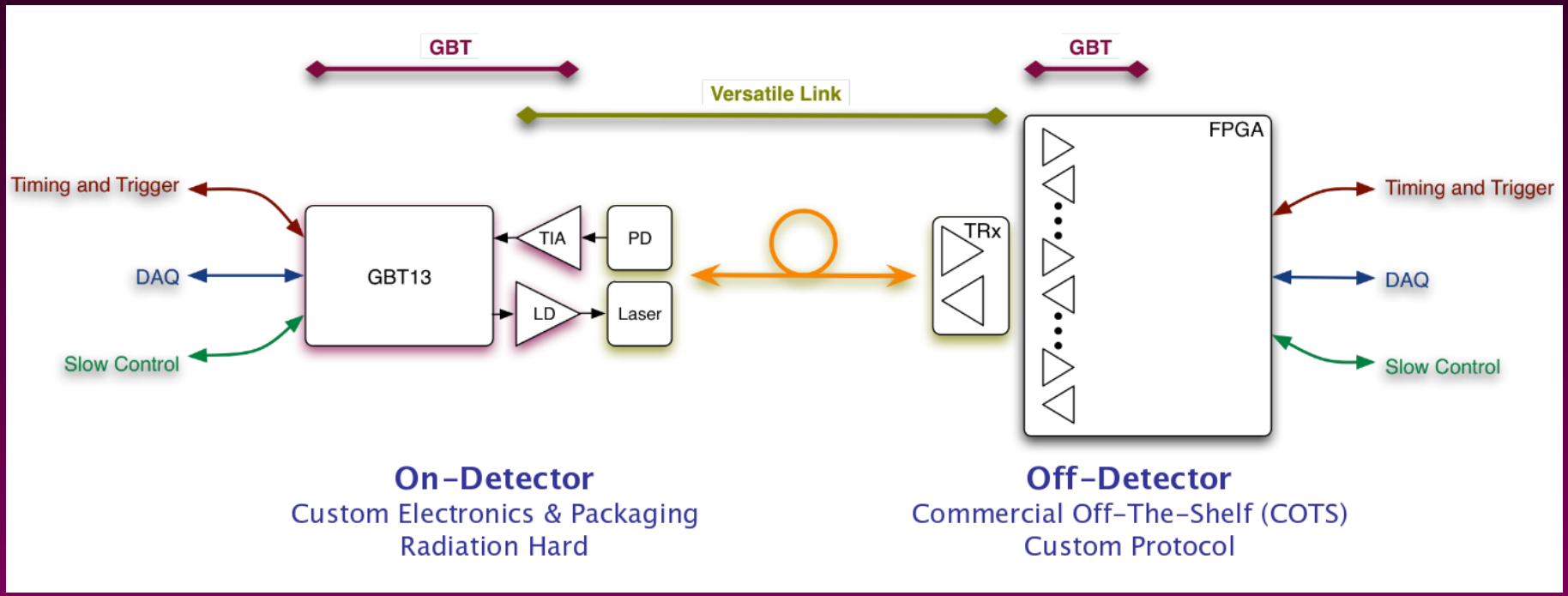

GBT chipset

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Radiation tolerant chipset :

- GBTIA : Transimpedance optical receiver
- GBLD : Laser driver
- GBTx : Data and Timing Transceiver
- GBT-SCA : Slow control ASIC

Target Applications :

- Data readout
- TTC
- Slow control and monitoring links

Supports :

- Bidirectional data transmission
- Bandwidth :
  - → Line rate : 4.8 Gb/s
  - → Effective : 3.36 Gb/s

Radiation Tolerance :

- Total dose
- Single Event Upset

Power regulator

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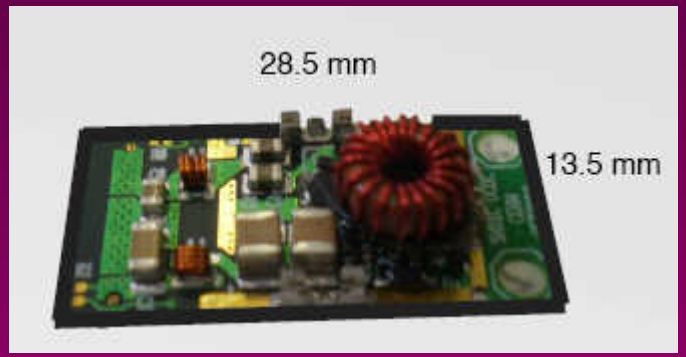
- ToPiX power supply 1.2 V – I_{DC} ~ 1 A (estimated)

  → voltage drop on cables is not negligible
- A DC-DC converter solution compatible with the radiation levels and the magnetic field of a silicon tracker is under development @ CERN for sLHC
- Current CERN version : V_{IN} 10÷12 V, V_{OUT}=1.8÷3.3 V, I_{OUT} < 3 A
- V_{OUT}= 1.5 V, I_{OUT} < 3-4 A now avail.
- Board position t.b.d.

  → *ToPiX internal regulator t.b.d.*



Conclusions

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- A pixel readout architecture has been defined – waits for more detailed rate simulations to be finalized.
- F/E ASIC with full pixel cells and columns has been designed and tested – a new prototype, with full end of column logic is currently under test.
- A GBT-based interface to the DAQ system is under evaluation. Contacts with the CERN GBT group ongoing.
- Started discussion with a CERN group for radiation tolerant DC-DC converter. Solutions based on the AMIS ASIC and commercial chips are under evaluation.

Next steps

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- Test of ToPiX v3
- Simulations of the ToPiX updated architecture with the data ← input from simulations
- ToPiX bus modeling
- ToPiX more accurate power estimation (from v3 tests) → input to cooling design
- 1st approximation definition of the data trasmission board and the power regulator board →input to mechanical design
- New aluminium cables testing with SLVS drivers

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Backup slides

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ToPiX block diagram

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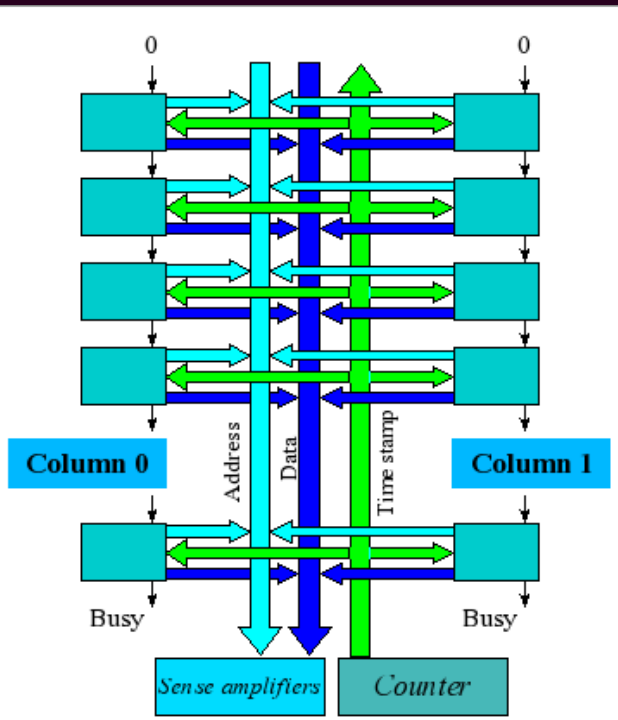

Double column structure
Common time reference
Readout data :
- Address
- Leading edge time
- Trailing edge time

End of column buffering
Serial data out

Data format

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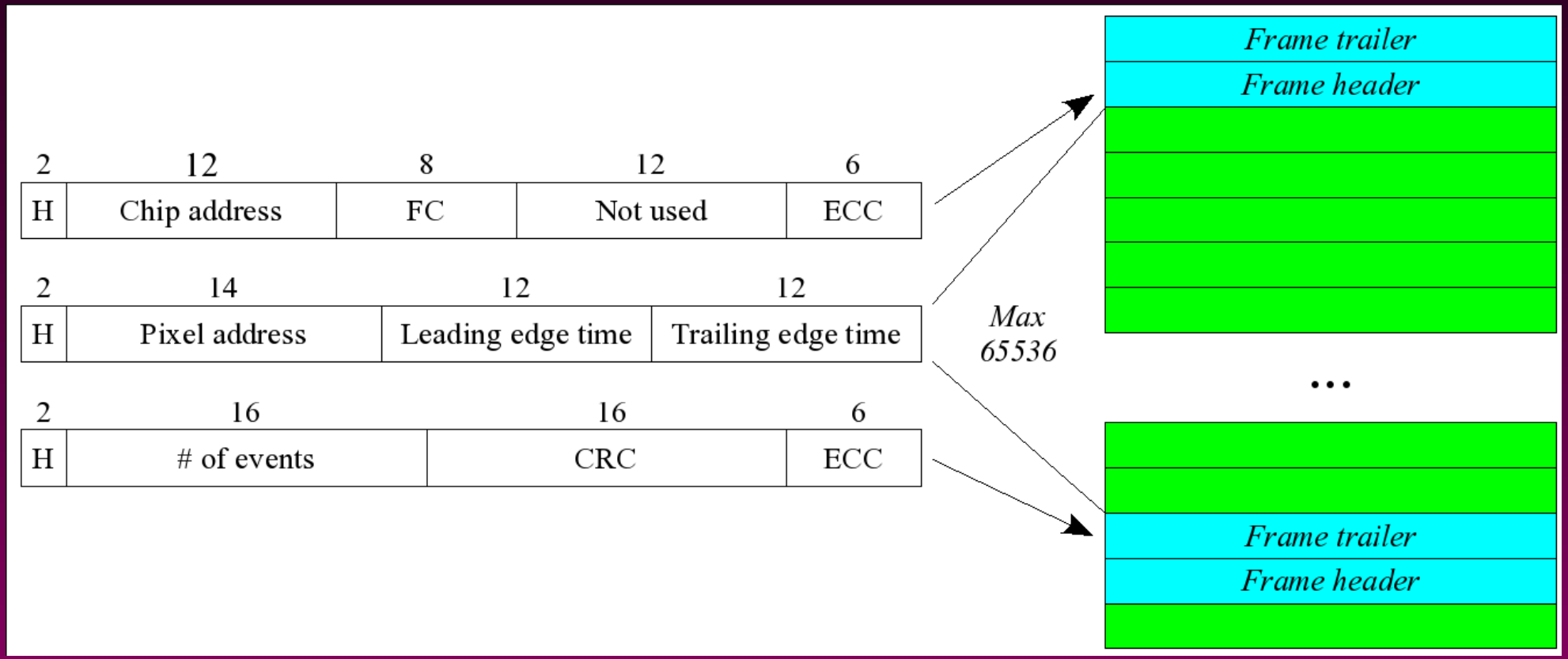

ToPiX ASIC

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- Custom development for the PANDA MVD
- Provides spatial and time coordinates plus energy resolution measurement (via ToT)
- Compatible either with p-type or n-type detectors
- Self triggered architecture
- Each event has a 12 bits time reference
- Double rate serial readout
- Radiation tolerant
- Data corresponding to a 12 bits counter cycle (26.21 μs) are packed in a frame, with an 8 bits frame counter (6.71 ms cycle)

Pixel cell

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