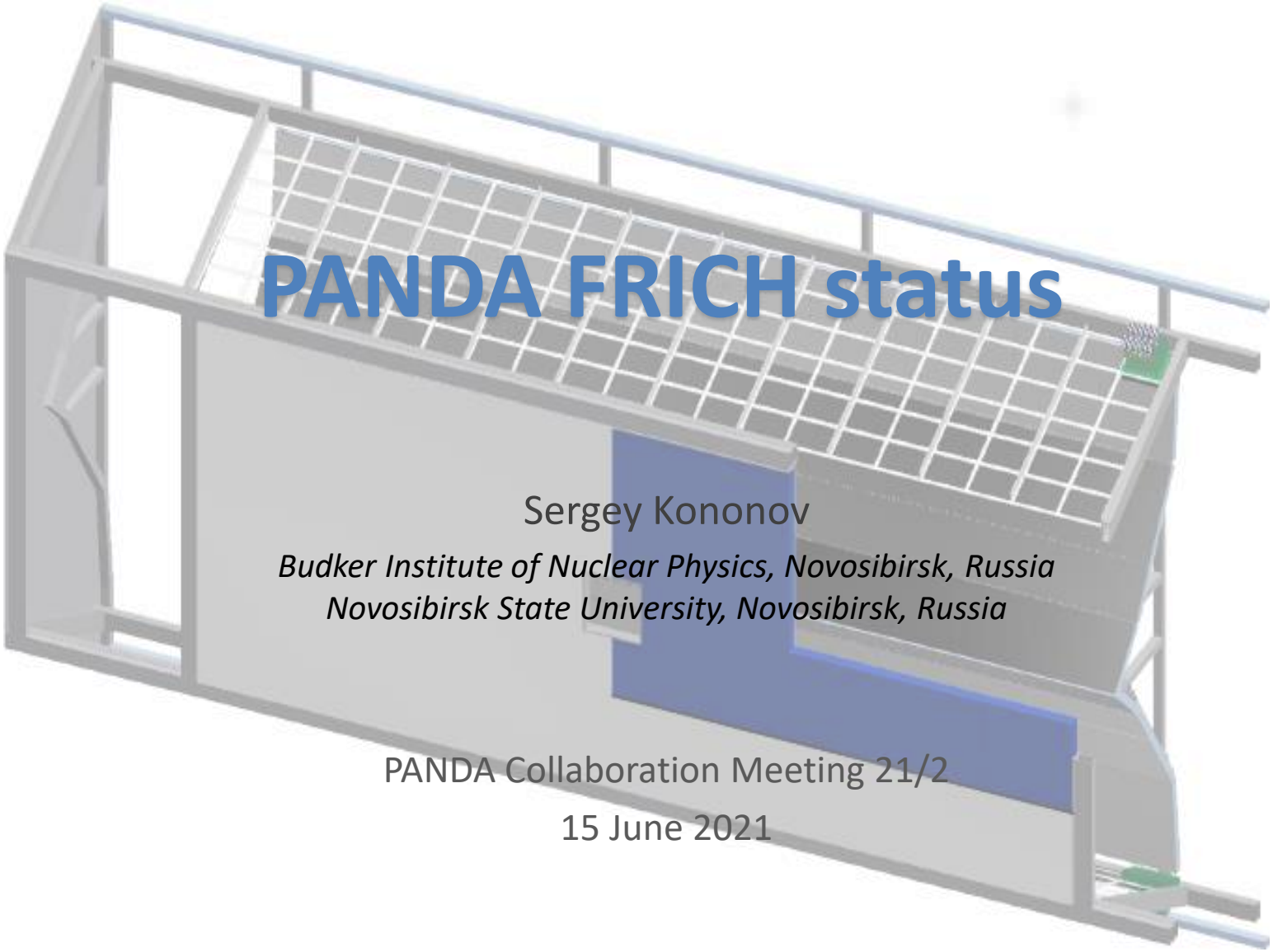

PANDA FRICH status

Sergey Kononov

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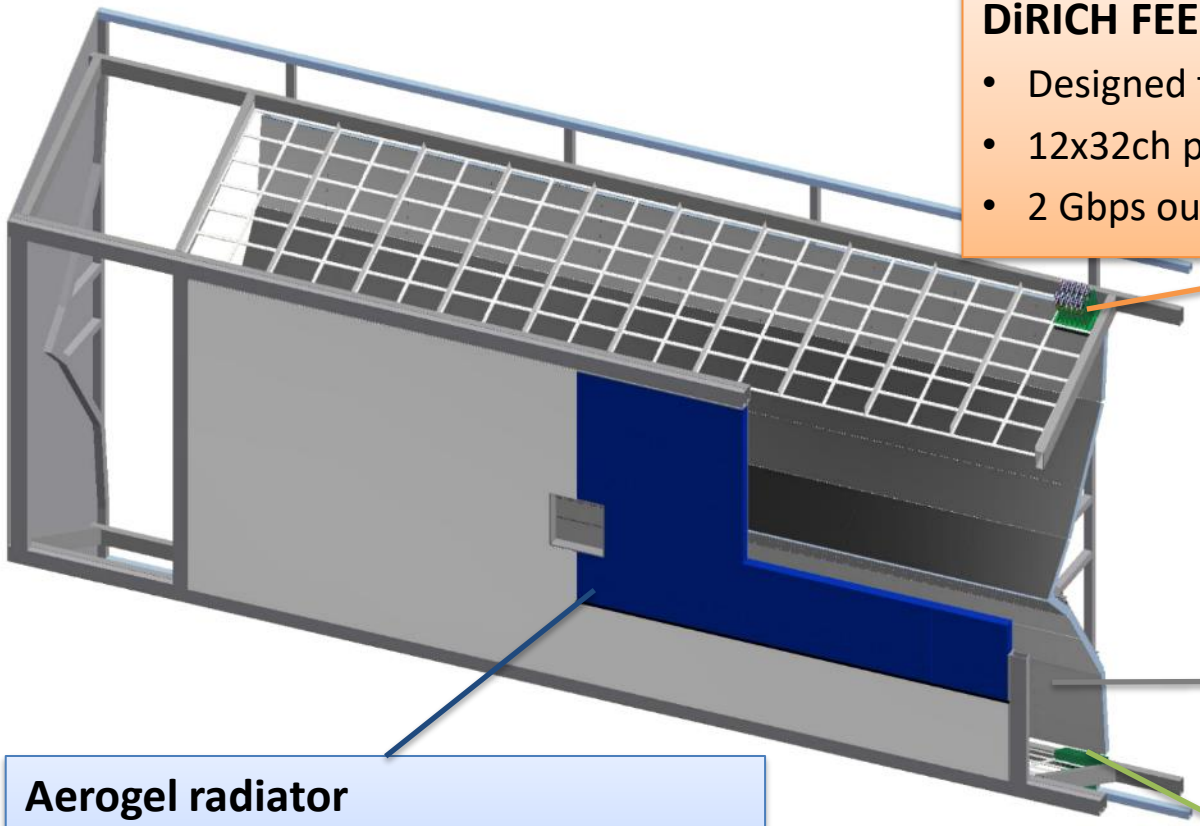
Novosibirsk State University, Novosibirsk, Russia

PANDA Collaboration Meeting 21/2

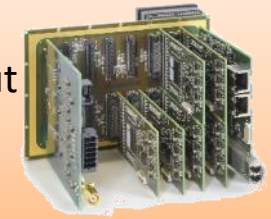
15 June 2021

FRICH baseline design



DiRICH FEE (GSI)

- Designed for H12700 readout
- 12x32ch preamp+disc+TDC
- 2 Gbps output link



Mirrors

- 2 mm float glass
- Al+SiO_2 coating

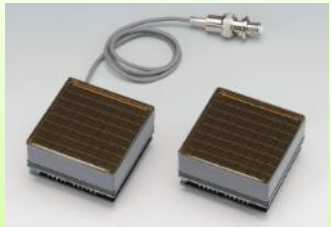
Aerogel radiator

- Focusing 2- or 3-layer aerogel
- n≈1.05
- 40 mm thick

Photon Detector

H12700 MaPMTs (Hamamatsu)

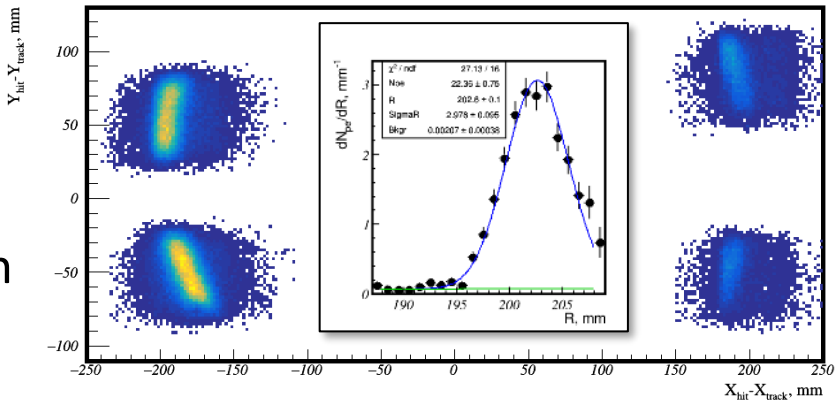
- flat panel
- 8x8 anode pixels of 6mm size



FRICH status as of February 2020

- FRICH prototype equipped with a stacked 2-layer aerogel radiator, flat mirror, 4 MaPMTs and DiRICH readout was tested with the 3 GeV electron beam at BINP in June 2019
- Test beam results including single photon resolution, number of photoelectrons have been obtained. In spite of worse than expected SPR and Np.e. evaluated π/K separation power at P=10 GeV/c (3.4σ) is good enough.

Cherenkov ring from 2019 test beam



- Main components of FRICH were described in the mechanical design
- Detector integration steps were described
- LV&HV system is to be designed
- Construction plans and cost estimation are to be updated
- TDR is to be written by mid-2020

Status of FRICH R&D as of June 2021

- Main R&D from FRRC funding finished in 2017
- Small NSU funding stopped in 2020
- An application to RFBR in 2015 fund was unsuccessful. New applications seem to be pointless.
- No active developers on the project since beginning of 2020
- No active work on FRICH TDR
- But some other FARICH R&D is ongoing at BINP mostly connected to the Super Charm-Tau Factory

Event reconstruction using Neural Networks

Motivation

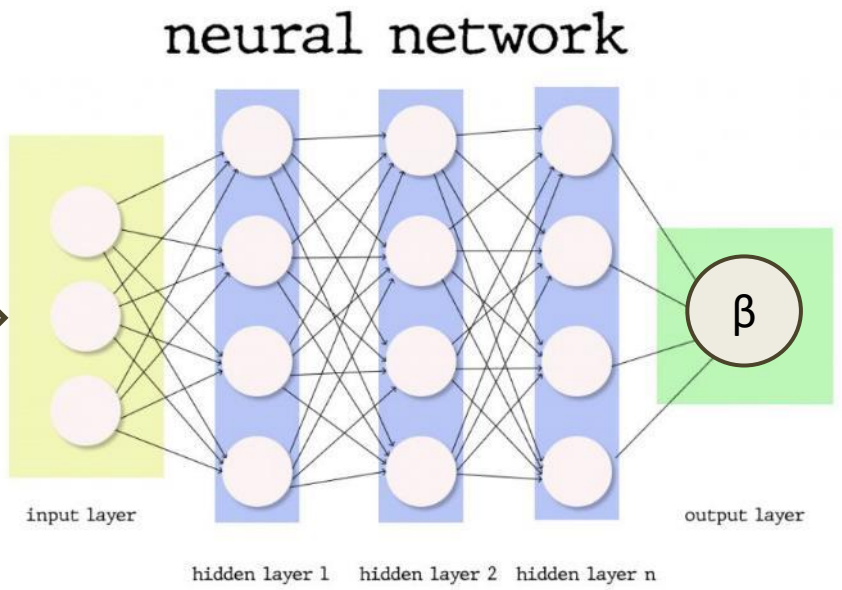
- Alternating approach to event reconstruction with a potential to include all observed data without knowing PDFs → flexibility
- More straightforward and attractive for developer

Implementation (started in Fall 2020)

- Python with Pandas, TensorFlow etc. packages
- Geometrical reconstruction of hit θ_c, φ_c, then NN training
- Obtain particle's β from a single NN output

N_{hits} (i, j, k)
i – bin on ϕ_c
j – bin on θ_c
k – bin on time

particle inc. angle



SCTF FARICH simulated configuration

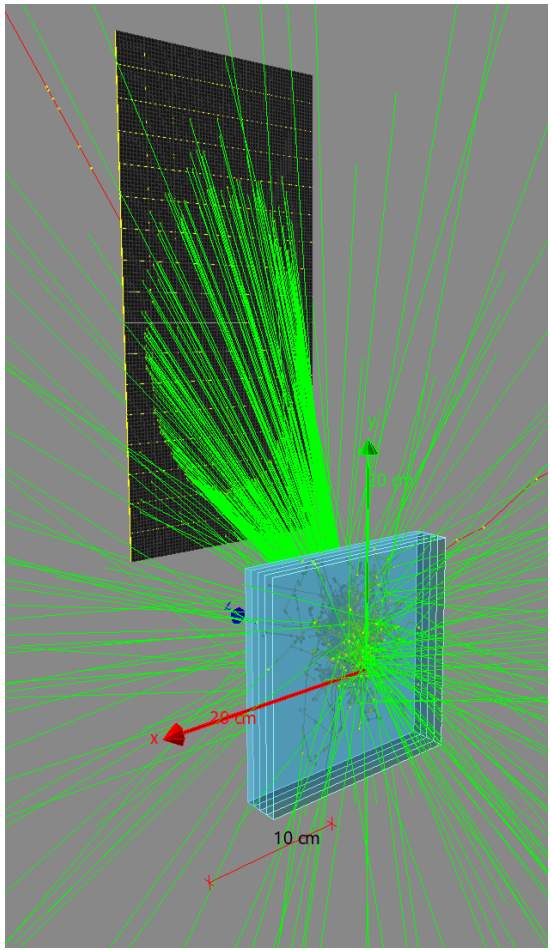
Photon detector

- ON Semiconductor (SensL) ArrayJ-30020-64P-PCB
- Pixel size 3.16×3.16 mm^2
- Pixel pitch 3.36 mm
- U_{bias} = 2.5V
- λ_{max}≈400 nm, PDE_{max}≈ 38%
- Sensor geom. fill factor ≈ 88%

Radiator

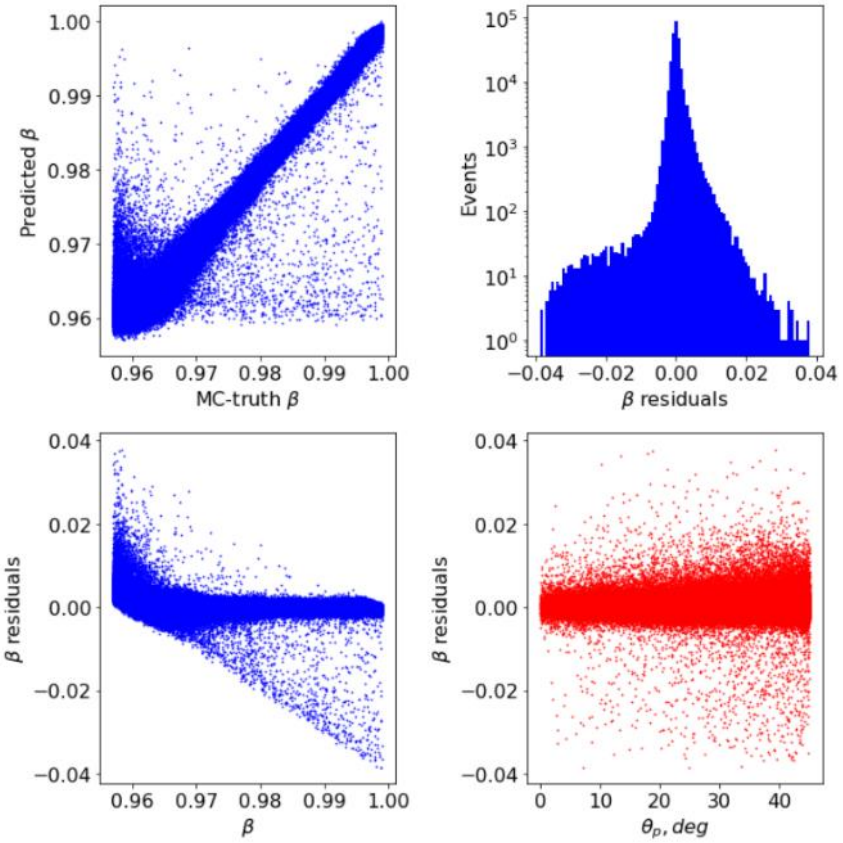
- 4-layer focusing aerogel
- n_{max} = 1.05
- 35 mm thickness

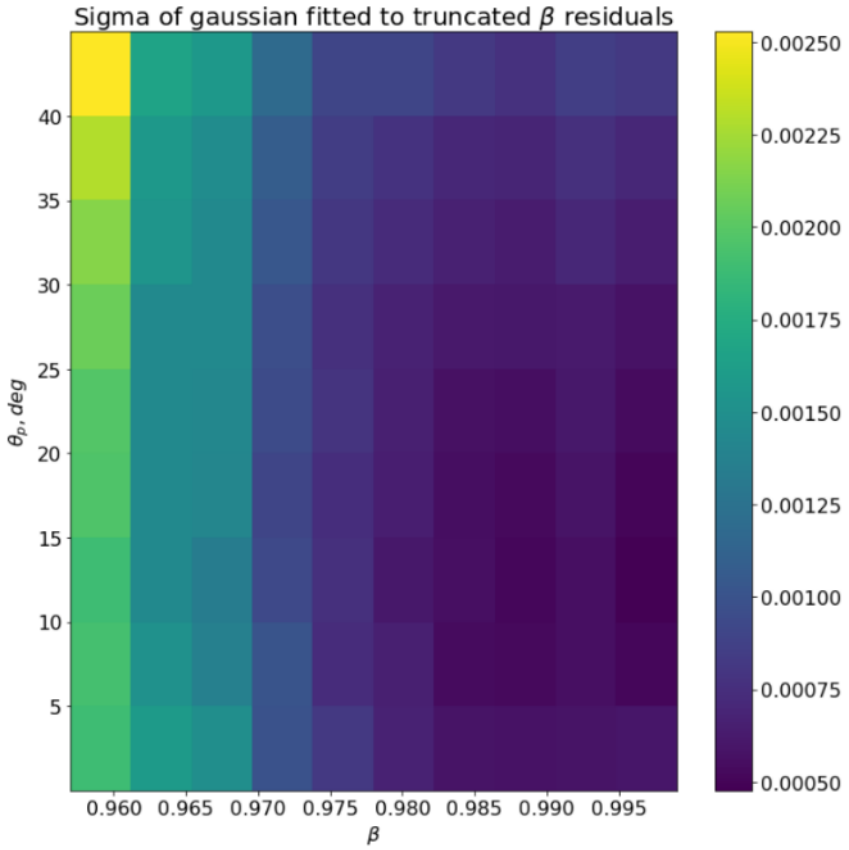
PD-Radiator distance: 200 mm



Results of NN event reconstruction

Scatter plots for β residuals

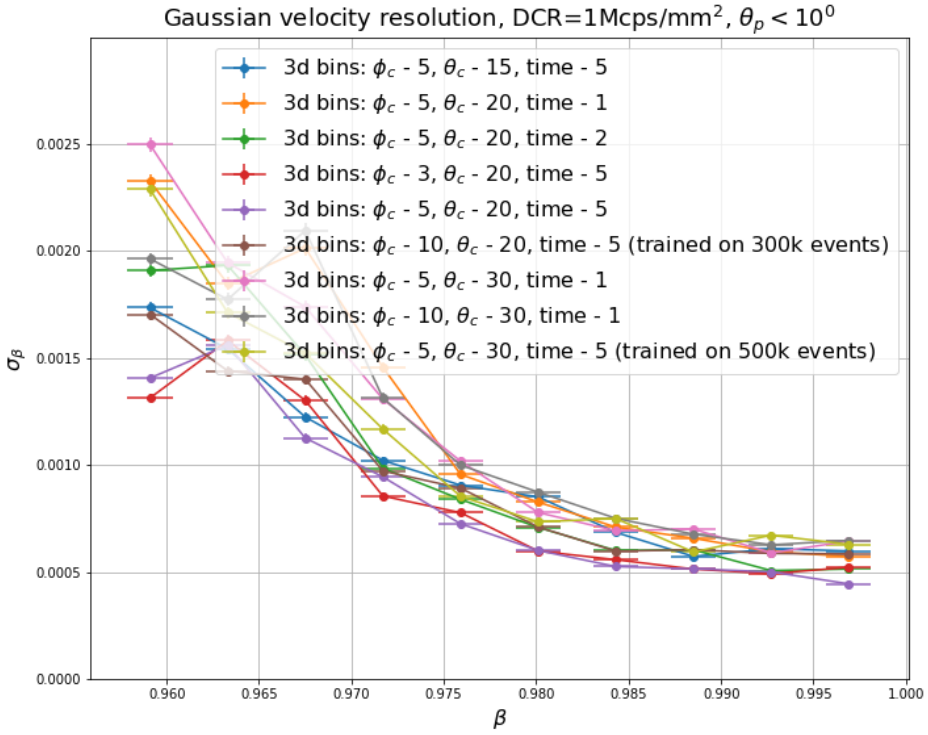




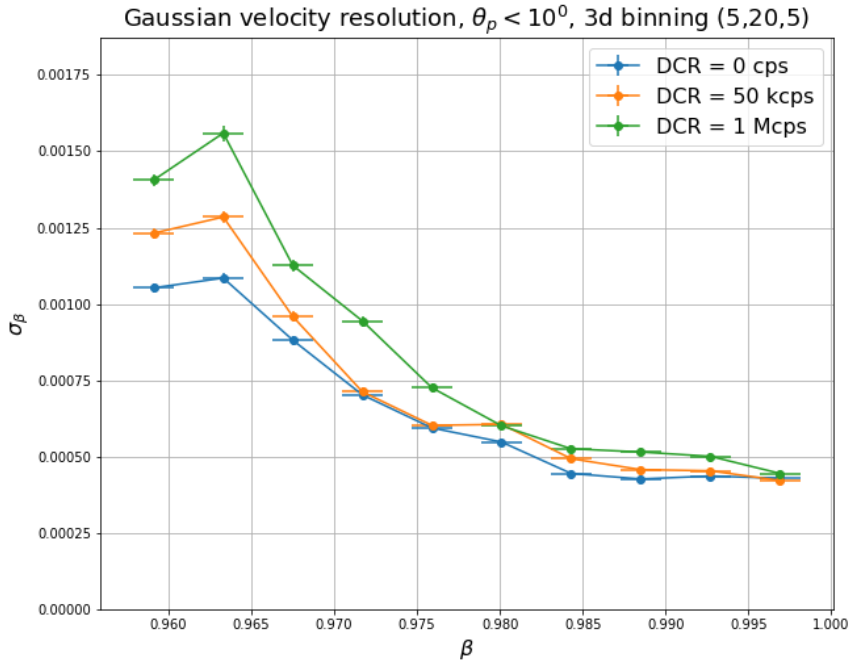
≥ $5 \cdot 10^{-4}$ β resolution for 1 Mcps/mm^2 dark count rate

NN performance

Different binning of hits



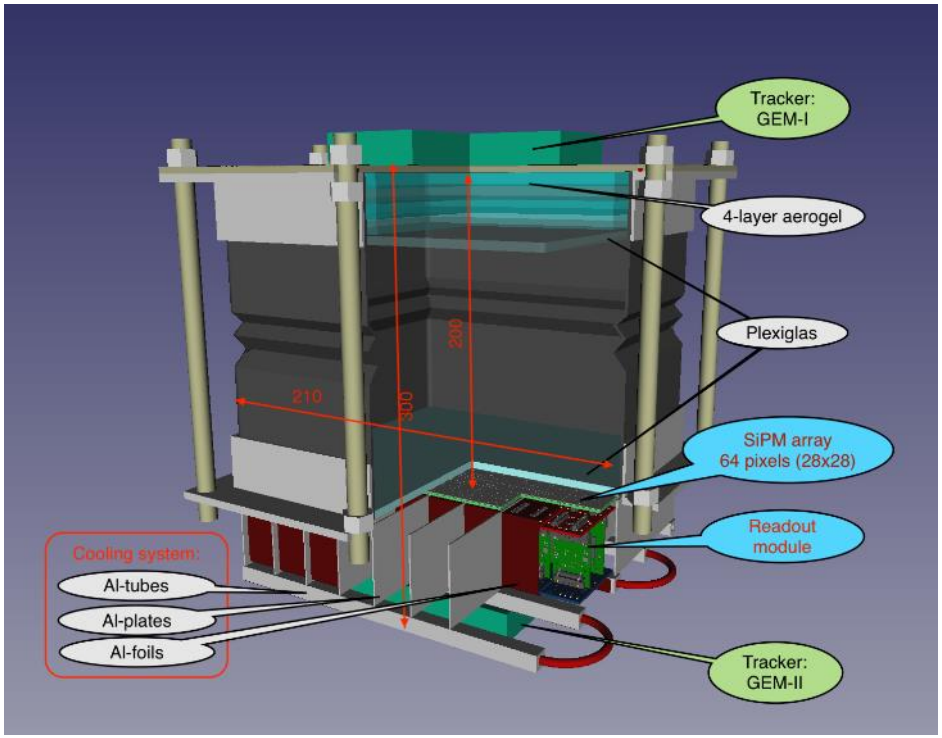
Dependance on DCR



Full-scale FARICH prototype with SiPMs

Full-scale prototype will detect full Cherenkov rings with SiPM arrays & compact readout FEE.

- photon detector size ≈21×21 cm^2
- 64 × (8×8) = 4096 pixels of 3×3 mm^2
- aerogels up to 20×20 cm^2 size
- aerogel isolated from environment
- folding envelope enabling focal distance adjustments
- liquid cooling system to operate at −30°C (≤ 5%X_0)



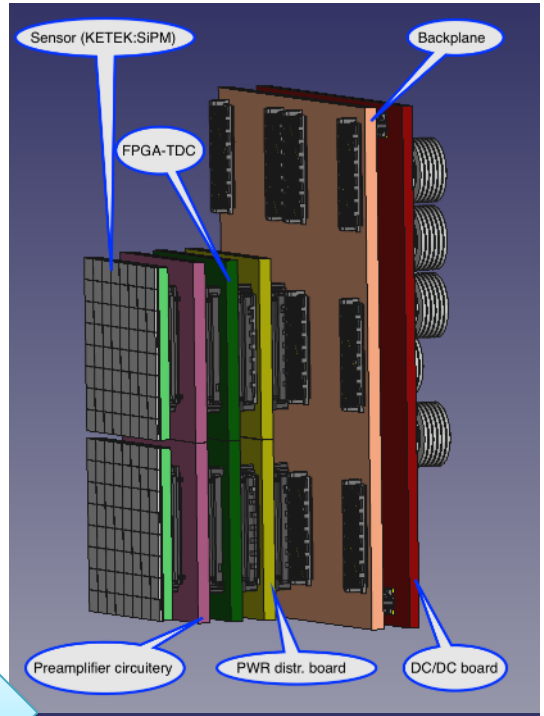
Full-scale prototype should be ready for test beam in 2022

R&D of front-end electronics for FARICH with SiPM readout

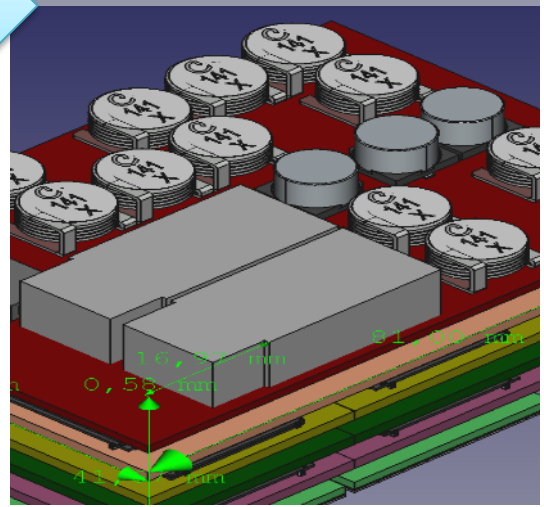
Objectives:

- High-density electronics with footprint of 3.4x3.4 mm per channel
- Fit SiPMs + FEE into ~5 cm radial space in barrel
- Power consumption as low as possible with a goal of 10-20 mW/ch
- TDC with ~100 ps timing resolution & coarse amplitude measurement (ToT)
- Possibility to cool down to −40°C

Very challenging project!



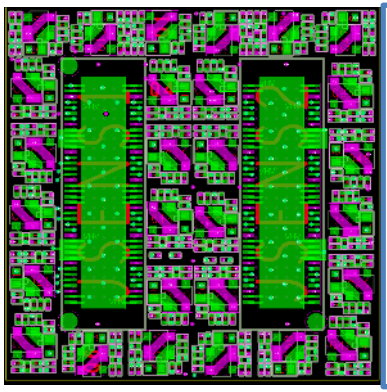
FARICH FEE module for 3x2 KETEK SiPM arrays



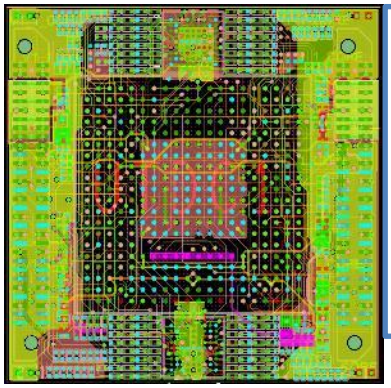
Status & plans:

- R&D has been started by GSI digital electronics group (M. Traxler) in 2020
- Concept: FPGA-based TDC (TRB3 platform)
- Layouts of 3 of 5 boards are ready
- Production will start in Spring 2021

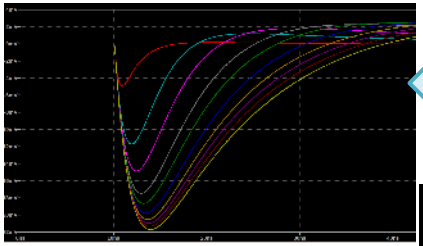
First version of FEE board layouts



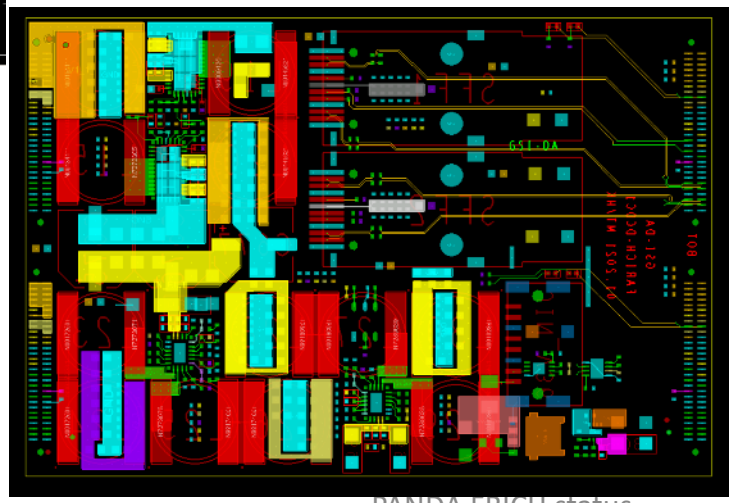
Amplifier board
- 27×27 mm^2 size
- 14-layer PCB
- 30x gain, 64 channels
- couples to KETEK 8×8 SiPM array



TDC board
- 64 channels
- 2 TDC + 4 threshold FPGAs
- 10ps precision

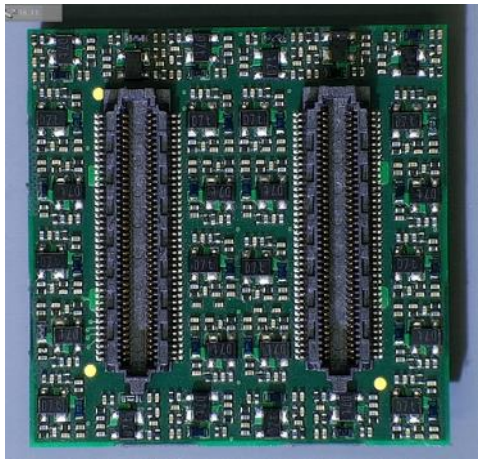


Simulated single photon pulse shapes from amplifier for different input resistance. ~ 22mV amplitude can be achieved.



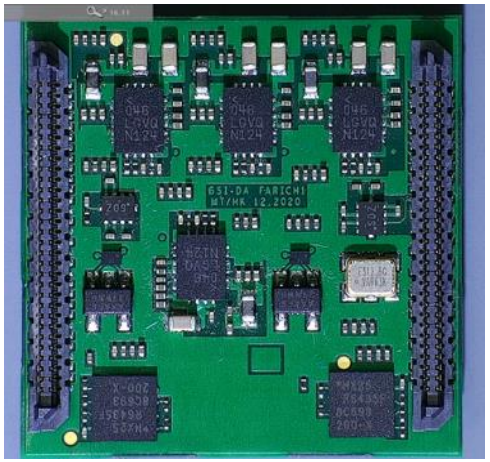
DC-DC convertor board
- goes behind the backplane
- 51×84 mm^2 size
- provides power to SiPMs, amplifiers, FPGA
- uses air inductive coils to operate in the detector magnetic field
- power, trigger & clock connectors

Preamp. board

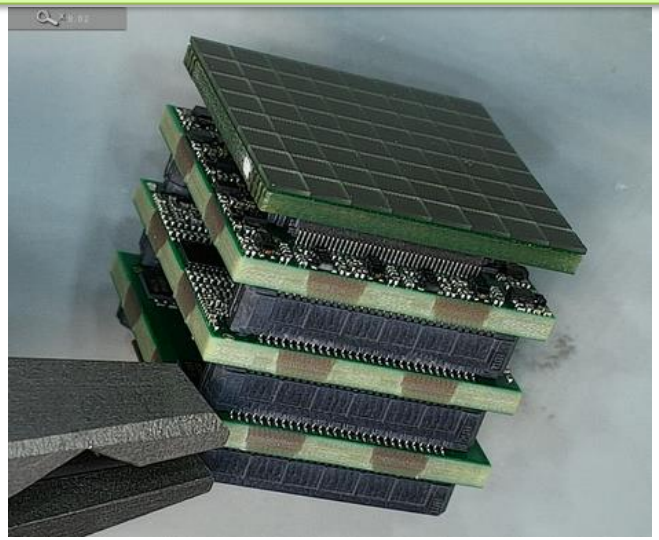


TDC board

Power dist. board



KETEK 64-ch. array & electronics assembly



Full FEE assembly for 6 arrays (384 channels)