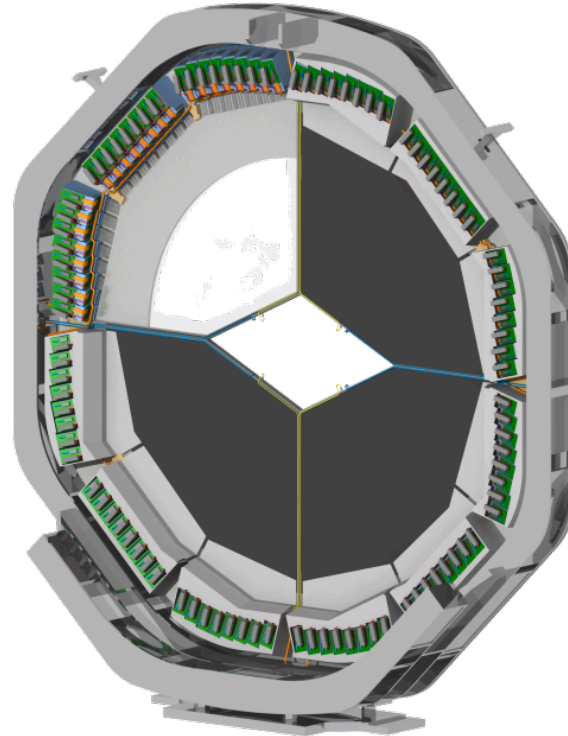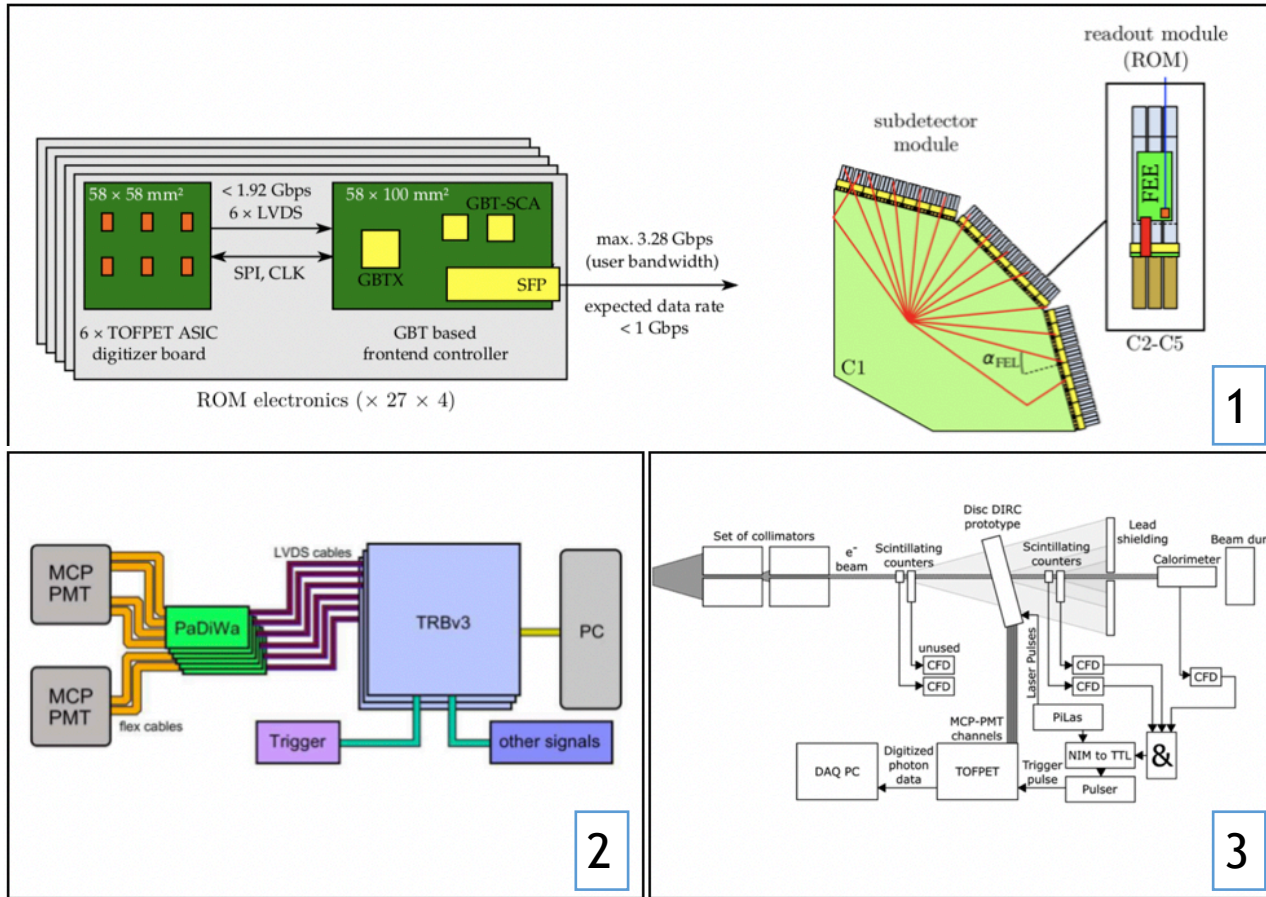# The EDD Frontend Electronics Update

Simon Bodenschatz, Lisa Brück, Michael Düren, Avetik Hayrapetyan, Jan Hofmann,

Sophie Kegel, İlknur Köseoğlu-Sari, Jhonatan Pereira de Lira, Mustafa Schmidt, Marc

Strickert, Leonard Welde, Chris Takatsch

PANDA Collaboration Meeting 21/2 - 2021/06/15

- The readout system was used in 2015 testbeam at CERN (2). TRBv3 boards with PadiWA
- First time it is suggested to use TOFPET system (1).
- First TOFPET system was used in 2016 testbed at DESY (3).
- TOFPET2 was used during testbeam 2018.

ToFPET 2 PETsys

Analog signal (MCP-PMT)

↓

Digitized signal (FEM)
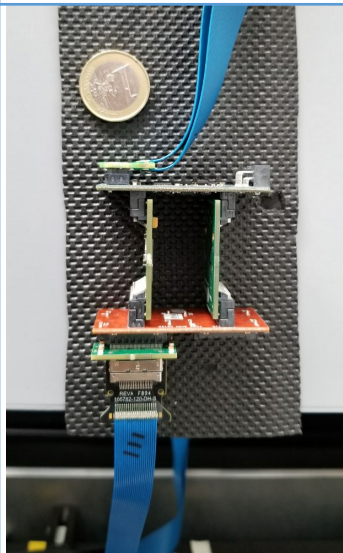
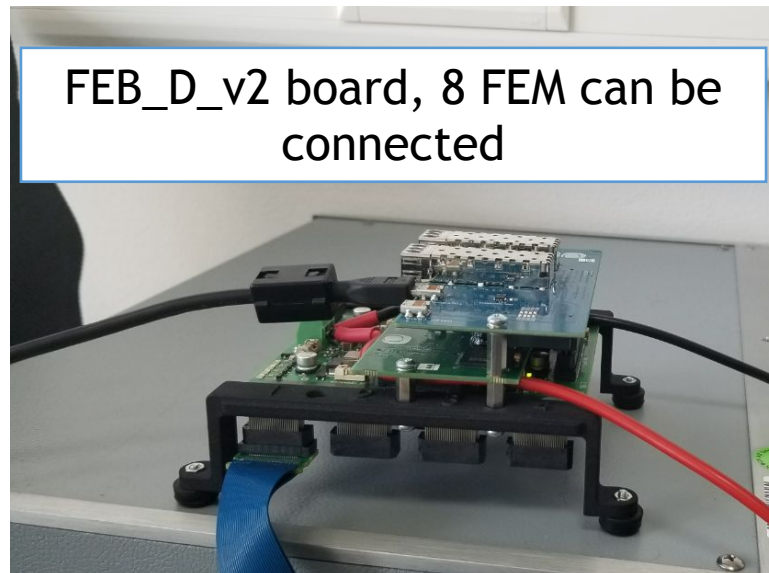↓

FEB_D_v2 (FPGA)

↓

Fan-out box

↓

DAQ board

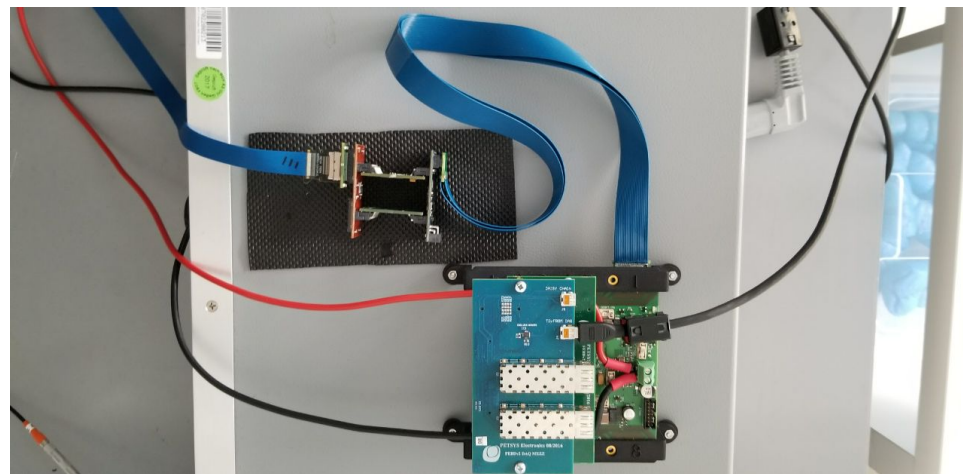System clock (200MHz) Synchronization signals

Max data rate 250 Mevents/s

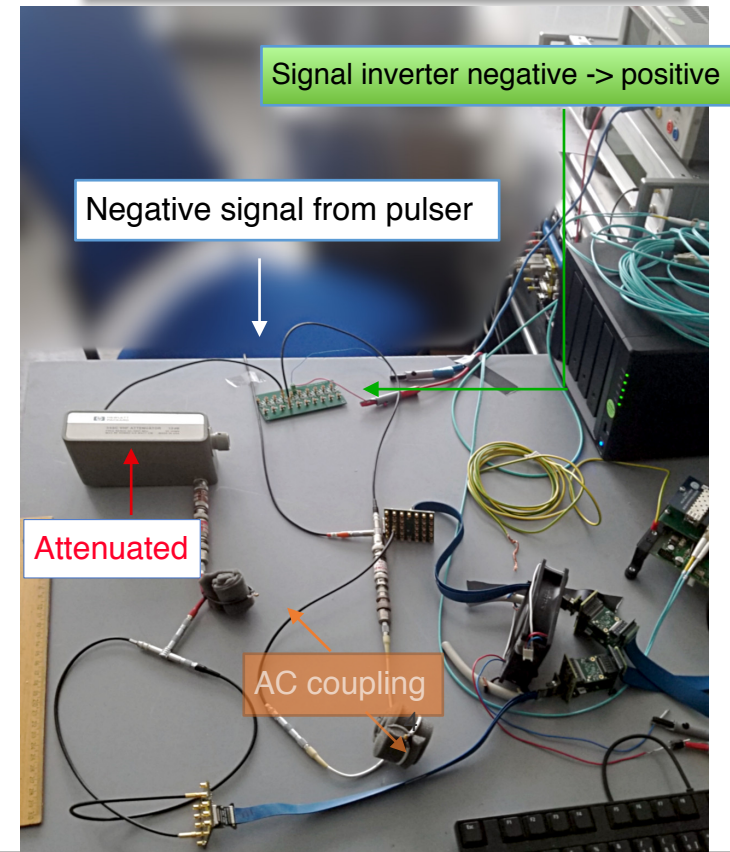FEM with 2 ASICs,128 ch

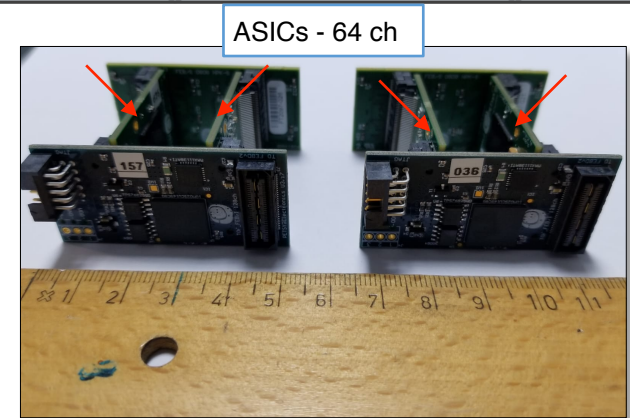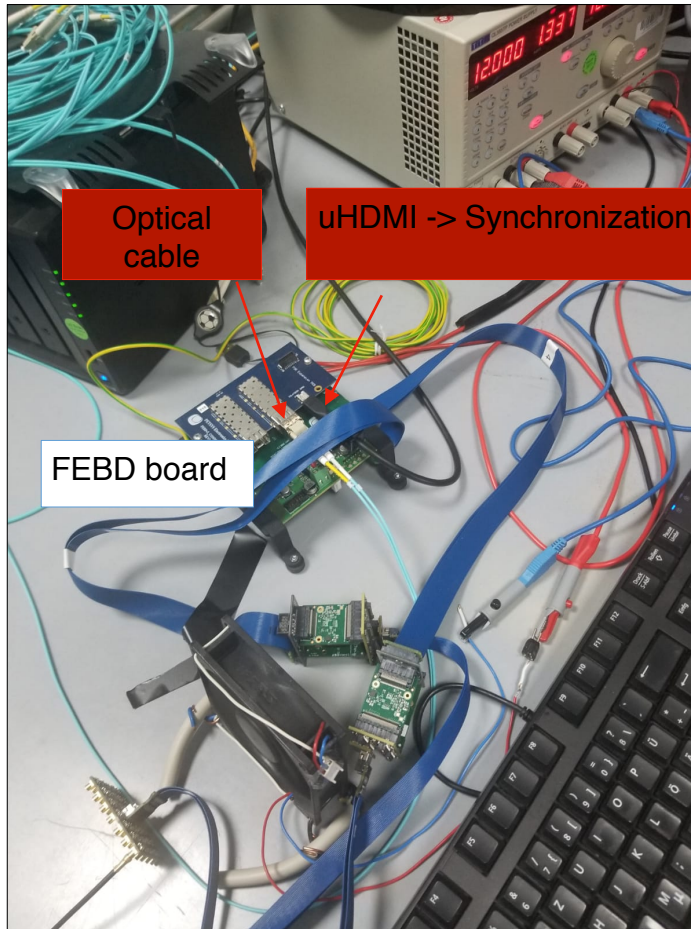
FEB_D_v2 board, 8 FEM can be connected

Test beam 2018
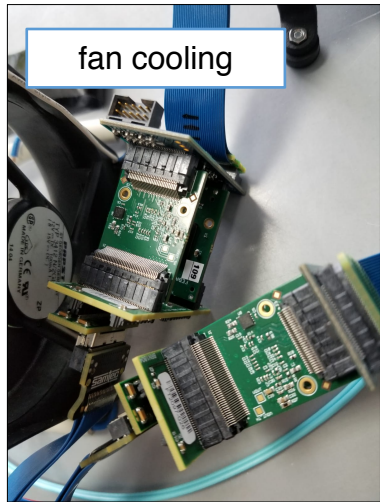
✗ Negative polarity

✓ Positive polarity

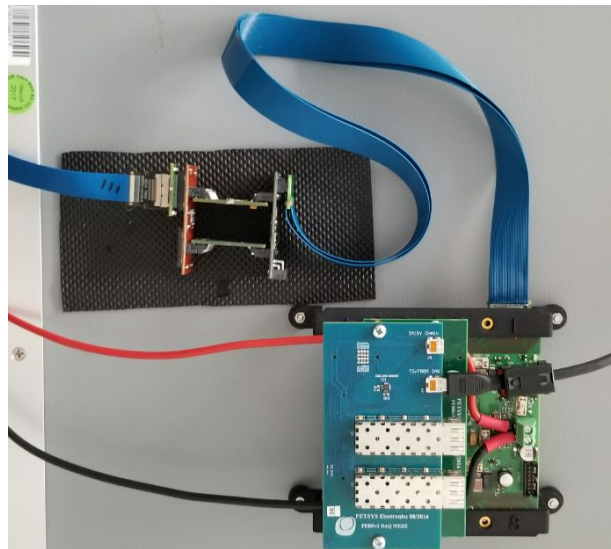# The 2020 batch of ASICs - test measurements

- Positive Signal ~ 40mV

- Negative Signal ~ 40mV, pW 3.5ns

- Compatible to work with both polarities

- Convincing results from GCS data analysis

ASICs - 64 ch

fan cooling

Optical cable

uHDMI -> Synchronization

FEBD board

Signal inverter negative -> positive

Negative signal from pulser

Attenuated

AC coupling

FPGA board + ASIC board

Excluding SiPM electronics

Implementing MCP-PMT

Custom-design PCB

PCB 1: Adapter Board

MCP-PMT

PCB 2: ASIC Board

Analog Signals

Analog Signals

HV Input

Routing and 3 Connectors (total 300 Pins)

5 ASICS, 320 ch. (3 Connectors) TOFPET V2

Flex PCB

Digital signals & Power Lines & Control Lines

PCB 3: FPGA Board

Low Voltage Input

Data output link Synchronization signals
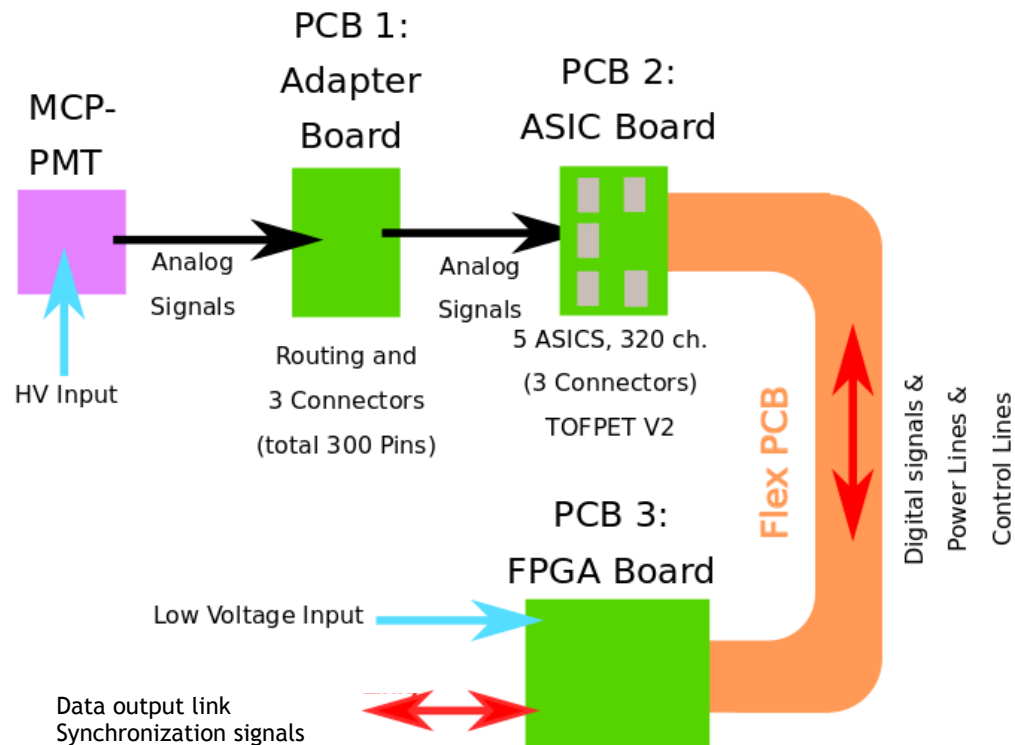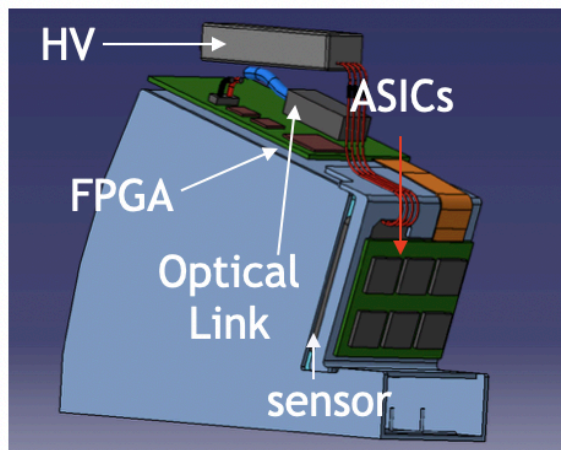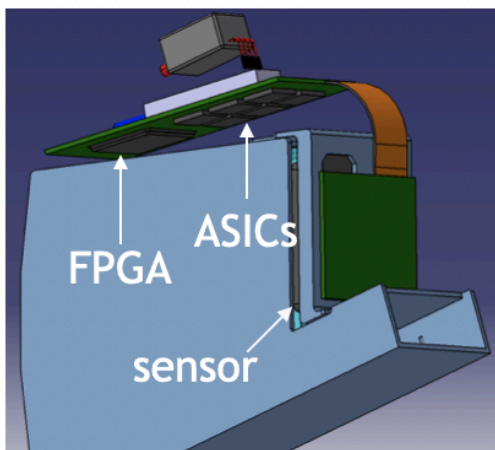
- Optical link -> VTRX+ link (radiation hard and magnetic field resistant)
- DC-DC converters -> FEASTMP modules
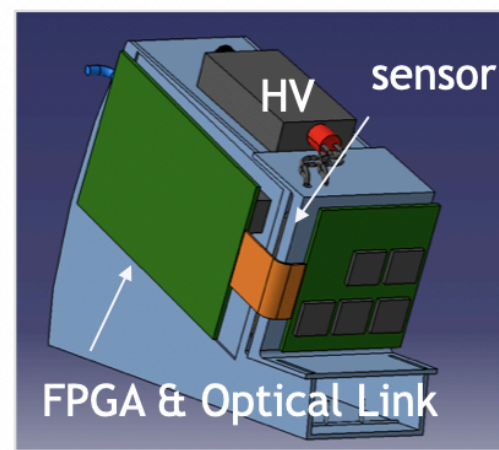- uHDMI cable -> synchronization purposes

- 6 ASICs
- ASICs are at the shortest distance to the analog signals.
- The elements are distributed considering the heat generation.

- 6 ASICs
- ASICs and FPGA are positioned on the same rigid board.
- Disadvantage: analog signals had to reach the second board for digitization.
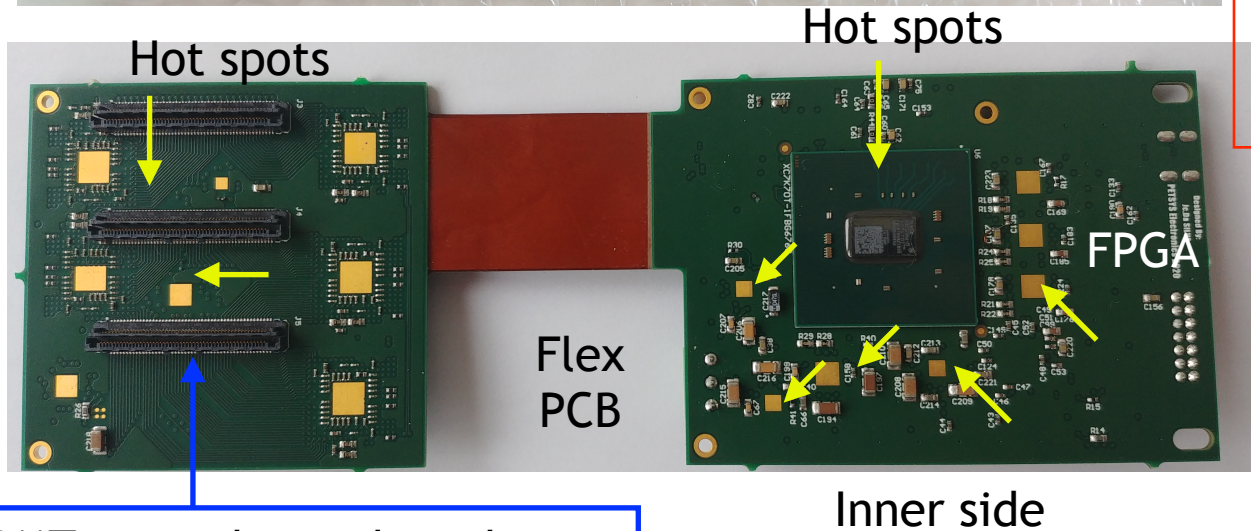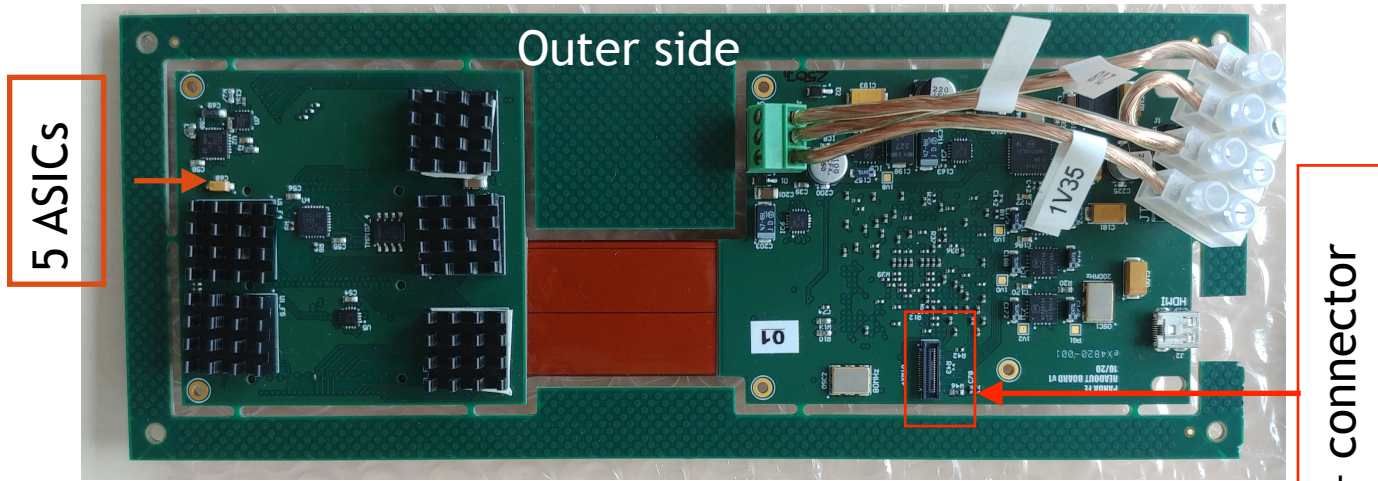- Disadvantage: Heat generation in a compact area.

- 5 ASICs
- Similar as in scenario-1.
- Due to the limited space in z-direction, alignment can be done to the side of the ROM.
- Disadvantage: 6 ROMs/side.

Custom-design PCB

- The custom-design PCB has been delivered 2 weeks ago.
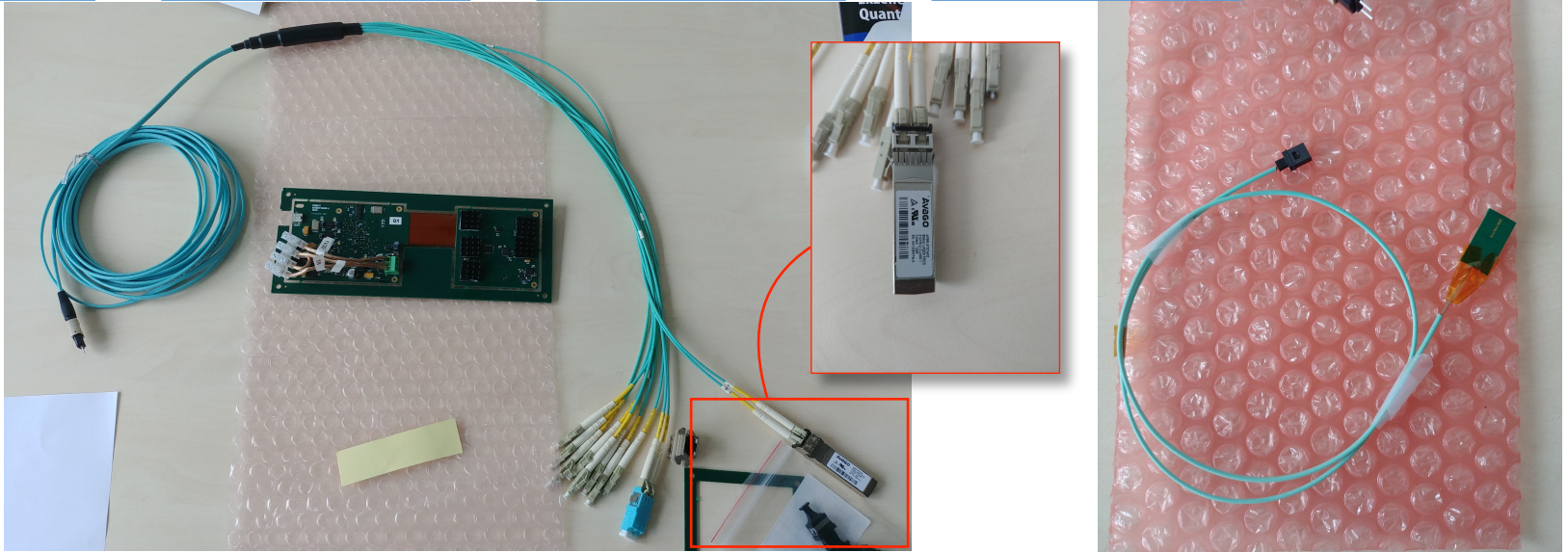- Several tests were planned.

FEASTMP modules

5 ASICs

Outer side

VTRX+ connector

Hot spots

Hot spots

FPGA

Flex
PCB

Inner side

MCP-PMT pins adaptor board

| VTRX+ pigtail Ferrule plugs | Bulkhead adaptor | MPO cable | SFP+ connection |

VTRX+

Plans with custom-design PCB

In order to test custom PCB, second DAQ board and fan-out-box (synchronization) are required. The current system is reserved for the GCS.

1. Testing the custom PCB with MCP-PMT, inside the magnet box without magnets. The laser will be focused on each pixel.

   - MCP-PMT will be provided by Erlangen group.

   - Magnetic field was measured for different distances, see Leonard's talk.

2. Same tests will be repeated with magnets. Magnet box allows changing the angle of the MCP-PMT with respect to the magnetic field.

3. Custom-design PCB together with MCP-PMT will be integrated into GCS. This requires a different cooling system -> Lisa's talk.
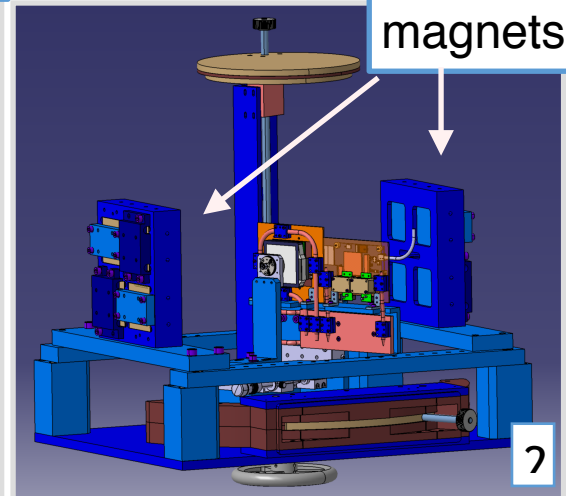
- The light-tightness was tested. It is not perfectly light-tight still some photons enter the box.

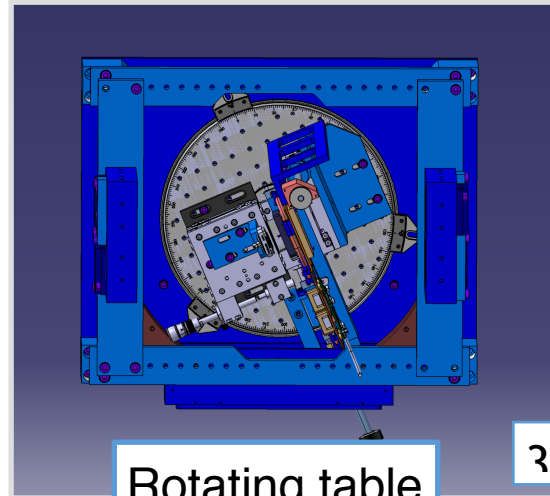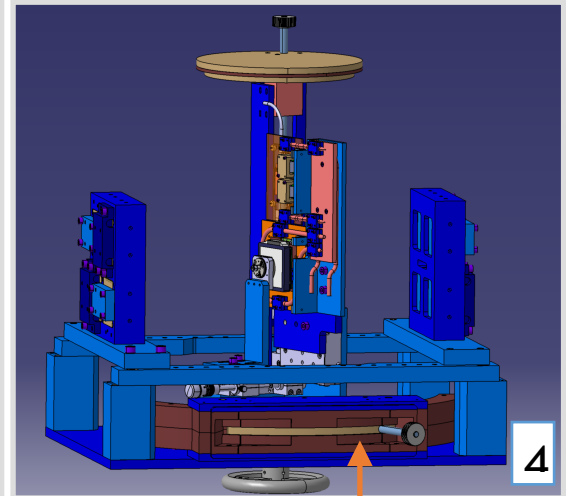- Dark count measurements are ongoing with Hamamatsu.
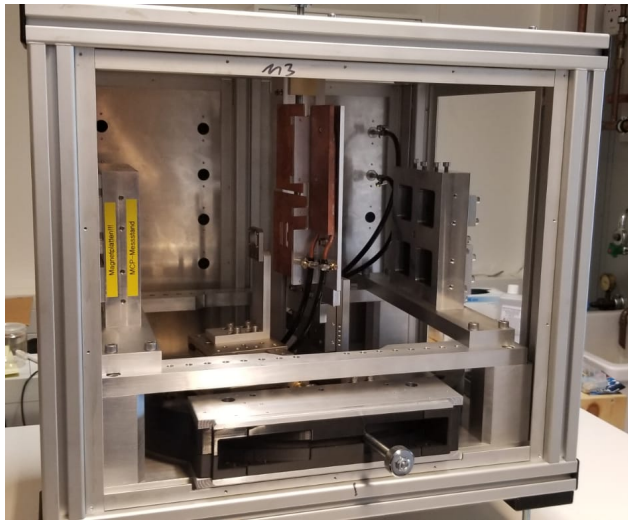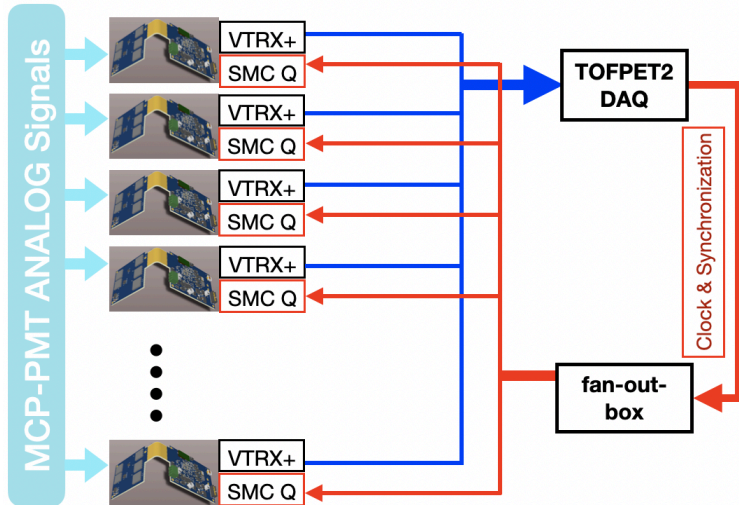

Light-tight box
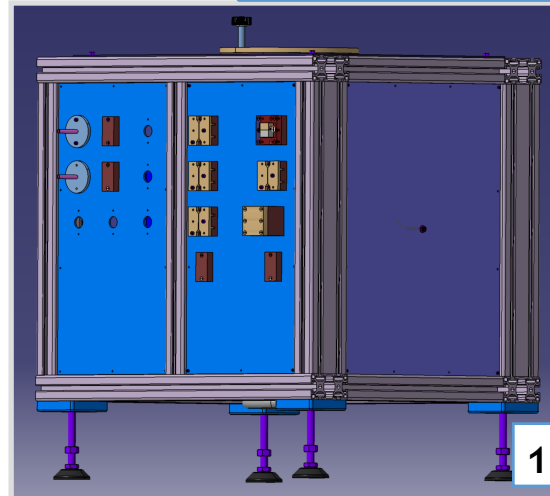
magnets

Rotating table

Wheel

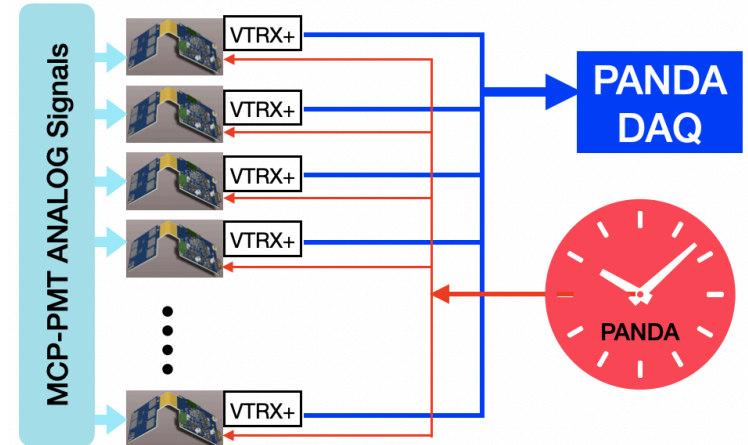$0° - 24°$

Project phases

Phase-I

- 16 ROMs are planned to be used.

- Existing DAQ system (TOFPET2 DAQ) will be used for data taking, clock & synchronization

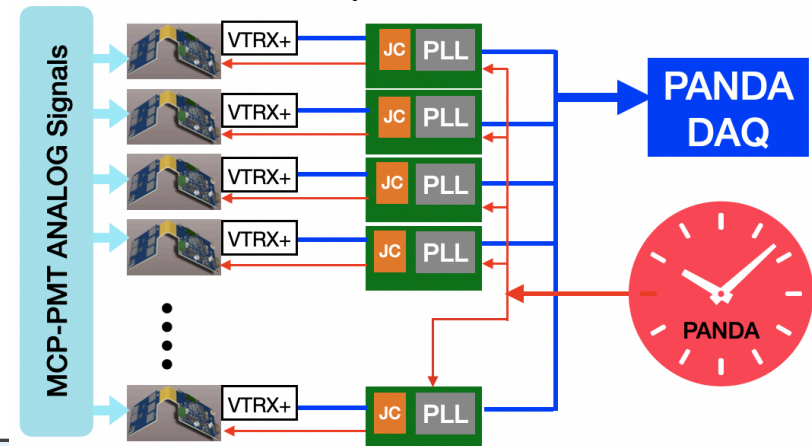- Optical link (VTRX+)-> data transmission.

Phase-II

Scenario-1: All control signals are received via optical cable

or

Scenario-2: If Clock & Synchronization signals are transmitted as hardware signals

- Reformatting outgoing data into the SODANET format
- Receive SODANET clock & synchronization commands

Conclusion

- TOFPET-2016 was compatible to work with both signal polarities.

- TOFPET2-2018 was compatible to negative signals.

- TOFPET2-2020 is compatible to work with both signal polarizations.

- TOFPET2-2020 ASICs are integrated to the GCS and convincing results were obtained.

- Custom-design PCB has arrived!

- The tests are planned for the custom design PCB with or without magnetic field.

- Thanks for your attention!