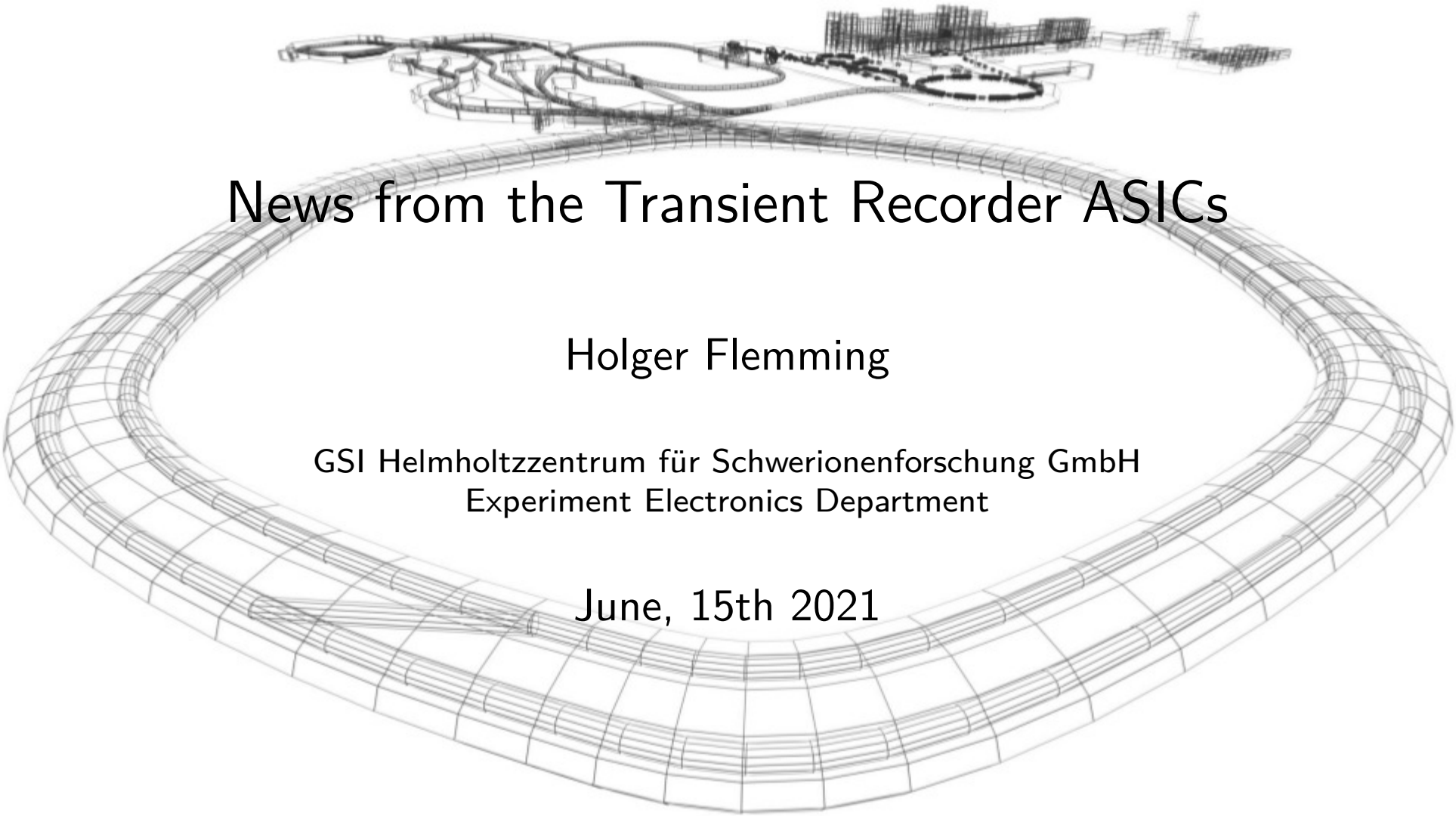

News from the Transient Recorder ASICs

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Introduction

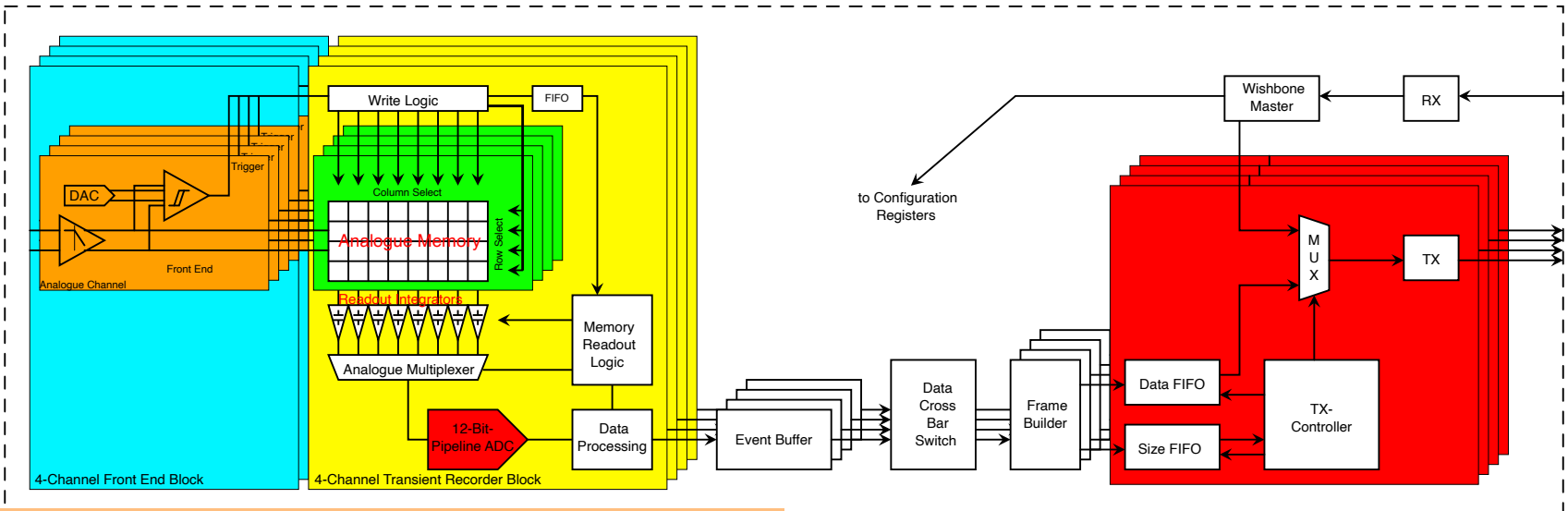
Analogue Transient Recorder (aka. HitDetection) ASICs
Currently two variants under development:

- $\pm 1\,\mathrm{V}$ differential input
  - PANDA EMC Readout
  - Characterisation results $\rightarrow$ Talk in EMC session of CM 20.3
- CSA input stage
  - PANDA GEM Tracker, SFRS GEM-TPC
  - Characterisation results $\rightarrow$ Talk by P. Wieczorek in FEE session of CM 20.1

Introduction

Generic Architecture

- 16 channel analogue transient recorder
  - Analogue memory 4 rows by 16 columns for each channel
  - 12 bit ADC
  - Data processing (calibration, feature extraction)
- Event buffer with trigger selector ⇒ Triggered and self-triggered operation
- Four serial links with 500 Mbit/s each



Highlights

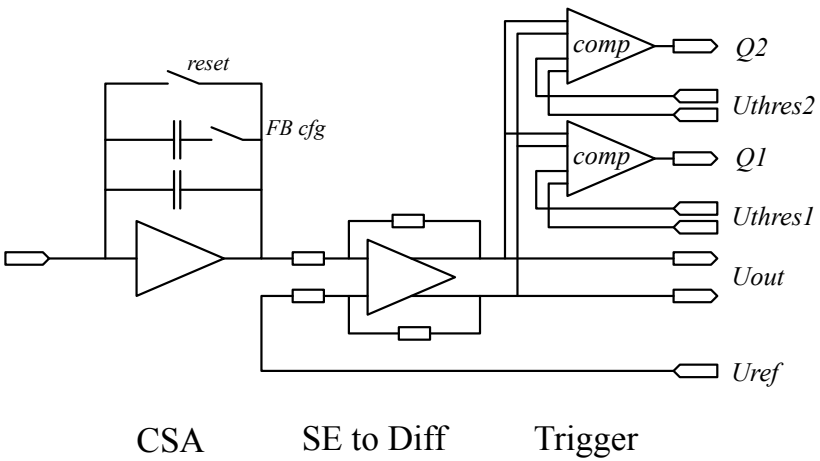
Event Triggering

- Input buffer variant
  - Leading edge discriminator and differential trigger mode ($\rightarrow$ Talk in EMC session of CM 20.3)
  - 12 bit threshold DAC
  - Automatic threshold setting ($\rightarrow$ Talk in PANDA FEE workshop 2019)
- CSA input variant
  - Leading edge discriminator mode
  - 2nd comparator for continous baseline monitoring
  - Automatic threshold setting and baseline adjustment

Highlights

Event Triggering

Triggering with CSA input variant



- U_{thres1}, U_{thres2} and U_{ref} generated with 12 bit DACs
- Q_1 used for baseline monitoring
- Q_2 used for trigger
- Baseline adjustment with U_{ref}
- Automatic threshold setting and baseline drift compensation

Highlights

On-Chip Data Processing

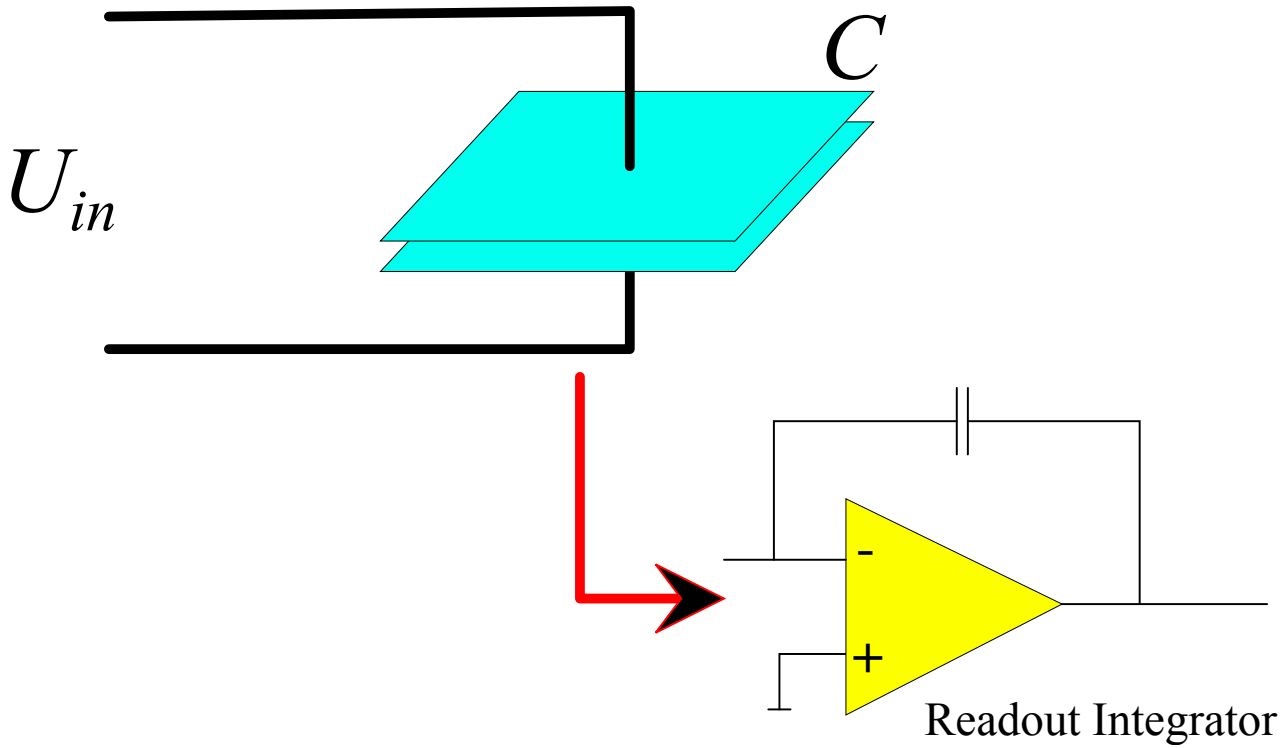
Why integrating on-chip data processing?

- CSA variant foreseen for SFRS GEM-TPC Readout ⇒ Triggered environment
- Limited Area for Latency Buffers ⇒ Data reduction ⇒ On chip feature extraction
- Memory correction has to be done before feature extraction

All data processing can be disabled, raw data is available!

Highlights

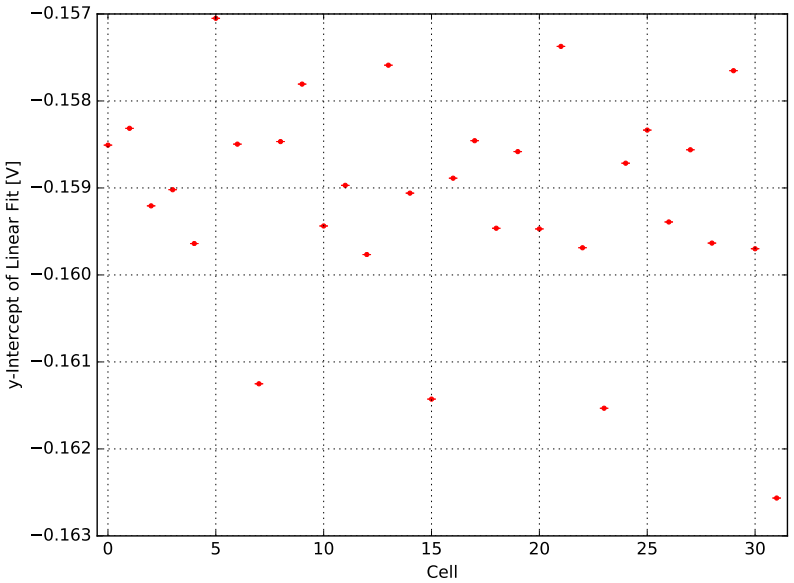
On-Chip Data Processing / Analogue Memory Correctioin



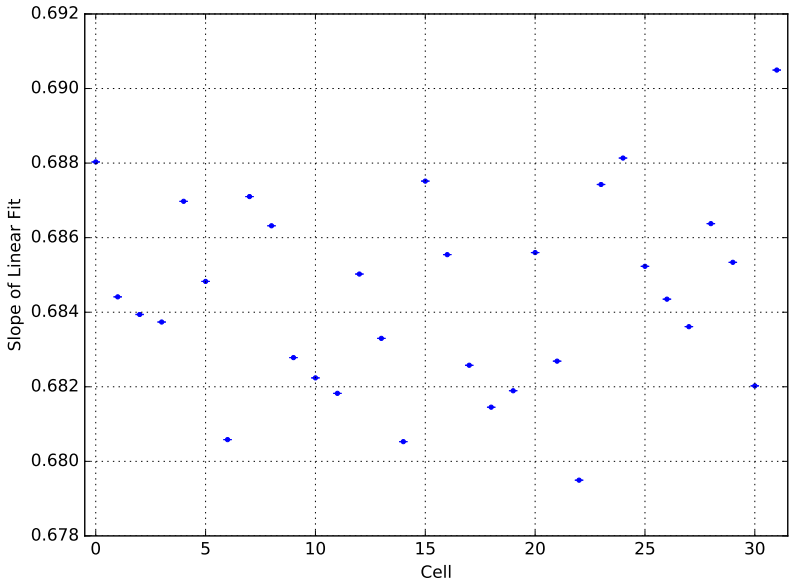
Memory cell written with voltage U, readout of charge $q = C_i U$
Capacity variations $\Rightarrow$ slope variations, Offsets due to asymmetries

Highlights

On-Chip Data Processing / Analogue Memory Correctioin



Offset



Slope

Measurements by P. Grasemann and O. Noll, HIM

To avoid additional noise variations have to be corrected!

Highlights

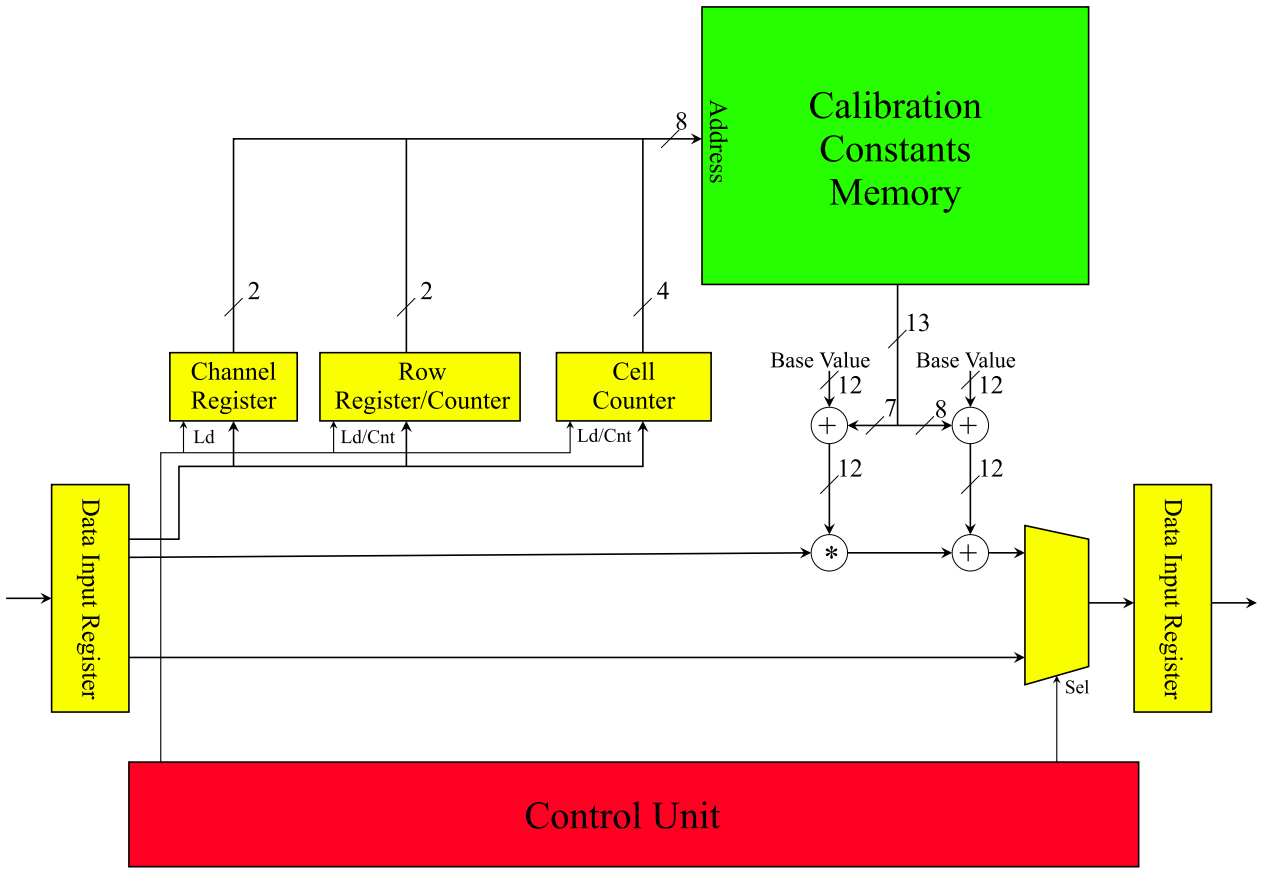
On-Chip Data Processing / Analogue Memory Correctioin

Calibration of memory correction

- Analogue inputs can be connected to internal DACs
- Recorder can be triggered manually / cyclic
  $\Rightarrow$ Recording of various defined DC levels
- Linear fit $U_{in} \Rightarrow n_{ADC}$ for individual cells
- Calculations of individual correction constants

Highlights

On-Chip Data Processing / Analogue Memory Correctioin



On Chip memory correction Unit

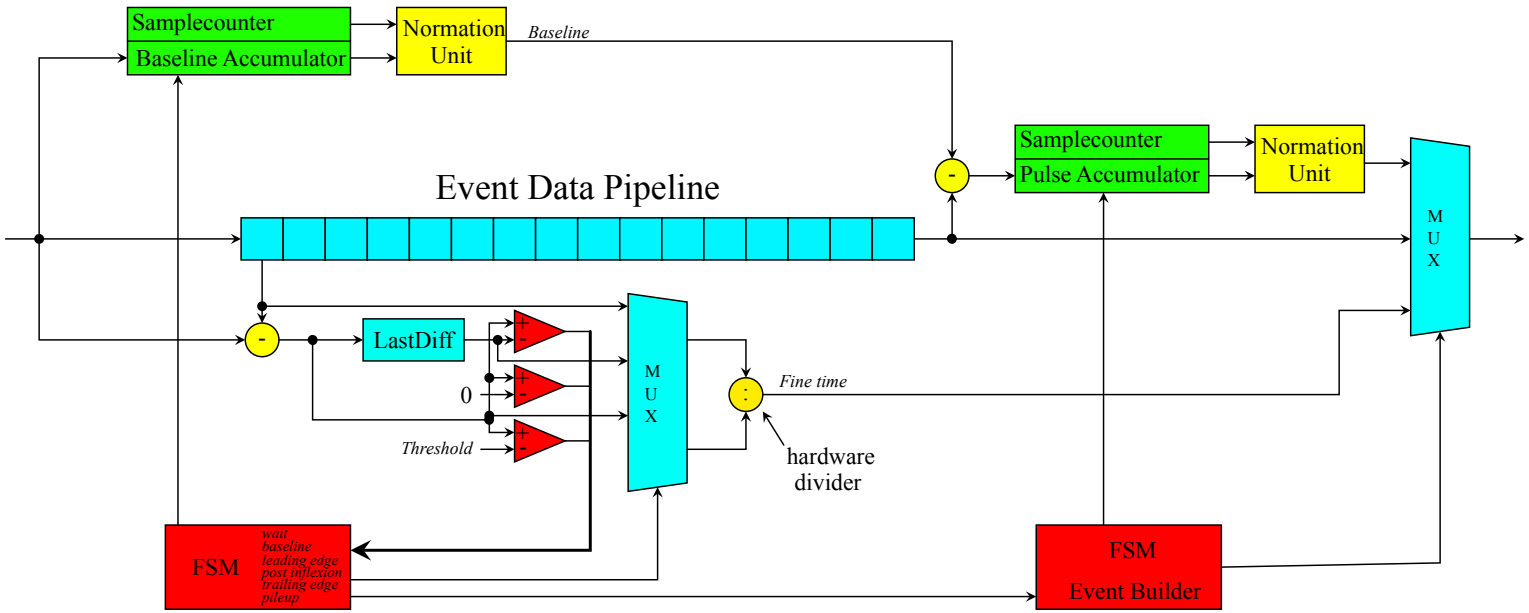
Highlights

On-Chip Data Processing / Feature Extraction

- Feature extraction of short transients (16 samples) differs from continous data streams
  Simulation studies presented in EMC Session of CM Nov. 2018
- Implemented Feature Extraction Processing Unit
  - 3 algorithms for time extraction
  - Configurable window integration for shaped pulses
  - Plateau integration for CSA transients

Highlights

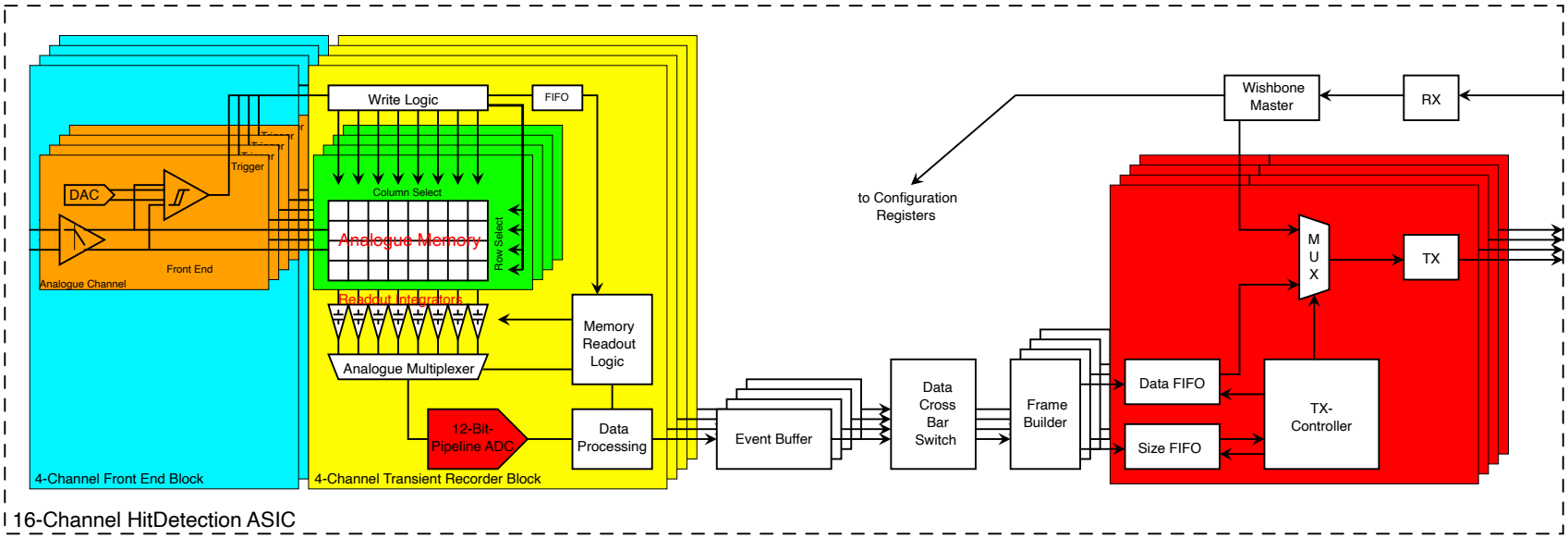
On-Chip Data Processing / Feature Extraction



Highlights

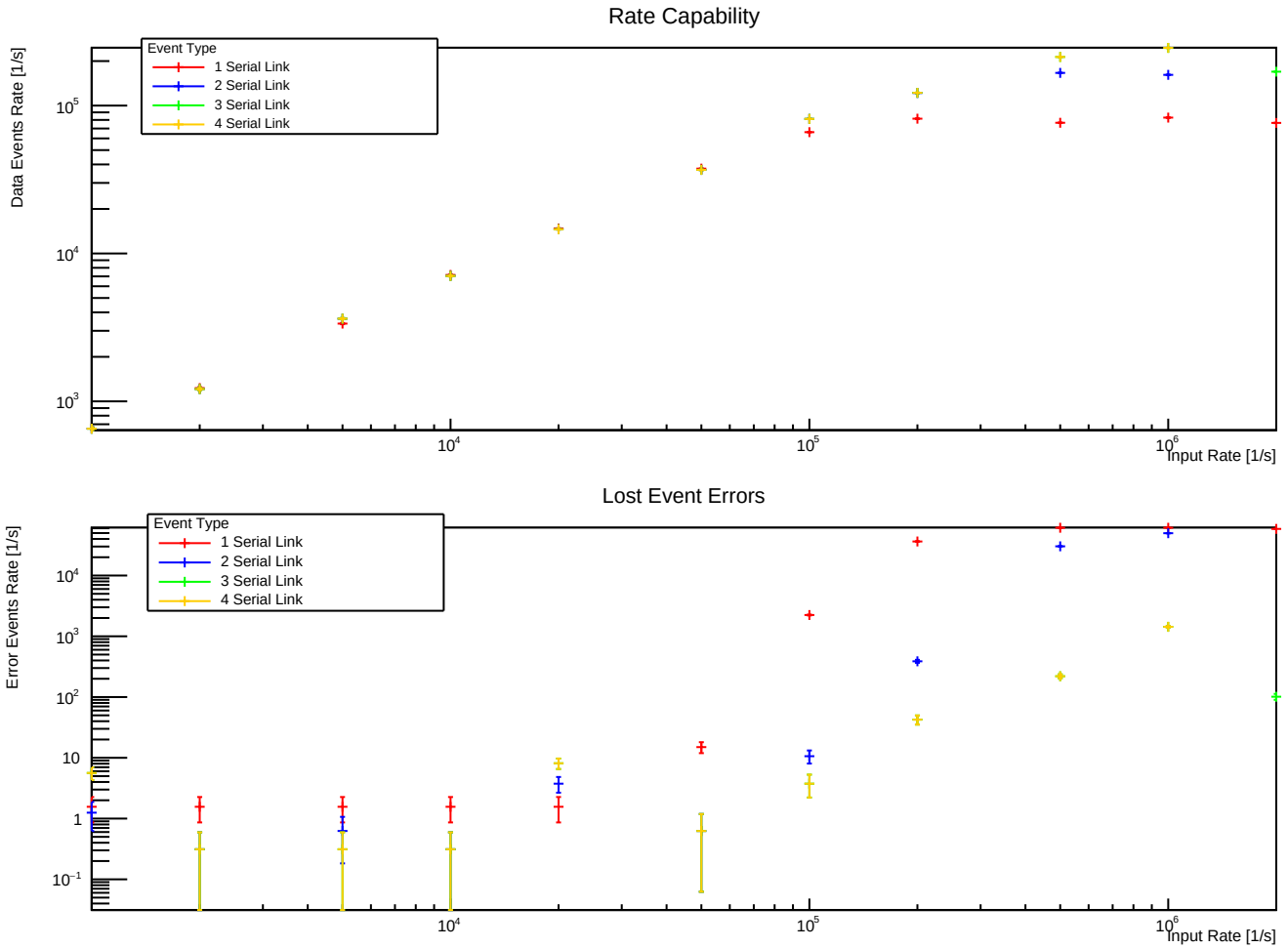
Data Transport

- For Serialiser 500 MBit/s on LVDS copper links each
- 1,2,3 or 4 Link operation
- Cross bar switch for link arbitration
- 1 Uplink with asymmetric bit rate



16 Channel Prototype for PANDA

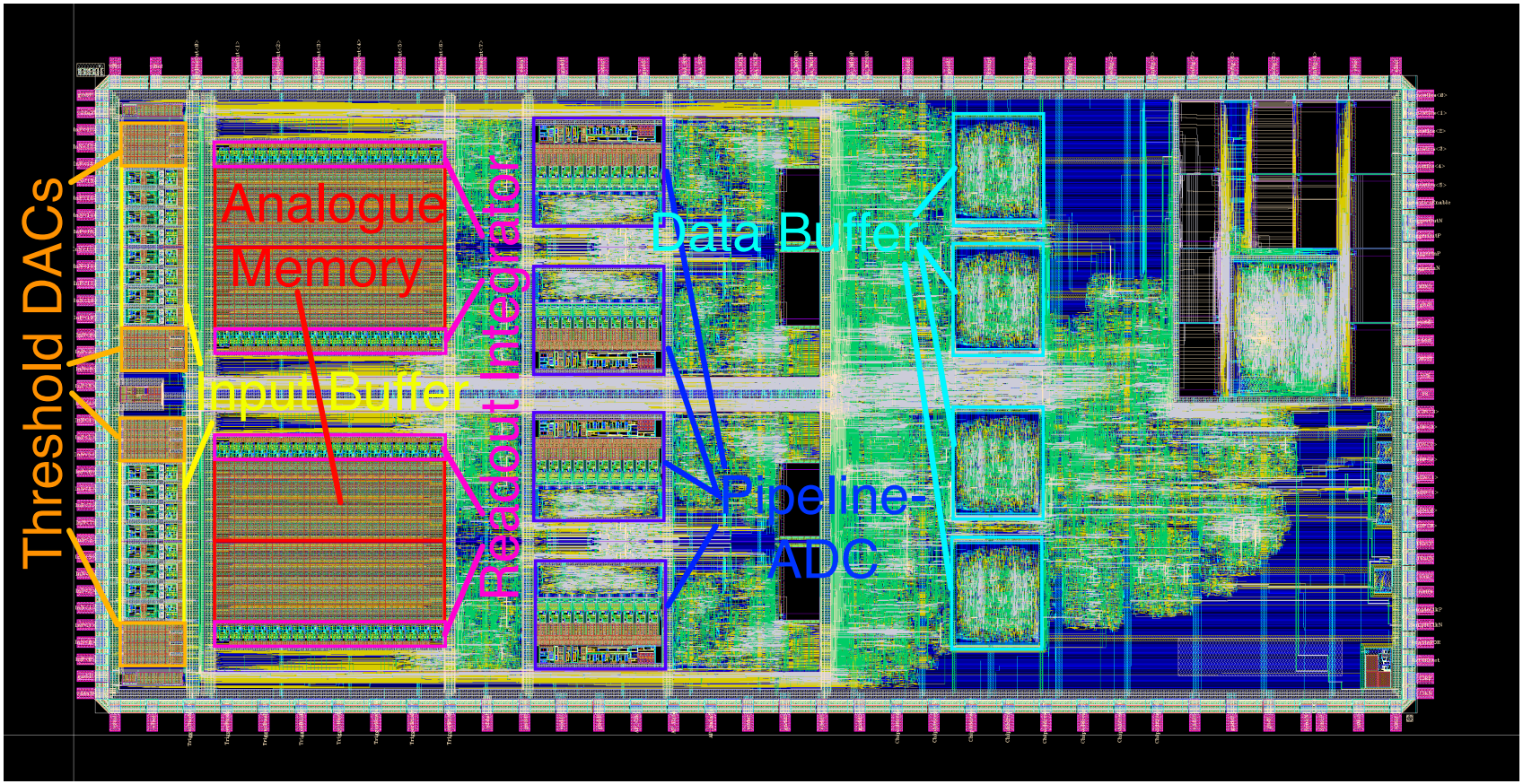
Data Transport



Prototype Production

- Both designs completed.
- Chip area: 5×10 mm^2, each
- Some numbers of input buffer variant:
  - 144 pins
  - 1 732 354 NMOS transistors
  - 1 555 283 PMOS transistors
  - 14 675 capacitors
  - 7570 resistors
  - 6 diodes
- Tape out was foreseen for MPW run on May 10th
  Run was canceled by UMC one week before deadline!
- Currently clarified if engineering run is an option.

Analogue Transient Recorder Backend



Layout of the input buffer variant