TDC and Read out Board
version 3

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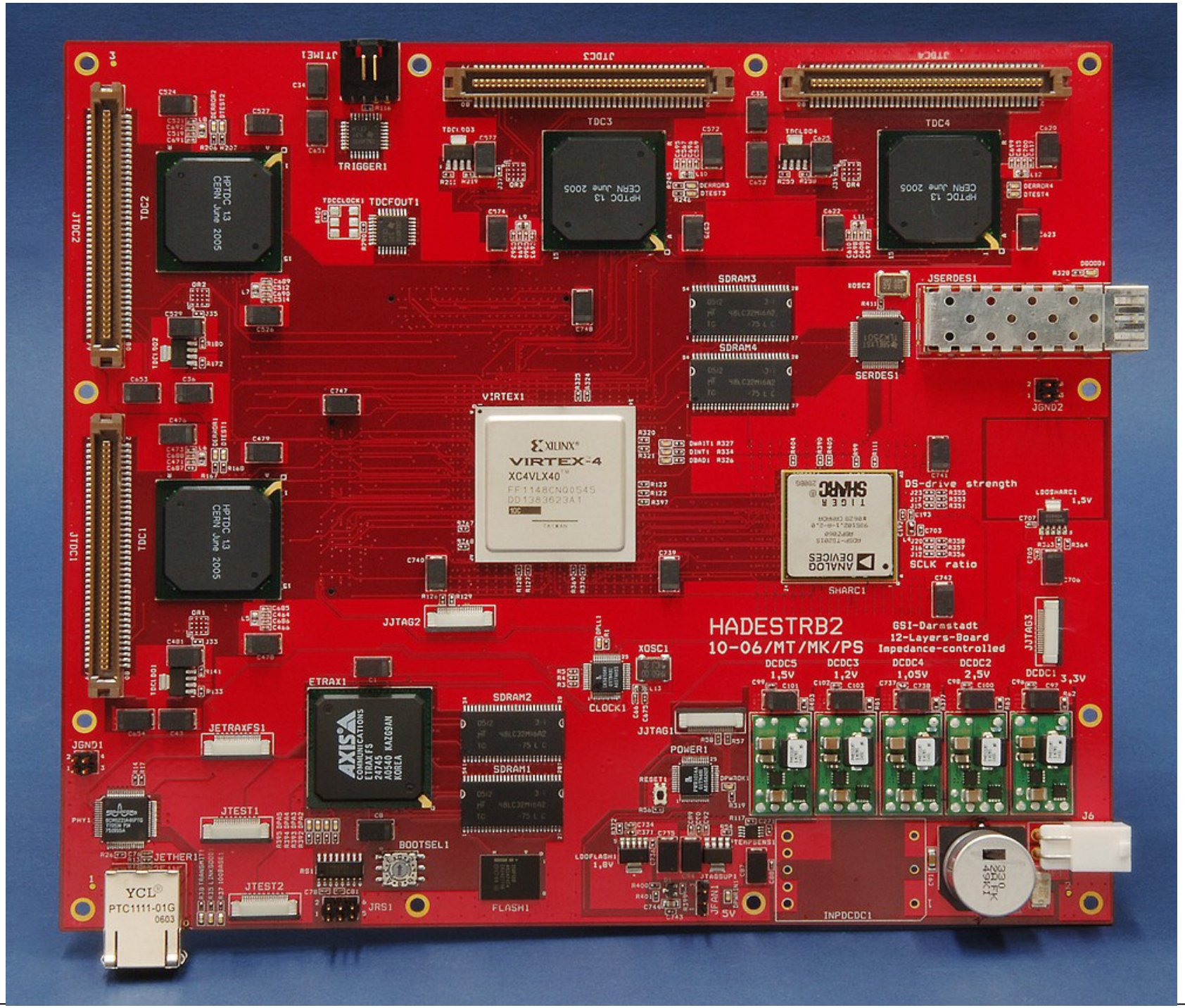
- TRB version 2
- TRB version 3
  - Specification
  - Layout
  - Application
- Current status

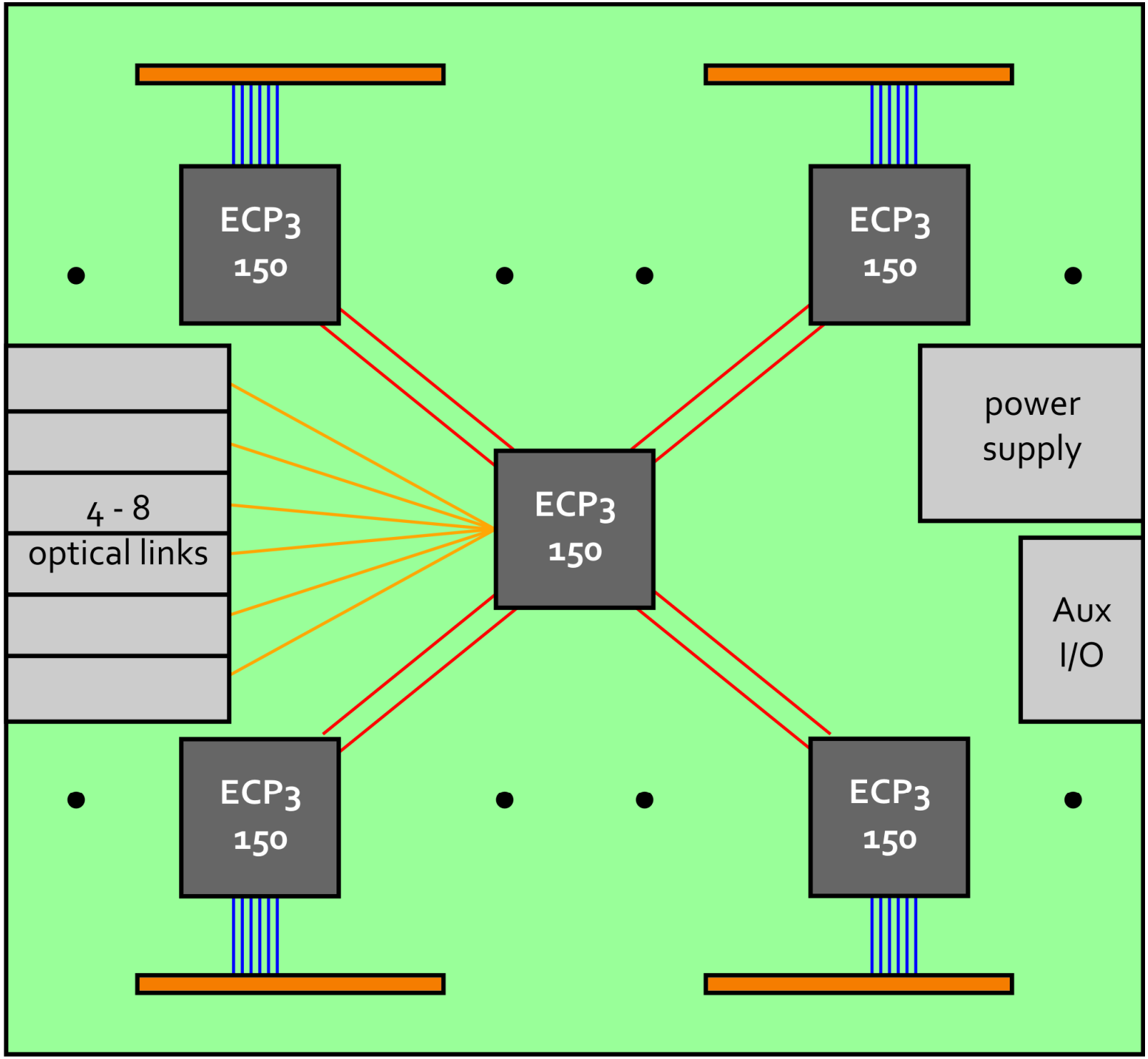
TRB version 2

- 4 x HPTDC
- Viretx 4
- DSP (Sharc from Analog Devices)
- ETRAX FS with Linux
- SDRAM (32M x 32-bit)
- 100 Mb Ethernet
- 2.5 Gb/s optical link


HADESTRB2
10-06/MT/MK/PS
GSI-Darmstadt
12-Layers-Board
Impedance-controlled
VIRTEX-4
XC4VLX40
TDC3
TDC4
TDC2
TDC1
SDRAM3
SDRAM4
SDRAM2
SDRAM1
JSERDES1
SERDES1
SHARC1
DS-drive strength
SCLK ratio
ETRAX1
JETRAXFS1
JETHER1
JTEST1
JTEST2
BOOTSEL1
FLASH1
CLOCK1
POWER1
INPDCDC1
TRIGGER1
TDCFOUT1
DCDC5 1,5V
DCDC3 1,2V
DCDC4 1,05V
DCDC2 2,5V
DCDC1 3,3V

TRB version 3

- ECP3 FPGA family from Lattice
  - LFE3-150EA-8FN1156C - central FPGA
  - LFE3-150EA-8FN672C - edge FPGA
- 4 to 8 3.2 Gb/s optical links
- 4 208-pin I/O connectors
- 125 MHz and 200 MHz on-board oscillators
- External trigger and clock inputs
- Single 48 VDC power supply


ECP3
150
ECP3
150
4 - 8
optical links
ECP3
150
power
supply
Aux
I/O
ECP3
150
ECP3
150

Mezzanine card connector

QMS family from Samtec

Performance:

Pins:	up to 8.0 GHz / 16 Gbps
Supply blades:	max. current: 9.2 A

Pin usage:

12-bit DQ lanes	13		
2.5V lines	16		
bidirectional serdes lines	6		
2.5V lines from central FPGA	8		
3.3V lines from central FPGA	4		
four supply blades:	2 * GND,	+6.5V,	+3.3V

Mazzanine Card

- Edge FPGA has six serial, high speed links to the connector and 164 digital data lines
- Supply voltages: 6.5V and 3.3V

Applications:

- Adapter for a cable connection
- Optical data transmitter
- Multichannel ADC card

TRBv3 Application

- Each edge FPGA may contain up to 40 TDCs
- Time resolution confirmed by tests: <10 ps
- Edge FPGA has two high speed links to the central FPGA (up to 3.2 Gb/s)
- Central FPGA may have up to eight optical links

Status

- The design complete
- PCB design in progress (mid-May)
- Production mid-June
- From June on → tests
- Code development is going on