Development of Front–End Electronics for Straw Tubes

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Outline

Motivation

Goals for Front–End Design

- Time measurements with 1–2 ns resolution.
- Energy meaurement (ToT or Amplitude).
- Low noise – Threshold for discriminator (5 σ) $\approx$ 2 fC.

Main Difficulties to Overcame

- Detector signal shape:
  - Long ion tail – tail cancellation circuit is needed.
  - Variable detector pulse shape – for good time resolution short peaking time needed.
- Fluctuations of baseline caused by: high count rate, temperature and residuals from tail cancellation $\Rightarrow$ baseline stabilisation is needed.

Front–End design is difficult!

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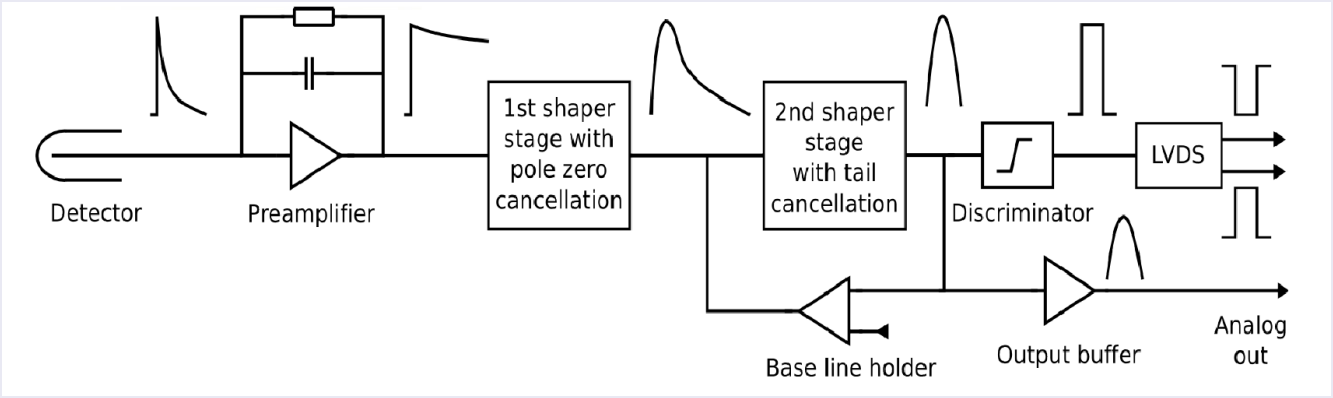
FE Architecture
Specifications



- 1^{st} prototype technology AMS C35B4 – $0.35\ \mu m$
- 2 output signals – Timing and Time–over–Threshold, Amplitude
  It is not final configuration, only for studies
- Preamplifier with variable gain and time constants
- CR–RC^2 Shaper with variable T_{peak} – default $\approx$ 20 *ns* for delta pulse
- Ion tail cancellation circuit with trimming
- Baseline stabilized by BLH circuit
- Leading edge discriminator for time measurements
- Fast LVDS output

FE Architecture
Specifications

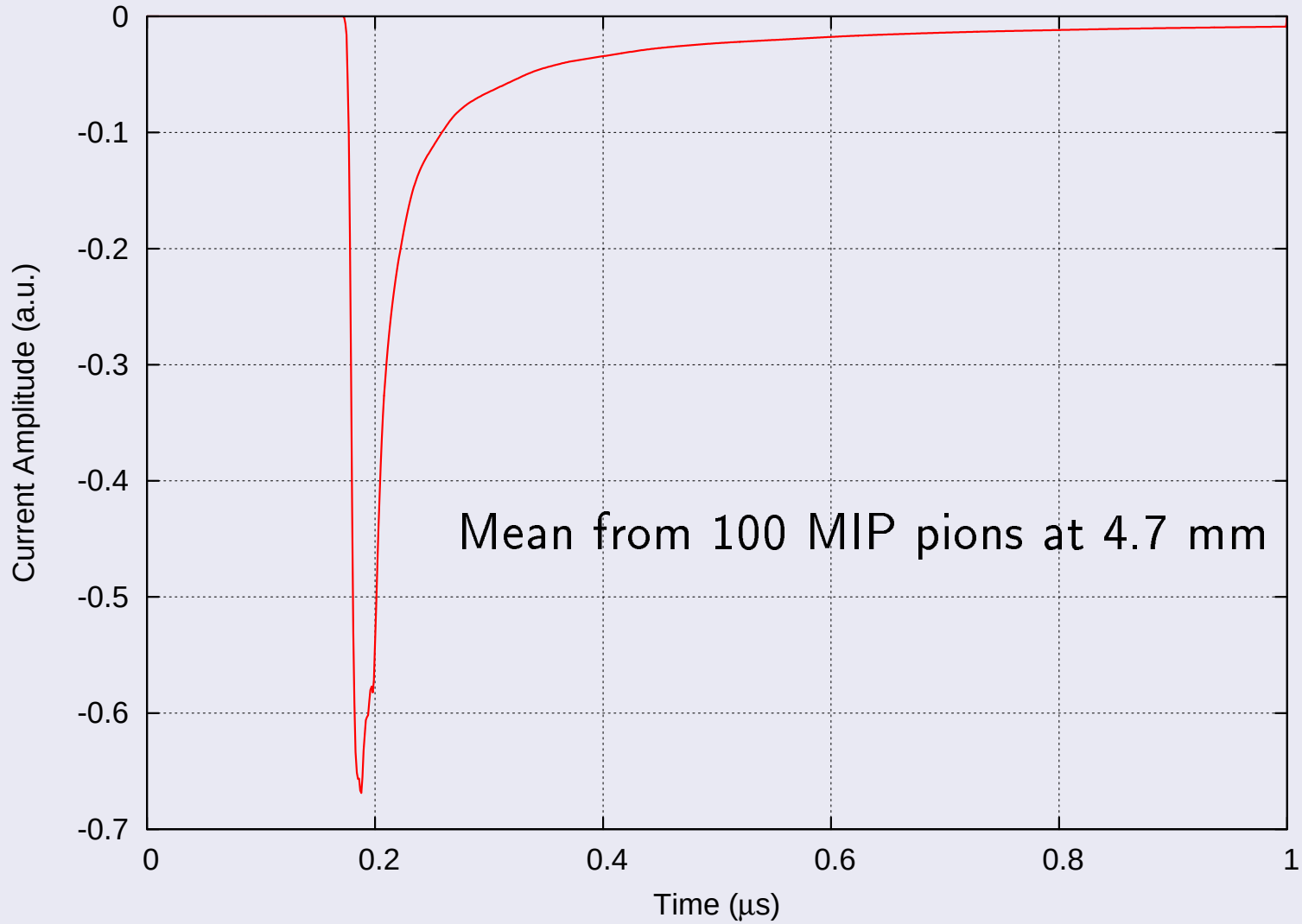
More detailed specification

Parameter	Range/Value
Charge gain [mV/fC]	3 – 20
Peaking time (for delta) [ns]	15–40
Power consumption [mW]	$\approx$ 16
ENC [fC]	$<$ 0.4
1^{st} TC time constant [ns]	20 – 500
2^{nd} TC time constant [ns]	3 – 40
Input transistor parameters	
Dimensions W/L	$2000\mu/0.35\mu$
Transconductance [mS]	$\approx$ 26
Drain current [mA]	2

Charge gain depends very much on tail canncellation circuit settings (through voltage gain of last shaper stage)

Simulations results

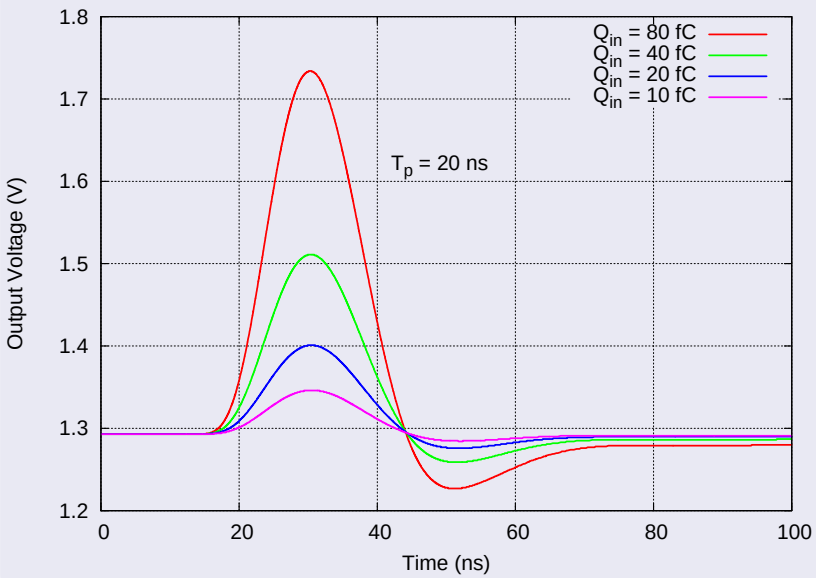
Reference detector pulse used in simulations



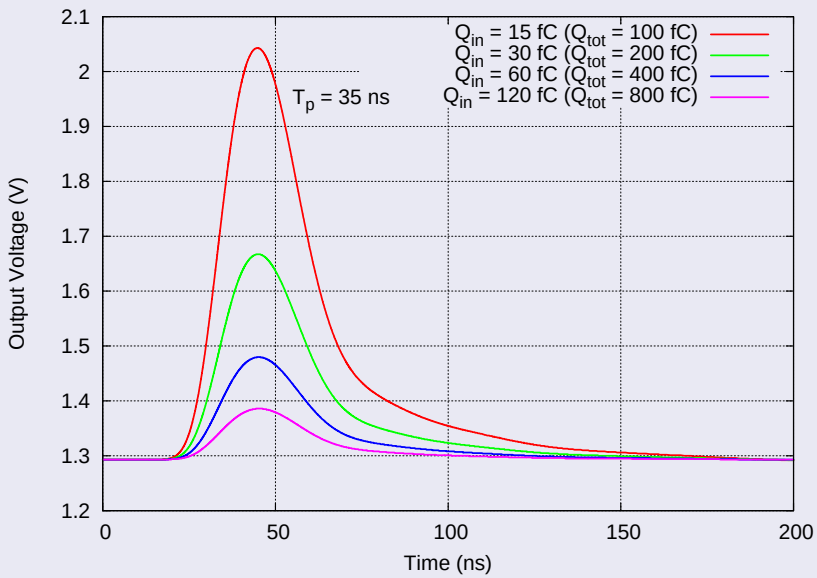
Simulations Results

Transient Response

Response to delta pulse

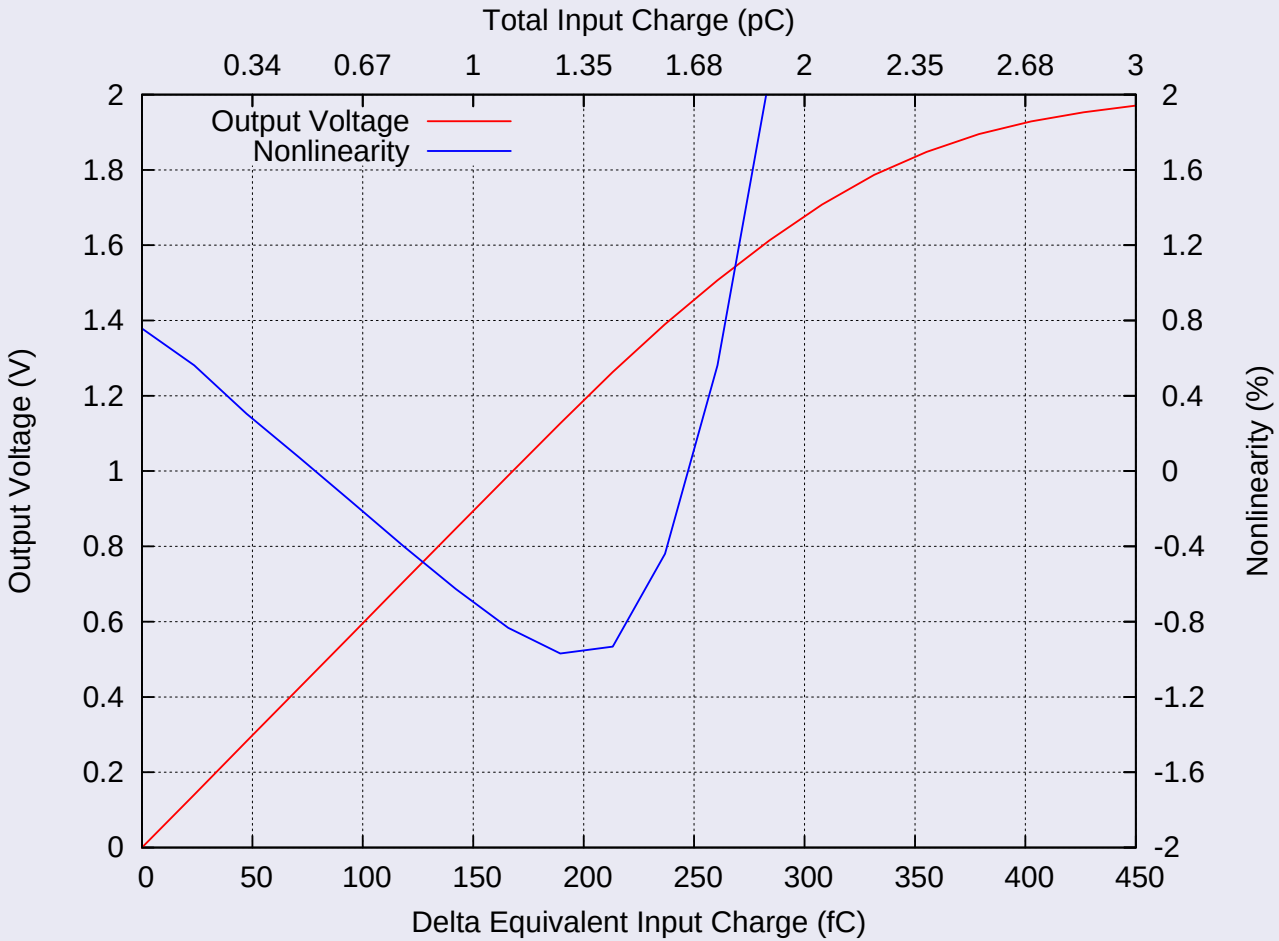


Response to reference pion



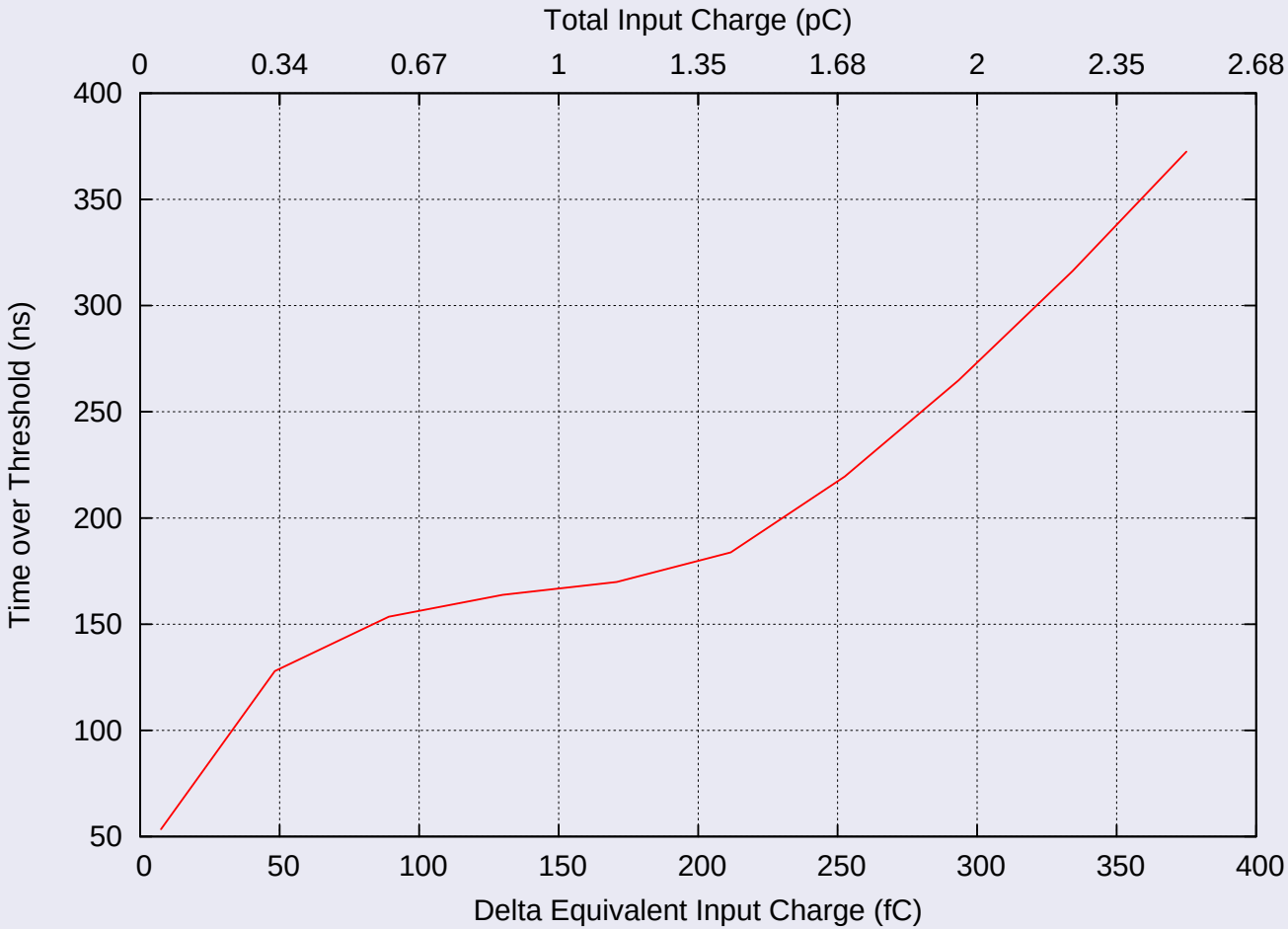
Simulations Results

Linearity and Dynamic Range



Simulations Results

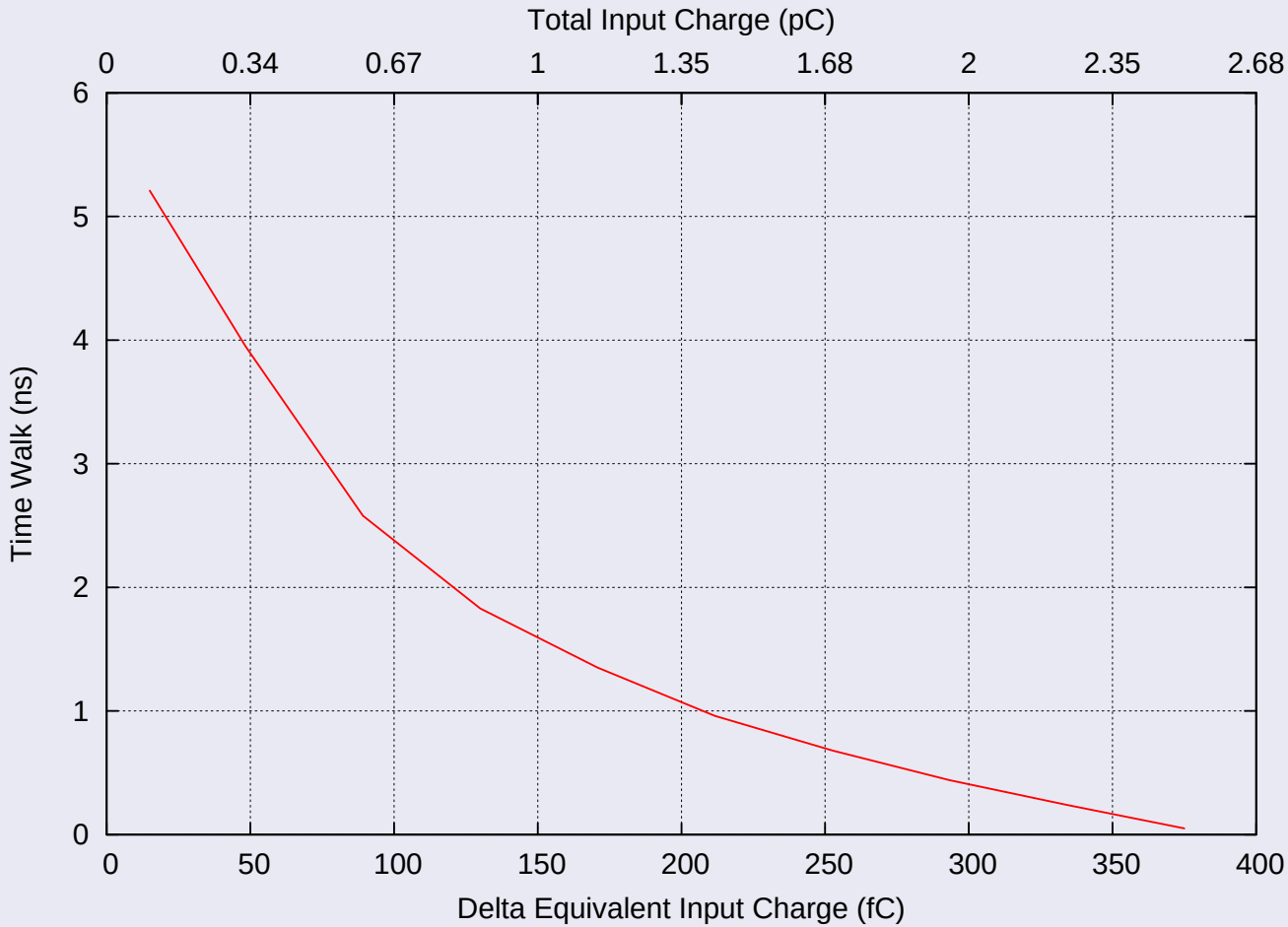
Time–Over–Threshold



Depends significantly on tail cancellation settings

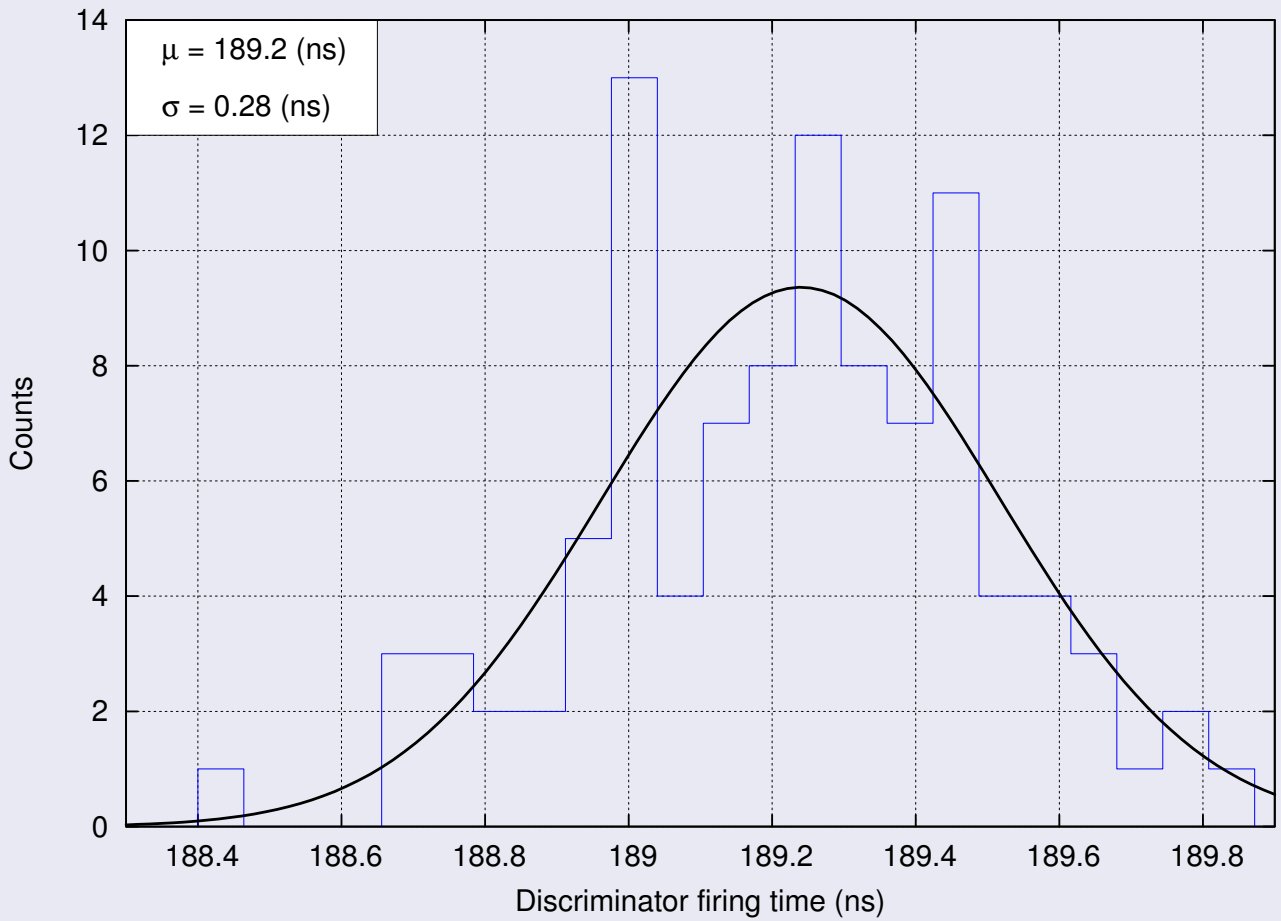
Simulations Results

Time Walk



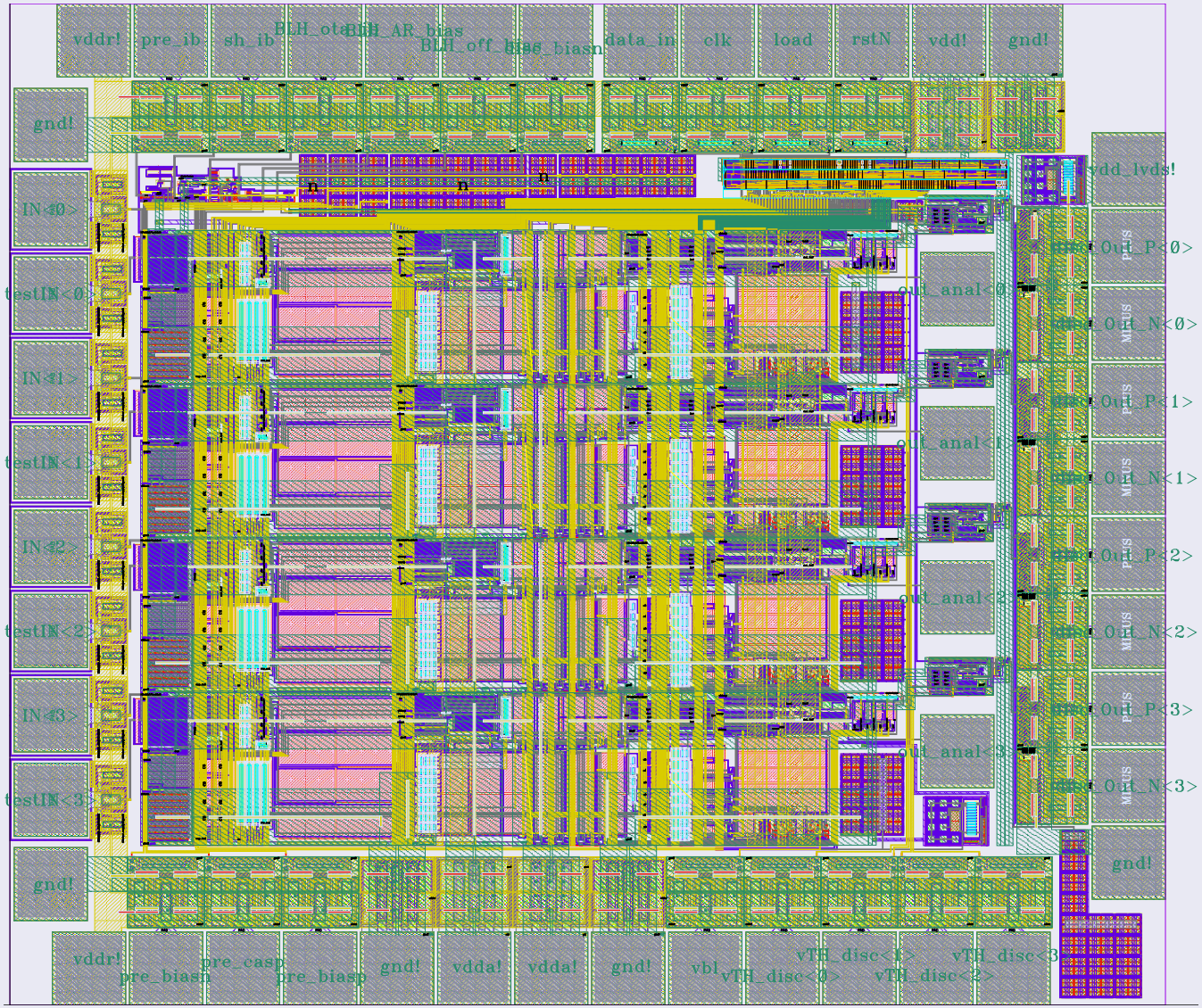
Simulations Results

Time Jitter



Layout

4 channels 1^{st} prototype. Chip size: $1.5 \times 1.3\ mm^2$



Conclusions

- 1^{st} Front–End prototype is designed and submitted.
- 1–2 ns time resolution can be achieved.
- Energy measurement using Amplitude or ToT available for studies.
- Impuls width (1%) for default settings is $\approx$ 150 ns $\Rightarrow$ few MHz counting rate is achievable.

Warning

miniASIC submission done during transition between Cadence (and simulators) versions to catch–up April deadline, some disagreements between different simulators – presently under study. In worst case would need to be resubmitted in july.