Straw Tube Readout with MSGCROC-ASIC

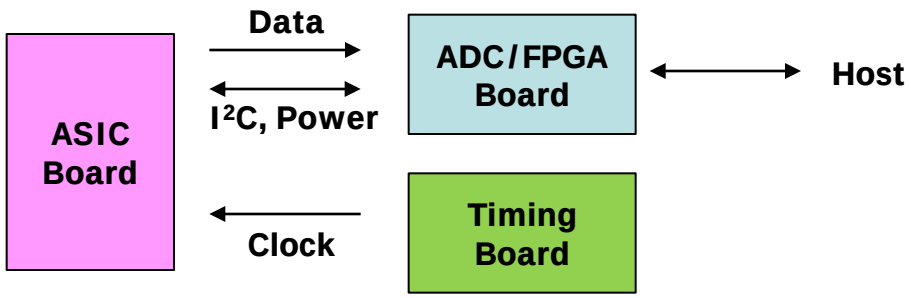
- Straw tubes for particle identification and tracking
  - Energy and time information of detectors needed
- 32 Channel MSGCROC-ASIC with such capabilities
  - Developed in FP7 NMI3 project DETNI (mainly by AGH Krakow in cooperation with University Heidelberg)
  - **But:** Analogue part optimized for Gd/CsI-MSGC detector, e.g.:

Micro-Strip input capacitance [pF]	20 - 40
Deposited charge per event (e^-)	$2 \cdot 10^5 – 3 \cdot 10^6$
Signal peaking time	15 ns (22 ns FWHM)
ENC [e^- rms] for energy signal 5σ Thr.	2000

  - Also 2nd version of ASIC with 128 channels existing (n-XYTER)
- Develpment of small scale system for evaluation of MSGCROC for straw tubes

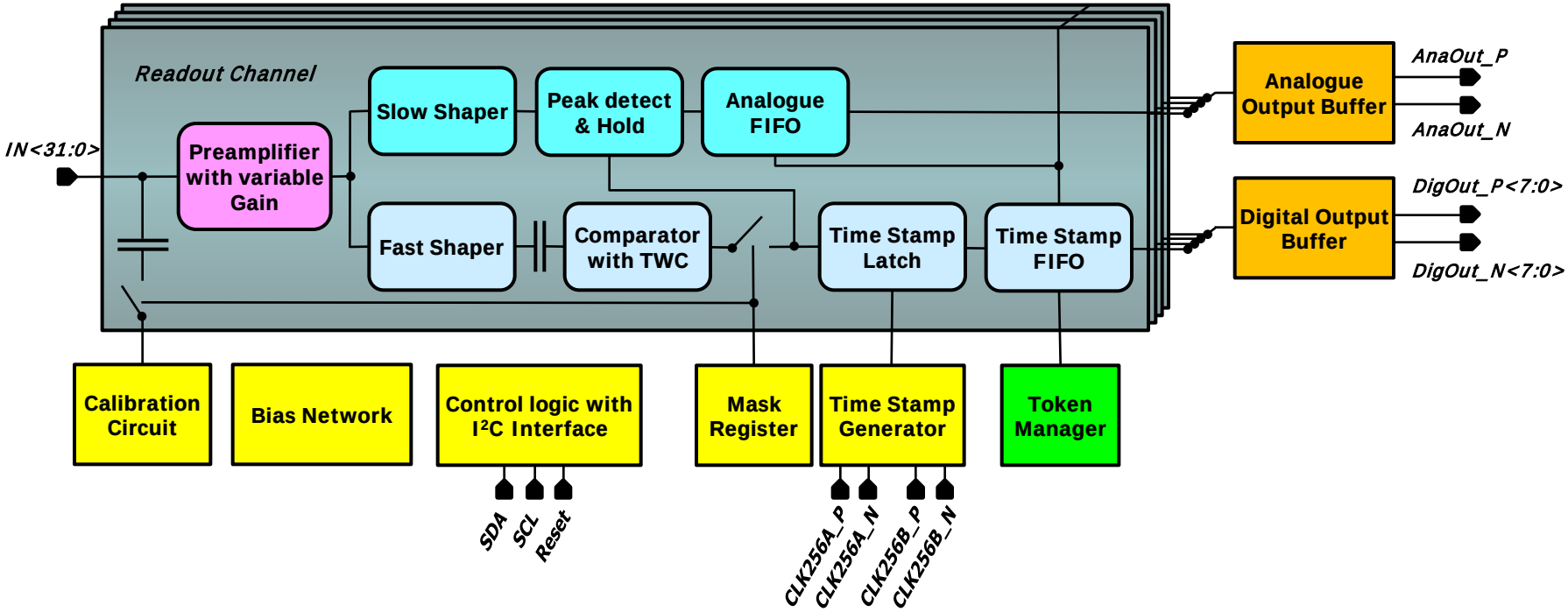
Readout System Architecture

- System functionality partitioned on separate boards
  - ASIC board with coupling of MSGCROC to straw tubes
  - Timing board for ASIC board clock supply
  - ADC/FPGA board for control & readout of ASIC board



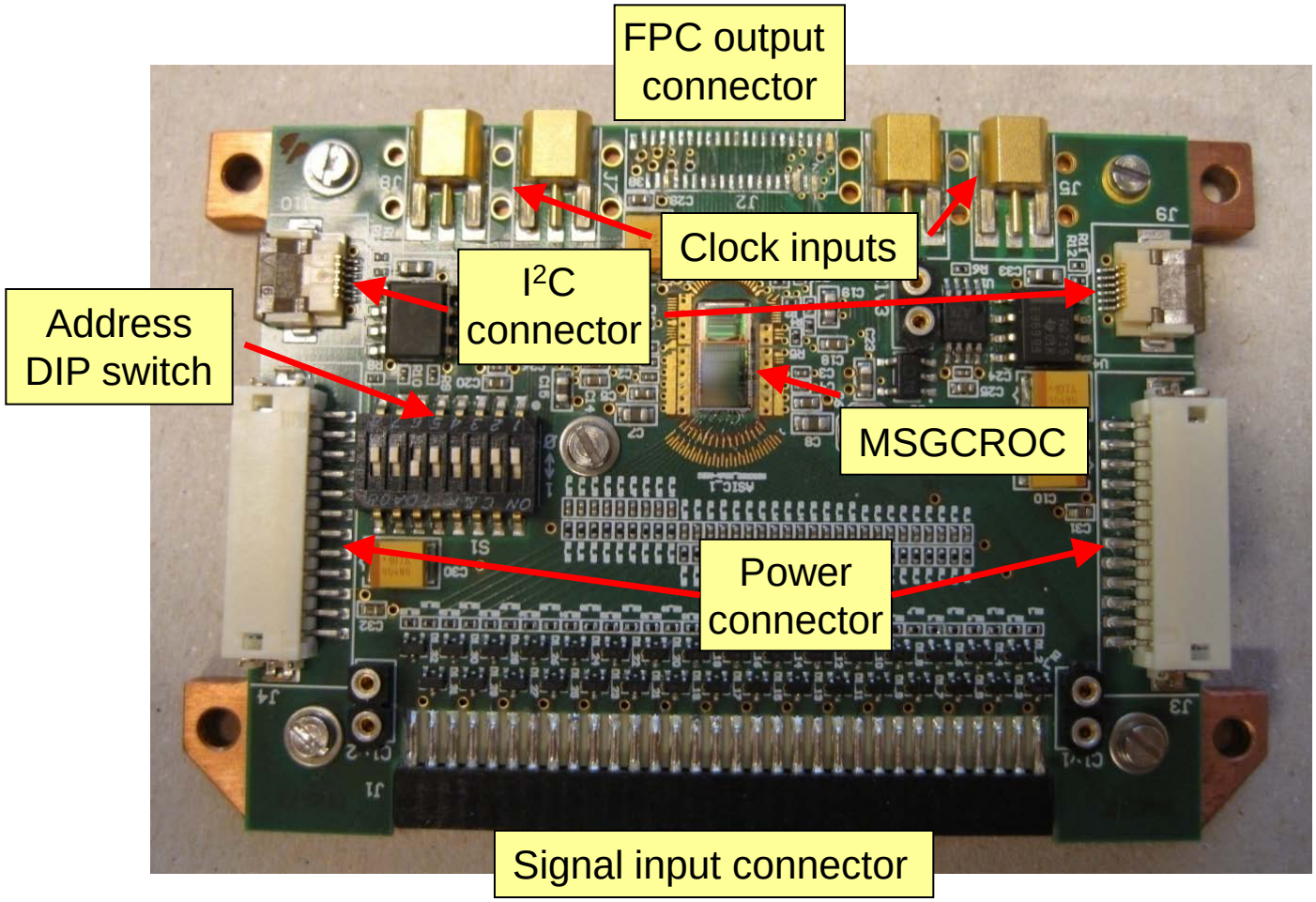
- Moderate efforts were needed for the development
  - New ASIC board developed/adapted to straw tubes (10 ASICs HZB)
  - Readout and timing boards available from DETNI project
- Goal: Test of energy resolution, time stamping for tracking

MSGCROC Block Diagram



- Accepts both input polarities
- 32 individual Channels
  - Channel-wise self triggered
  - Up to ~900 kHz hit rate per channel
- Variable preamplifier gain
  - 5 gain modes x1, x2, x4, x8, x16
- ASIC Outputs:
  - Analogue amplitude
  - Time stamp (2 ns with 14 Bit)
- Token-ring readout
  - Skip empty channels
  - Derandomization
  - Zero suppression

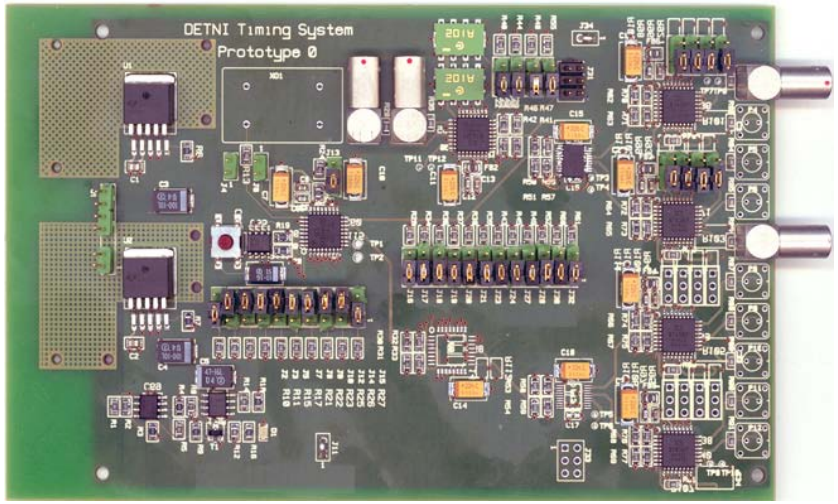
MSGCROC Board adapted to Straw Tubes

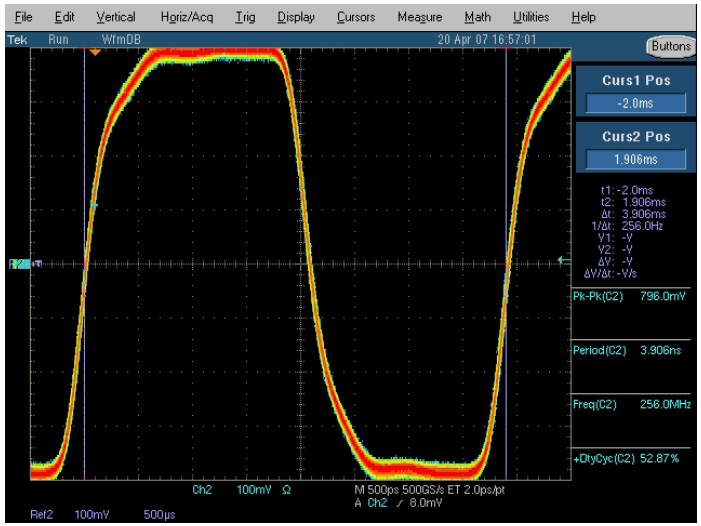


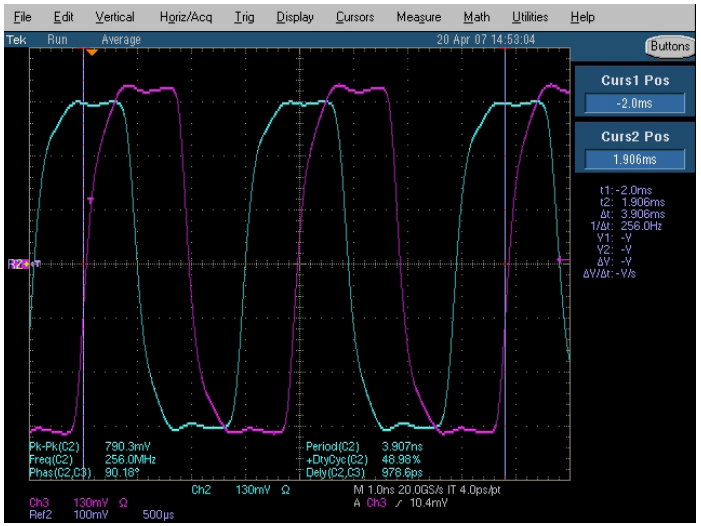
- Developed by J. Majewski (Krakow) by order of FZJ-IKP

Clock Distribution Board

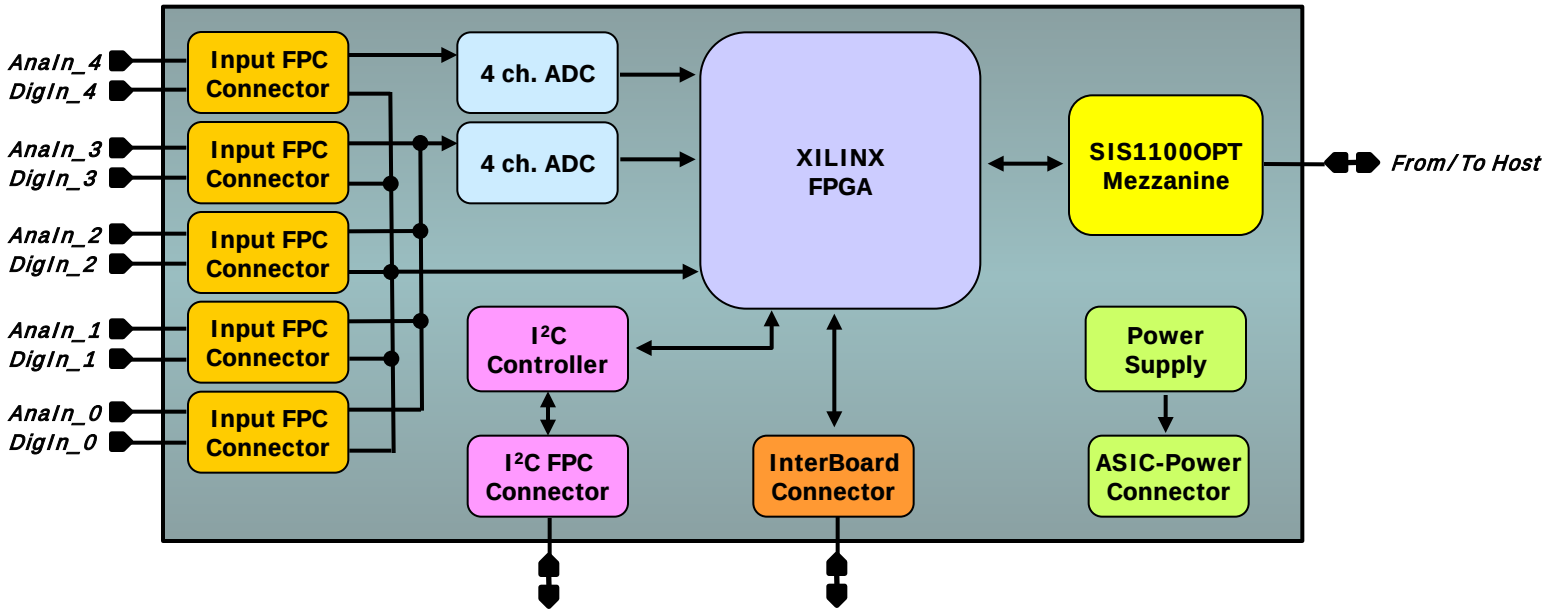
- Master clock 32 MHz
- Board output clock signals:
  - 5 x 256 MHz and 5 x 256 MHz 90° phase-shifted
- Clock precision:
  - Jitter: 30 ps max. (LVDS outputs)
  - Skew: 150 ps (path to path)
  - 90° phase stability: ± 10°





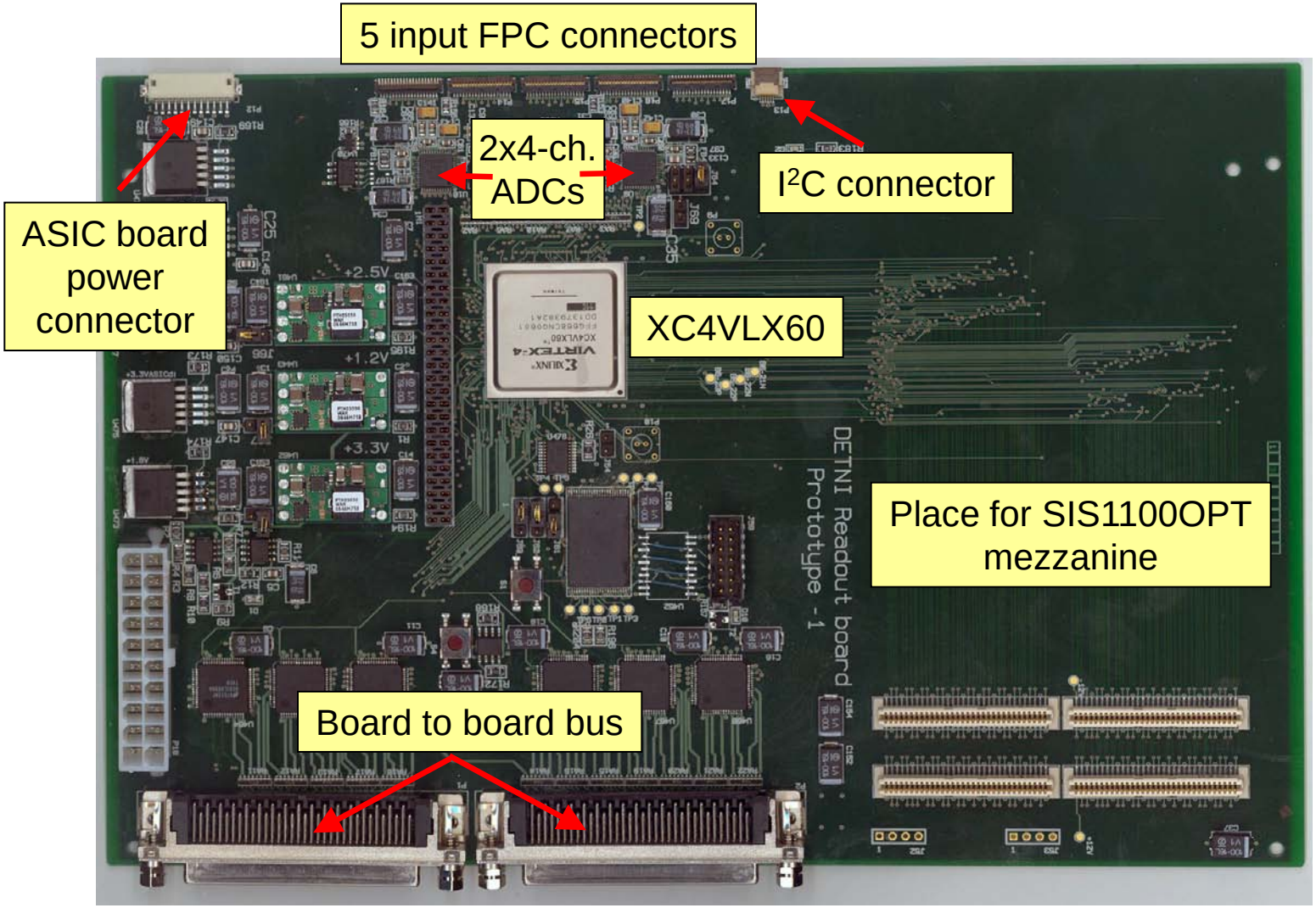


ADC/FPGA Board Blockdiagram

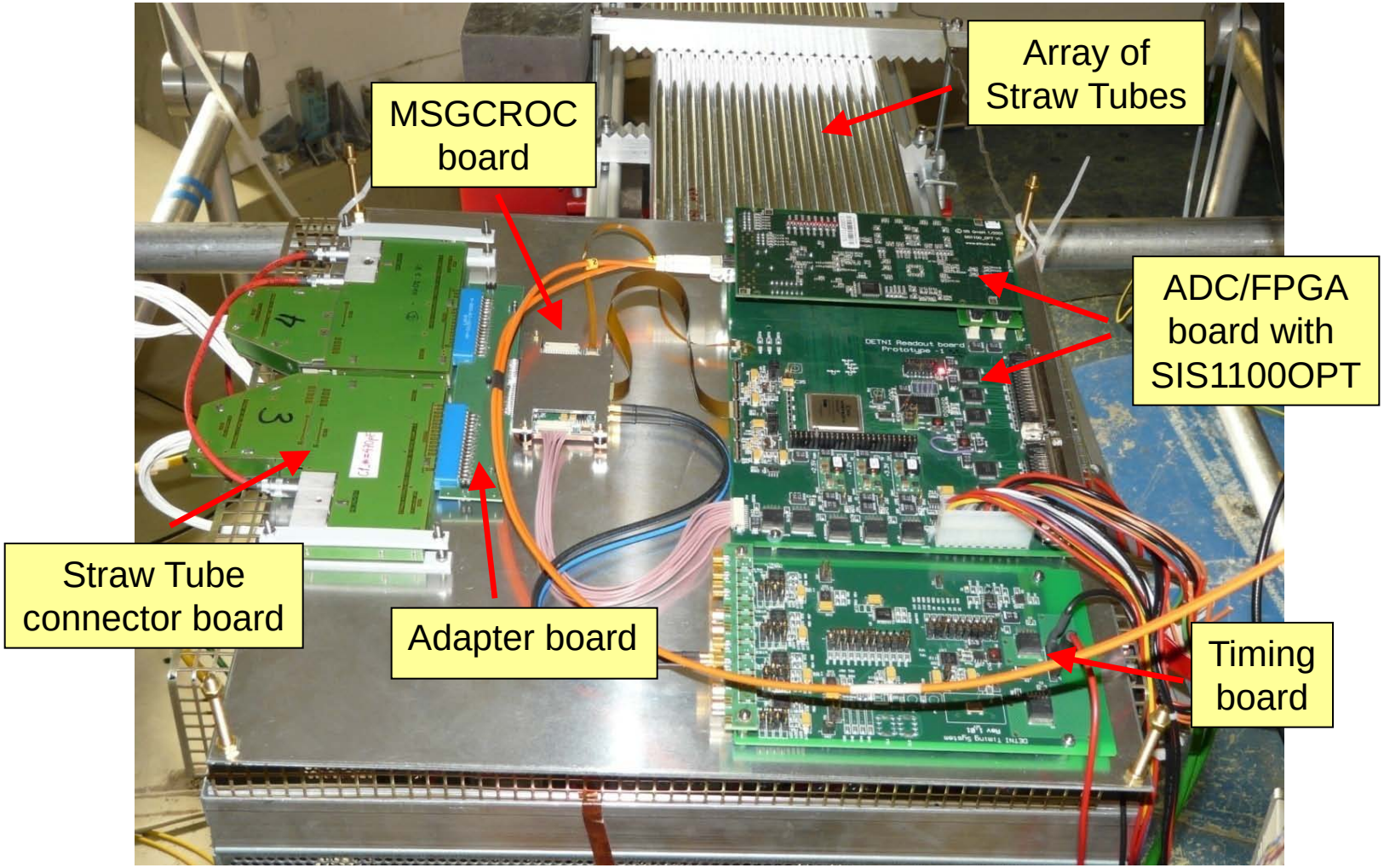


- ASIC board readout
  - Digital data @ 32 MHz readout cycle (8 bit @ 128 MHz)
  - Analogue data are fed into 2 Quad-channel ADCs (AD9229)
  - Merging of data inside FPGA and transfer to host via SIS1100OPT
- ASIC setup and power supply
  - Access to I^2C via FPGA and I^2C controller (PCA9564)
  - Up to 7.5 Amp @ 3.3 V
- Board to board communication
  - Transparent access via FPGA on 1^{st} board
  - Data transfer 32 Bit @ 40 MHz

ADC/FPGA Board

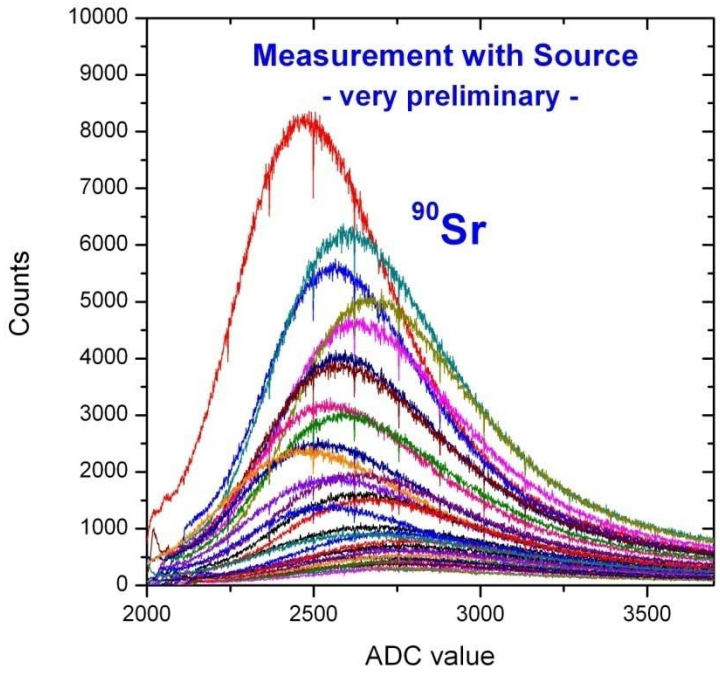


Test Setup at COSY



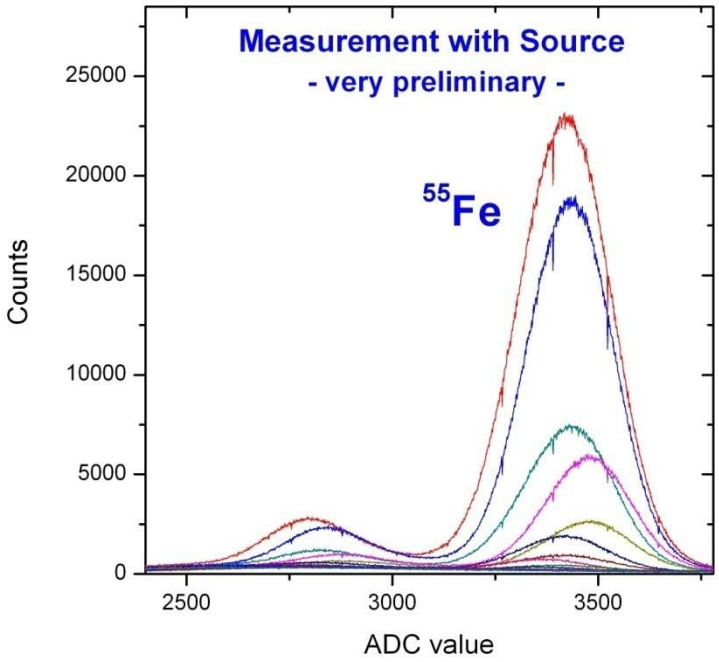
System Commissioning: First Tests (1)

- System has been recently put into operation at COSY
  - Tests with β- and γ-sources during commissioning phase
  - Annoying deficiency: pedestals at middle of ADC range due to missing ADC buffer on ADC/FPGA-board
  - Beam tests envisaged at a later stage



- Measured amplitude distributions of electrons from a ^{90}Sr-source
- Visible problems:
  - Different peak locations of channels (different gains or offsets ?)
  - Strange equidistant intensity drops within spectra (ADC ?)
  - Additionally also strange behaviour at out-of-range pulses

System Commissioning: First Tests (2)



- Measured amplitude distributions of 5.9 keV γ-rays from a ^{55}Fe-source
- Obviously: same problems as with ^{90}Sr spectra
- Estimation of energy resolution:
  - By location of 5.9 keV photopeak and 3 keV escape peak
  - Preliminary result: $\Delta E/E$ (FWHM) ~ 20%

Summary & Outlook

- Small scale readout system for evaluation of MSGCROC-ASIC for straw tubes has been developed
  - Test of energy resolution and time stamp for tracking
  - New ASIC board developed, adapted to straw tubes
  - Reuse of timing- and ADC/FPGA-boards, developed for DETNI
- System Commissioning
  - First measurements carried out with β/γ-sources
  - Some strange effects observed in pulse height spectra
  - Tests are still in a very early stage, so no reliable results so far
- Next Steps
  - Further investigations in spectra by source measurements to understand and solve problems
  - Short to medium term: redesign of ADC/FPGA board
  - Measurements with COSY beam