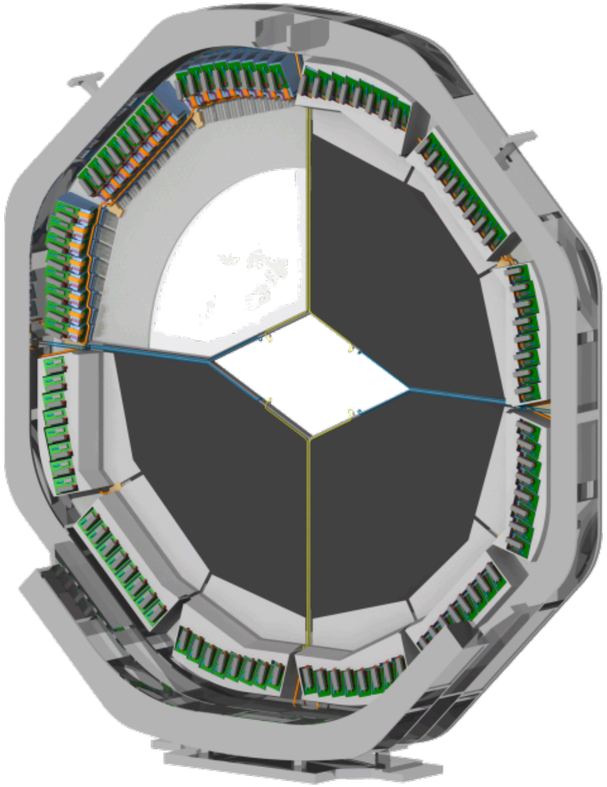
Data Acquisition of the PANDA Endcap Disc DIRC Project



Simon Bodenschatz, Lisa Brück, Michael Düren, Avetik Hayrapetyan, Jan Hofmann, Sophie Kegel,

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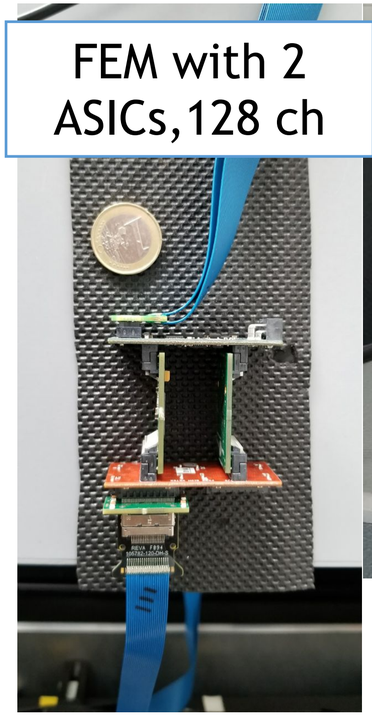
PANDA CM 21/1- 2021/03/10

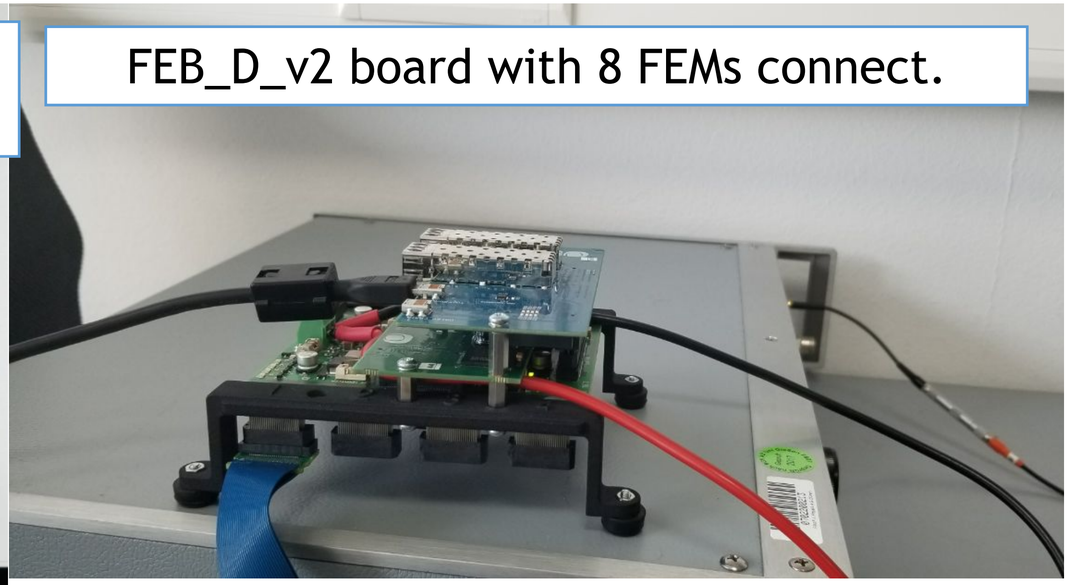
Requirements

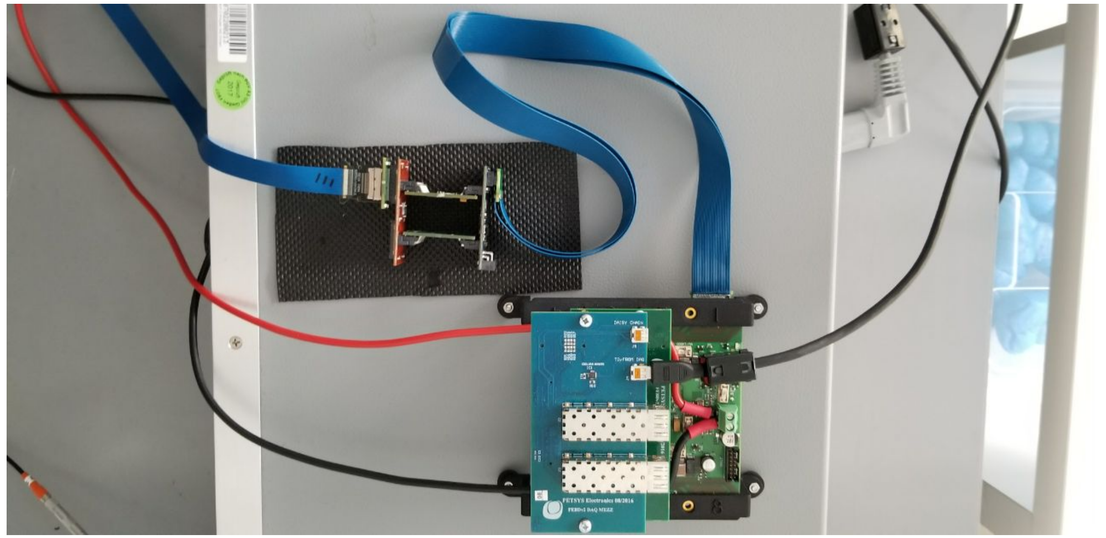
- Channels: 28,800 for EDD. For 1 quadrant ~7200 MCP-PMT channels
- Average photon rate: 17.3 MHz/MCP-PMT
- Time resolution: ~ 1 ns
- Maximum data rate for one ROM: 938 MB/s
- Average data rate: 280 MB/s
- Charge: ~10^6 e-/MCP-PMT.

FEM with 2 ASICs,128 ch



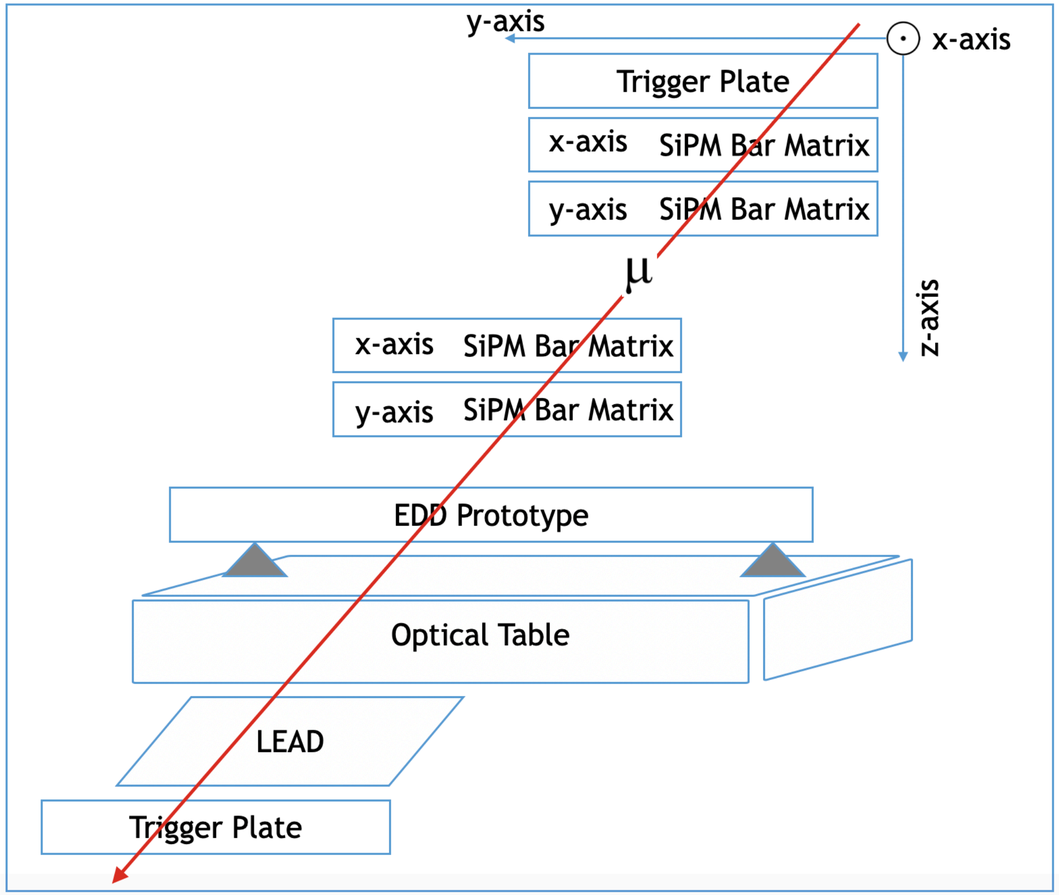
FEB_D_v2 board with 8 FEMs connect.

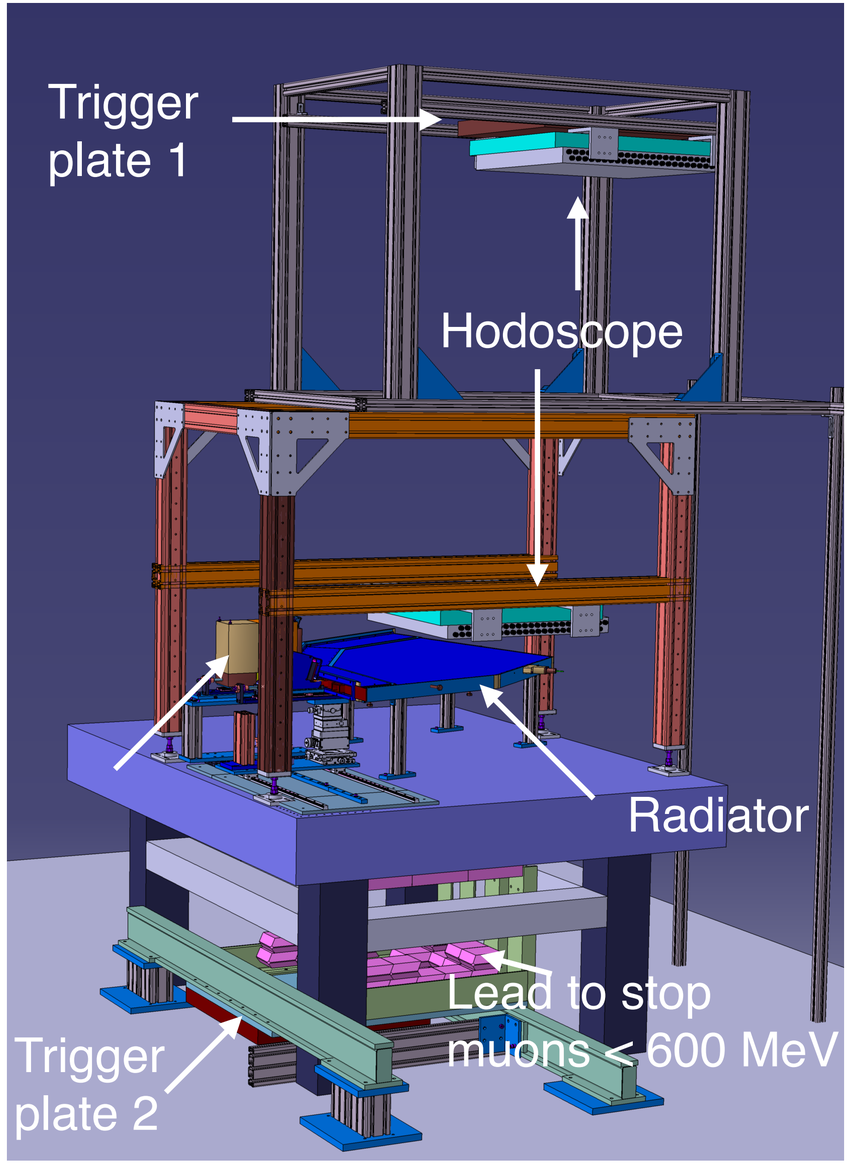


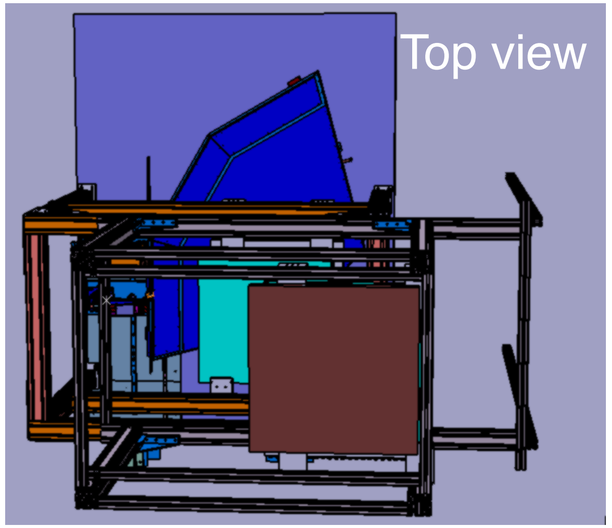


Giessen Cosmic Station (GCS) 3D Construction

Confirm the performance of the readout system and the prototype







GCS - Data Acquisition existing readout system

DAQ

Multimode Fiber optic patch Cord-24 MPO-MTP connection

Fiber optic cable

Fiber optic cable

TRIGGER PLATE 1

TOP X SiPM array

TOP Y SiPM array

FEM 2 ASICS

FEM 2 ASICS

FEB/D-v2 FPGA board (Positive sig)

Bottom X SiPM arr.

Bottom Y SiPM arr.

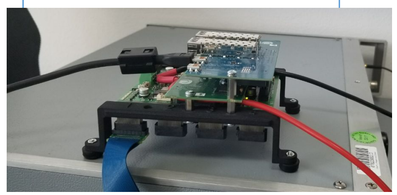
FEM 2 ASICS

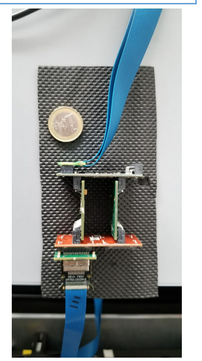
FEB/D-v2 FPGA board (Negative sig)

FEM 2 ASICS

MCP-PMT

RADIATOR





LEAD

TRIGGER PLATE 2

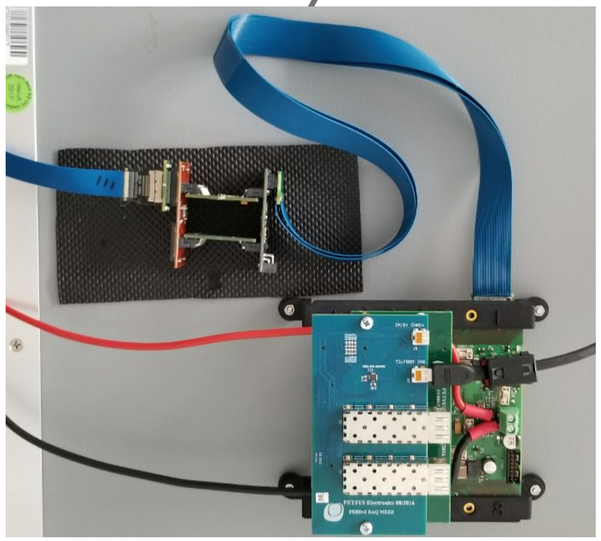
FEM 2 ASICS

uHDMI

uHDMI

fan-out-box

Different Scenarios - developing geometrical design

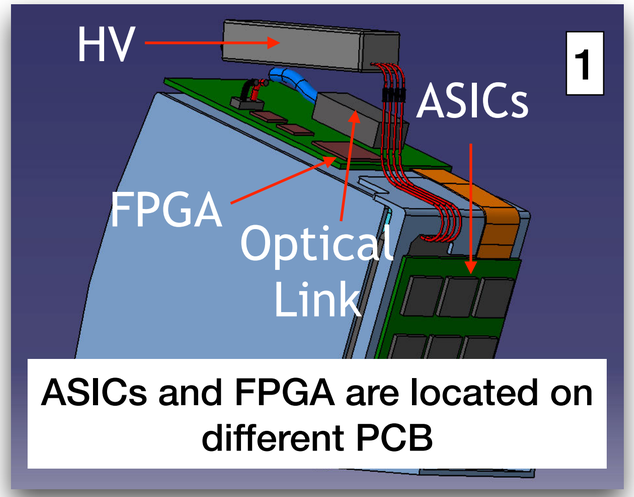


FPGA board + ASIC board

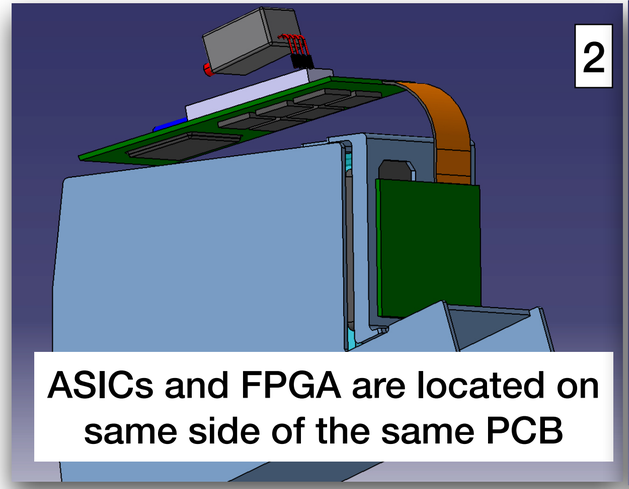
Excluding SiPM electronics

Implementing MCP-PMT

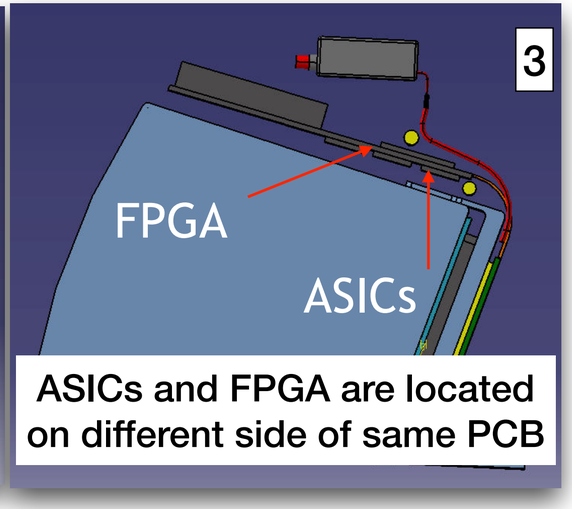
Custom-design PCB



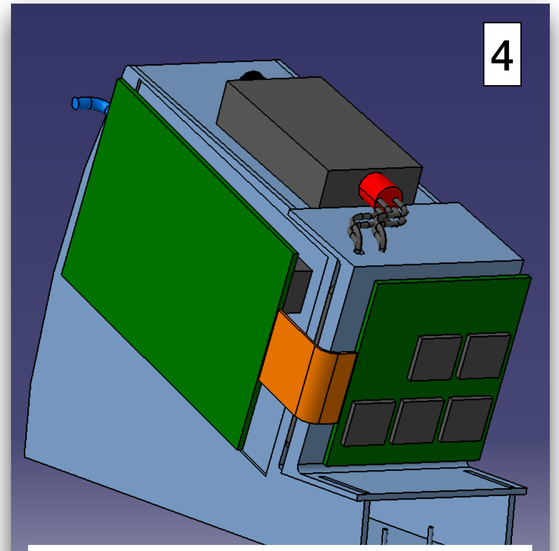
ASICs and FPGA are located on different PCB



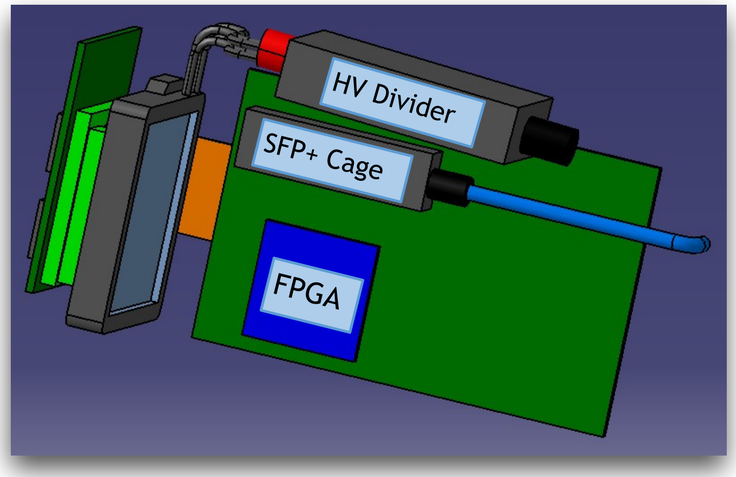
ASICs and FPGA are located on same side of the same PCB



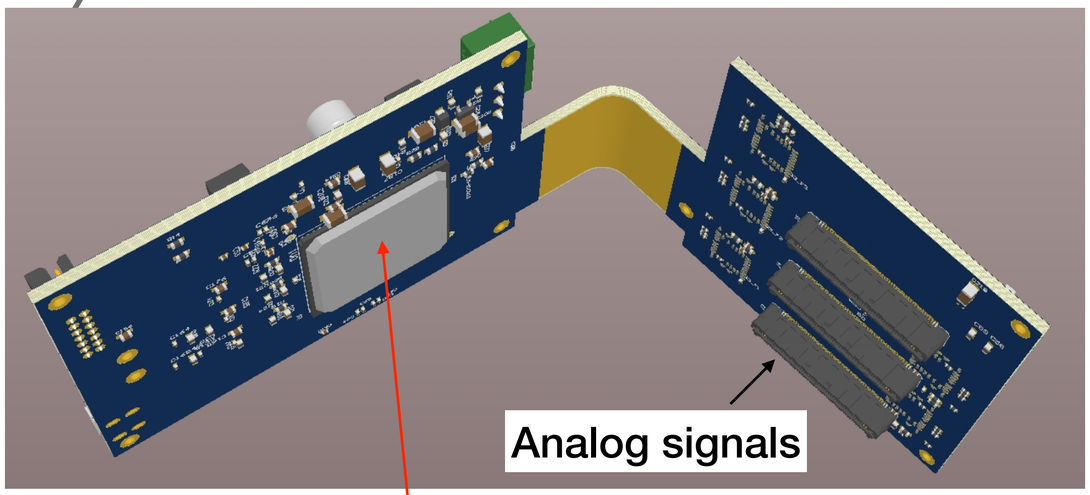
ASICs and FPGA are located on different side of same PCB

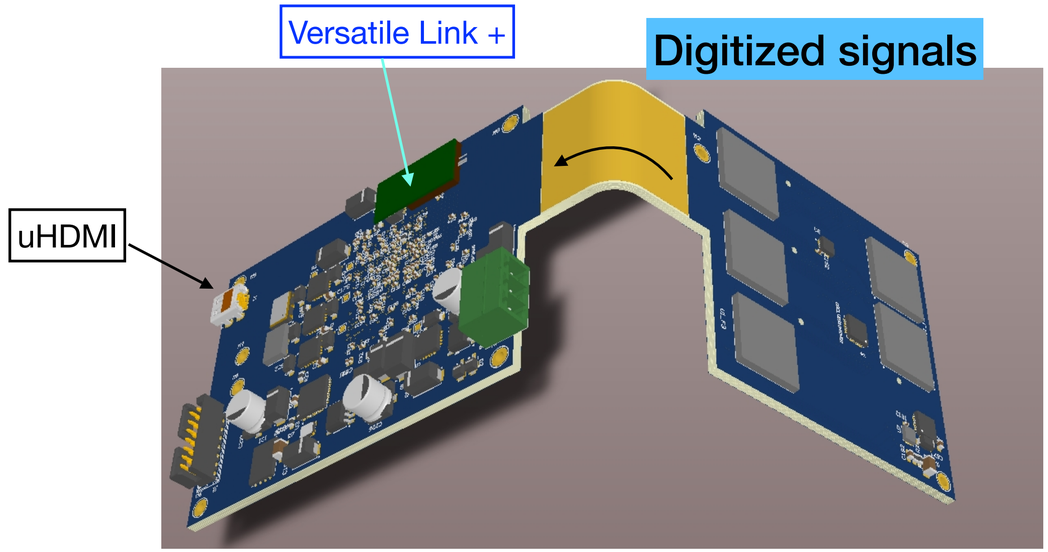


side alignment



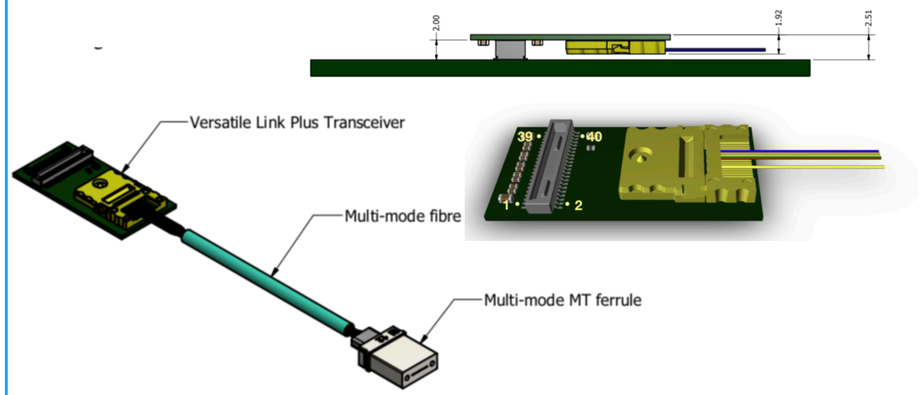
Custom PCB design for compact readout





- 5 ASICs, 1FPGA per rigid-flex board
- JTAG interface -> programming purposes or debugging.
- Optical link -> data transmission.
- SMC Q type -> clock and synchronization signals.
- FEASTMP
  - power for ASICs and FPGA (DC-DC converters)
  - slow control lines
  - return path for each ASIC data output link
  - temperature sensors

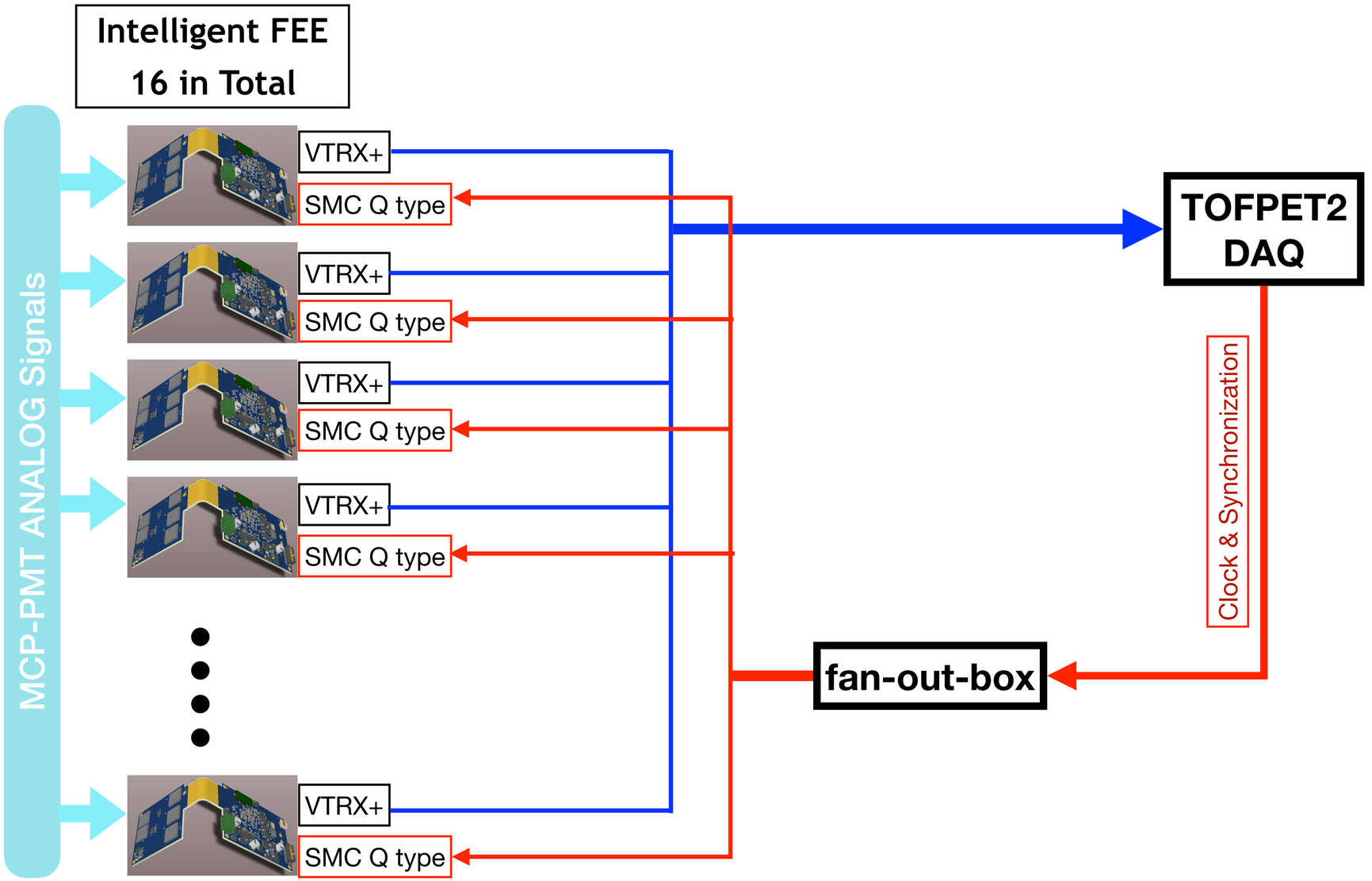
Versatile Link +: data transfer



- **FPGA:** high-performance **Xilinx Kintex-7FPGA** which is compatible with PANDA DAQ system.
  - Operating supply voltage 1.2- 3.3V
  - Data rate 6.6 Gb/s
- **uHDMI:** Clock & Synchronization for the current setup

Phase1 - Existing DAQ system

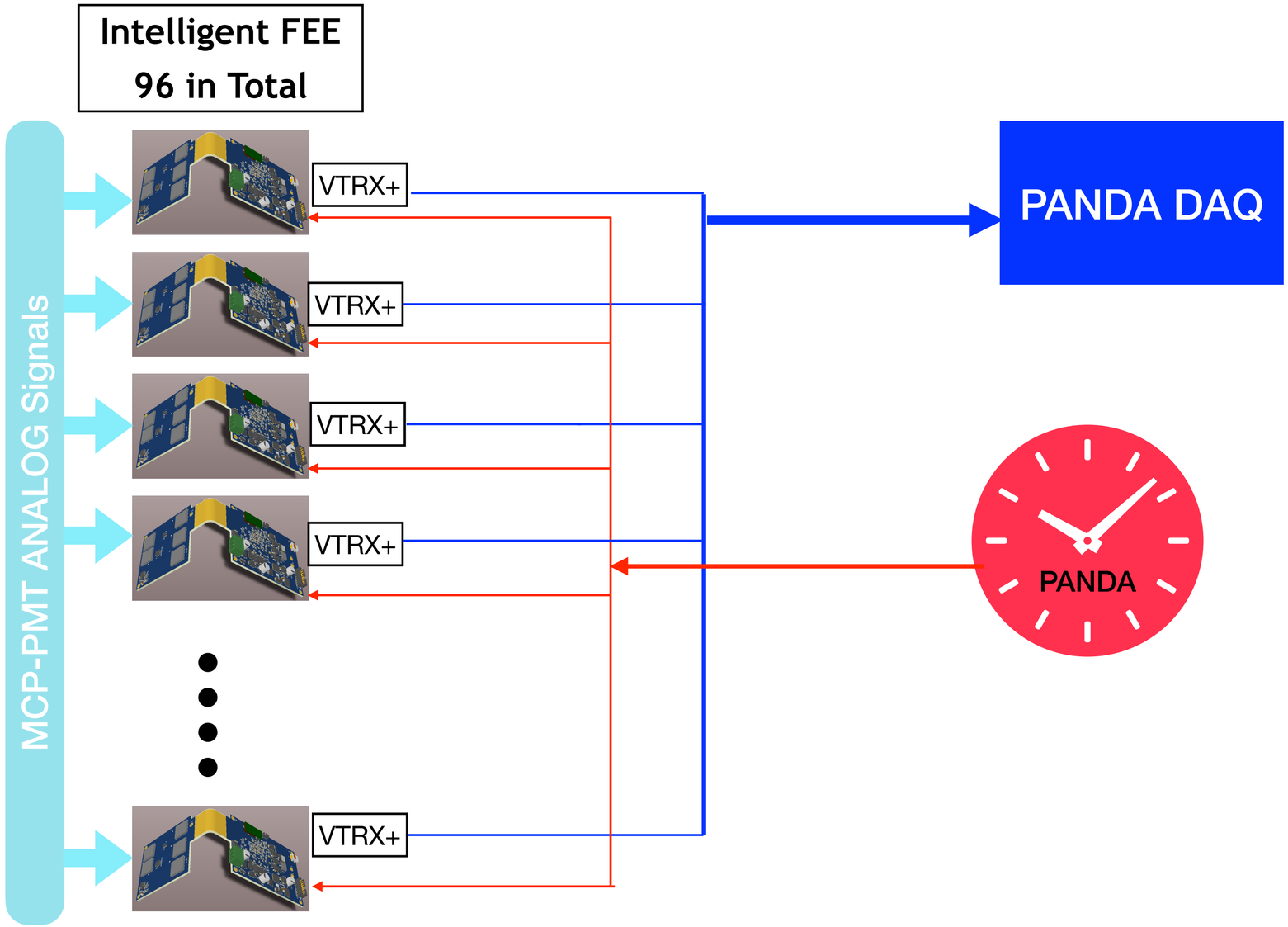
- 16 ROMs are planned to be used.
- Existing DAQ system (TOFPET2 DAQ) will be used for data taking, clock & synchronization
- Optical link (VTRX+)-> data transmission.



TWO POSSIBLE SCENARIOS FOR PHASE-2

Phase2 - Communication with central DAQ system

Scenario-1: All control signals are received via optical cable

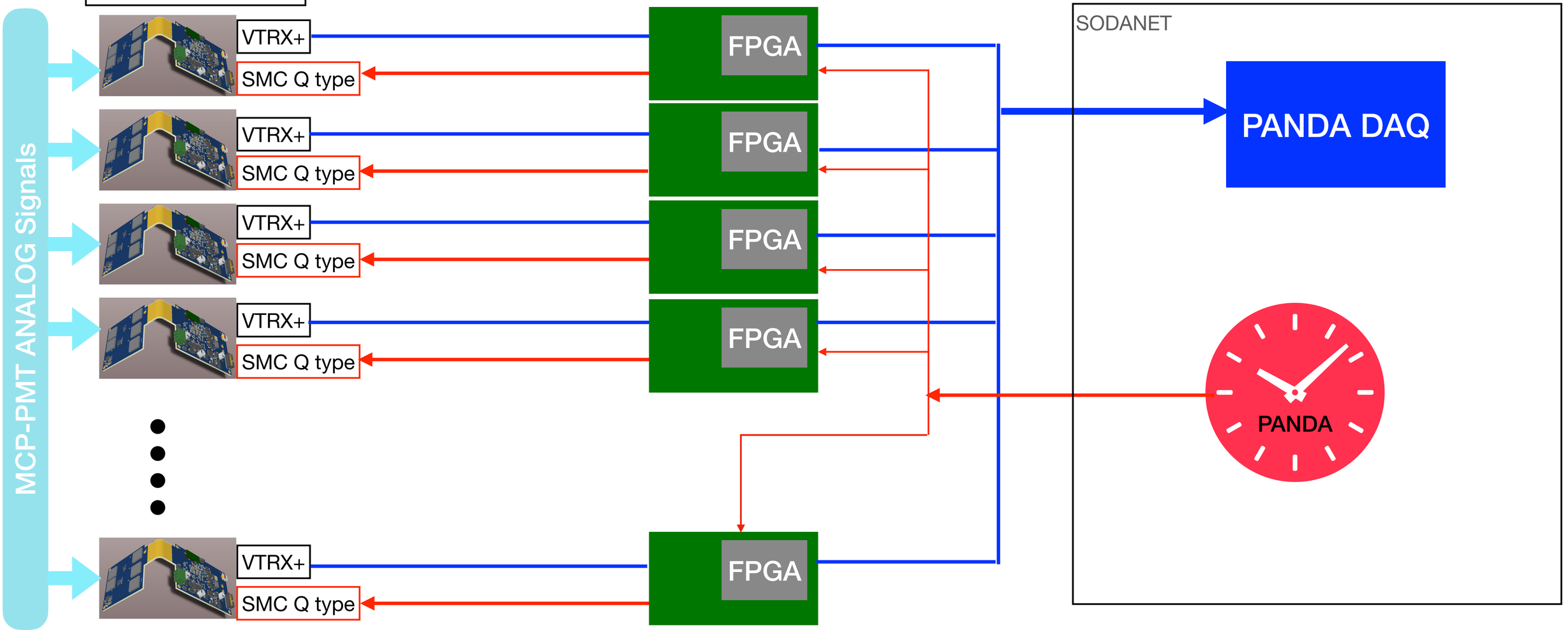


Phase2 - Communication with central DAQ system

Scenario-2: If Clock & Synchronization signals are transmitted as hardware signals

Intelligent FEE
96 in Total

ADAPTOR BOARD has to be designed
- Reformatting outgoing data into the SODANET format
- Receive SODANET clock & synchronization commands



Thanks!

ToFPET2 ASICs

- Designed in standard CMOS 110 nm technology.
- Signal amplification and discrimination for each of 64 independent channels.
- Separately configurable t1, t2 and energy thresholds for each channel.
- Rejects dark counts without triggering, allowing to handle large dark counts rates.
- Configurable charge integration time up to one microsecond.
- Quad-buffered TDCs and charge integrators for each channel. The first branch is used for timing measurement. The second branch can either be used for time-over-threshold (ToT) or charge measurement with a Wilkinson ADC.
- Dynamic range: 1500 pC.
- TDC time binning: 30 ps.
- Gain adjustment per channel in the charge branch: 1, 1/2, 1/4, 1/8.
- On-chip charge calibration pulse generator with 6-bit programmable amplitude.
- Main clock frequency: 160-200 MHz.
- Configurable digital data output over 1, 2, or 4 LVDS data links at 2x the main clock frequency and single data rate (SDR) or double data rate (DDR).
- Max output data rate per ASIC: 3.2 Gb/s.
- Max event rate per channel: 600 kevents, 80 bits per event.
- Power dissipation per channel: 8.2 mW, for the recommended settings.