

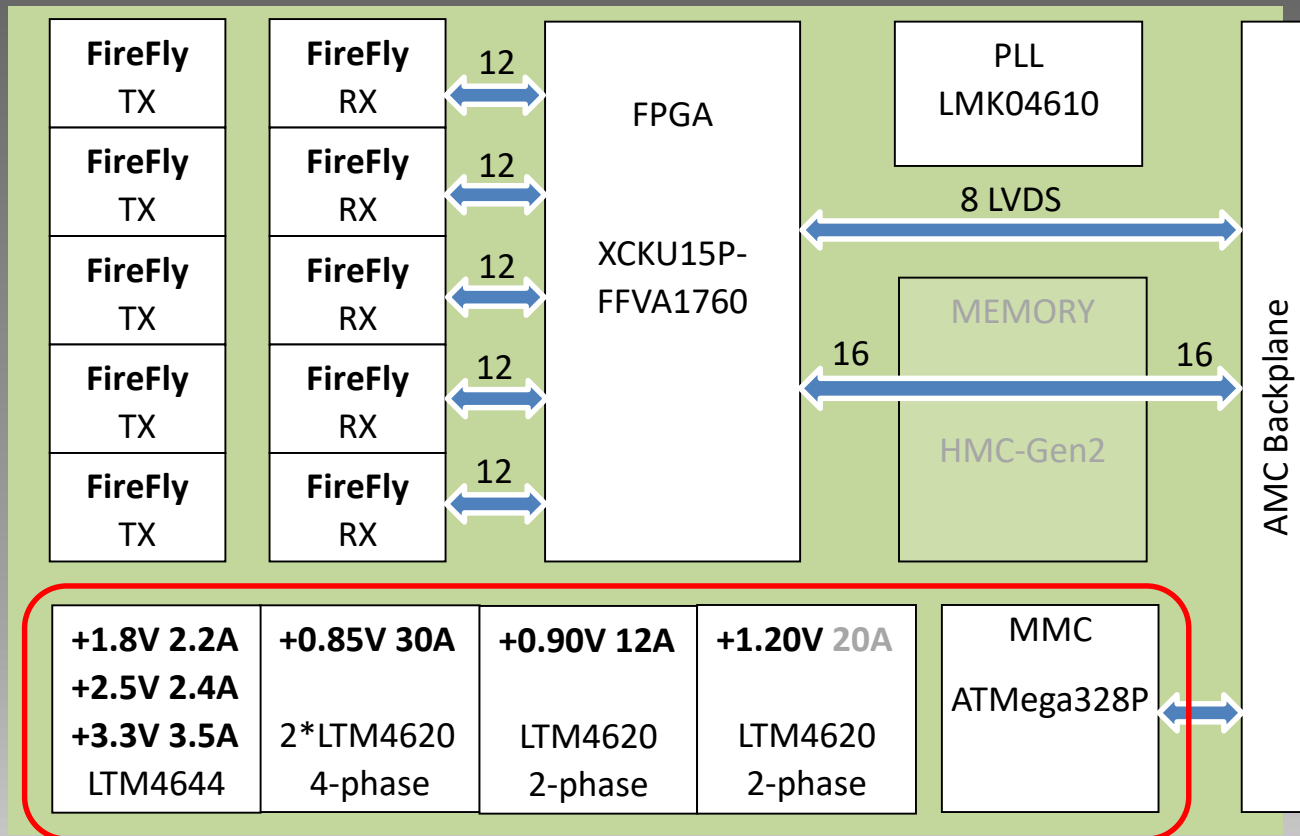


Status of the DAQ electronics for the PANDA-EMC

- PANDA DC
- LVDS ROB
- Crate Electronics
 - Backplane
 - Power Supplies
 - Crate Controller

Panda DC

60 x 14 Gb/s

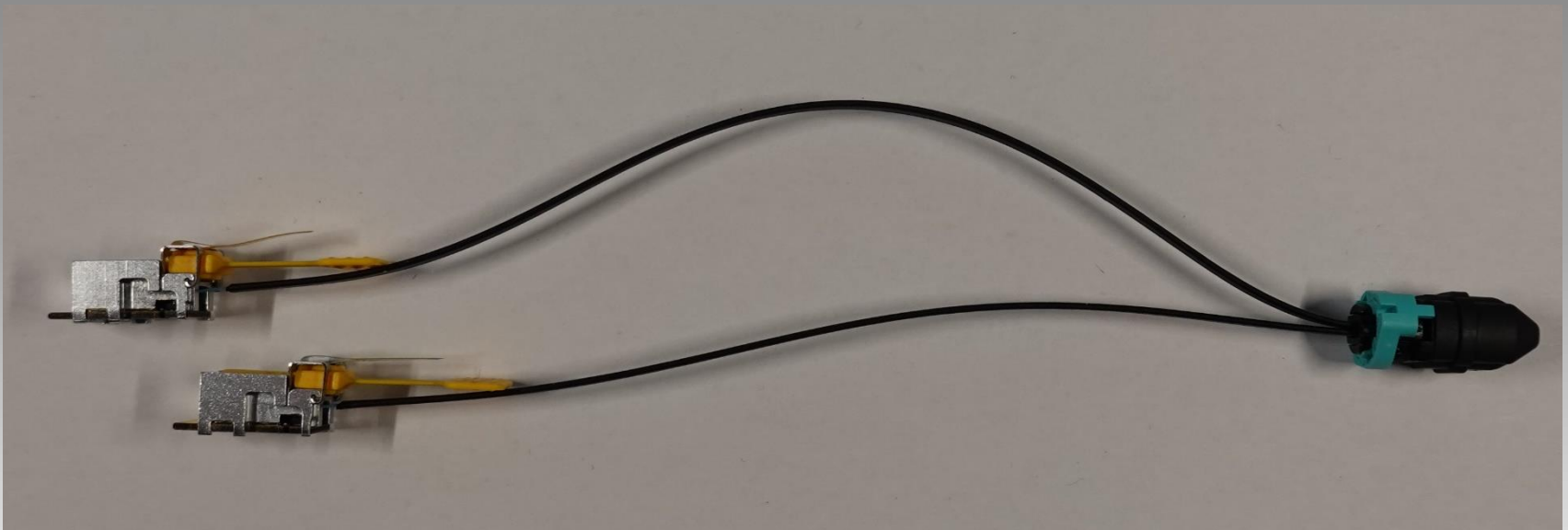


16 x 14 Gb/s

PANDA DC

Production and component stock

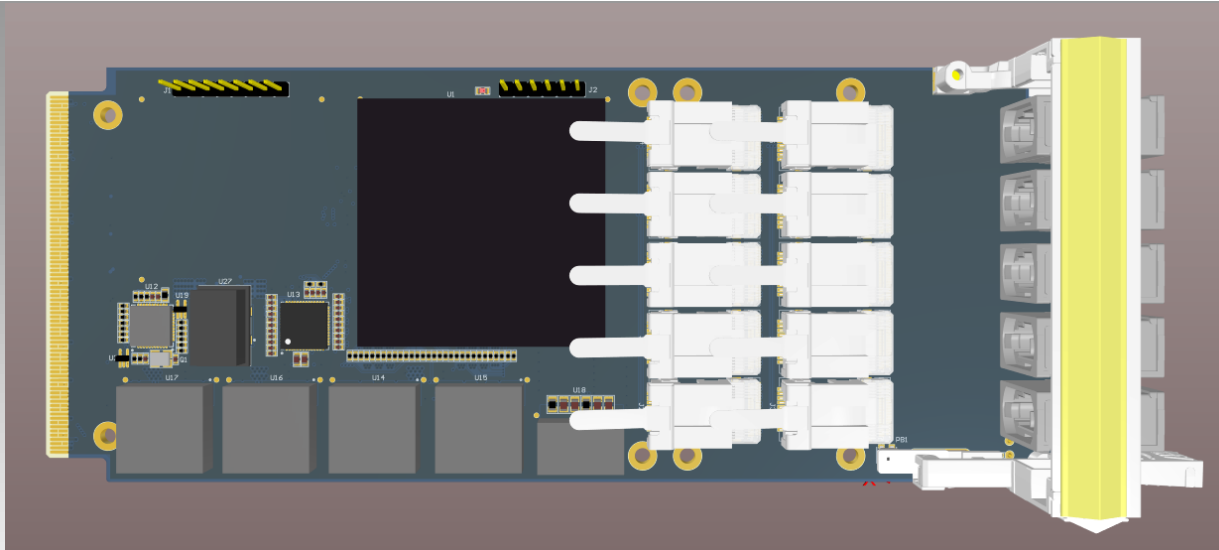
1. The device has been manufactured and delivered to Uppsala
2. All components purchased for 10 pcs.
3. The FireFly modules (non-standard pig-tail lengths) are purchased for two pcs. The rest is negotiated between Uppsala, CERN and Samtec.



PANDA DC

First tests

1. First tests show problems with power supply. They are being investigated in Warsaw (Semicon).
2. The second pcb has been assembled with power supply only and still shows problems, which are not trivial to understand.
3. We suspect problems are coming from the fragile laminate (Megtron 7)
4. A new Power test pcb (FR4) is on the way



LVDS DC

A readout board/data concentrator/feature extraction device

Input/output toward FE:

As many inputs/outputs as possible handling up to 600 Mbit/s

Optical interface (ECUO)

(FireFly™ Active Optical Micro Flyover System™)

or

Electrical interface (ECUE)

(FireFly™ Low Profile Micro Flyover System™ Cable Assembly)

or

Custom interface/connector

(to be developed on demand)

Input/output toward DAQ

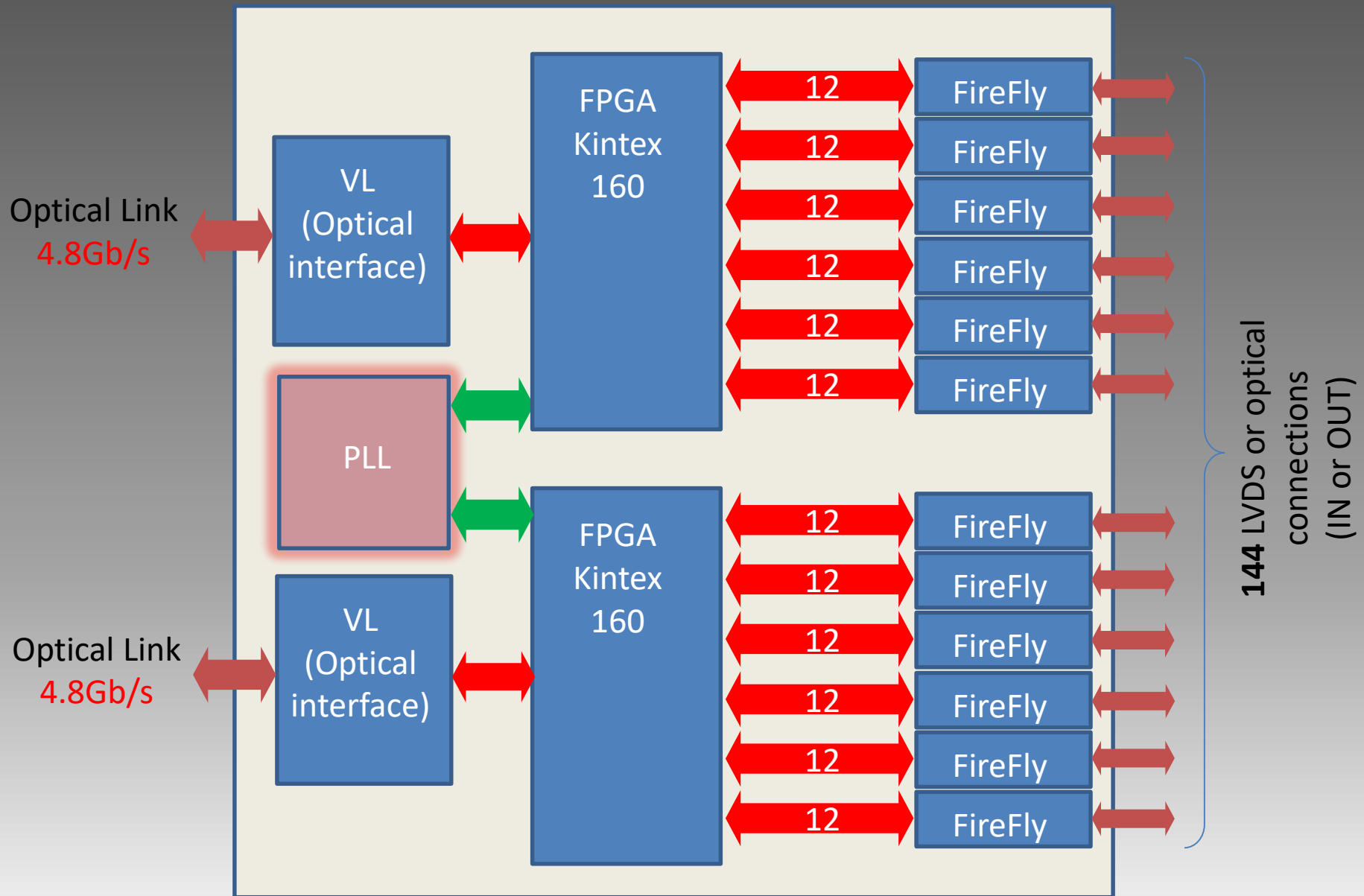
1 or 2 optical interfaces up to 4 Gbit/s

Optical interface:

SFP/VL compatible



LVDS DC



Optical interface:

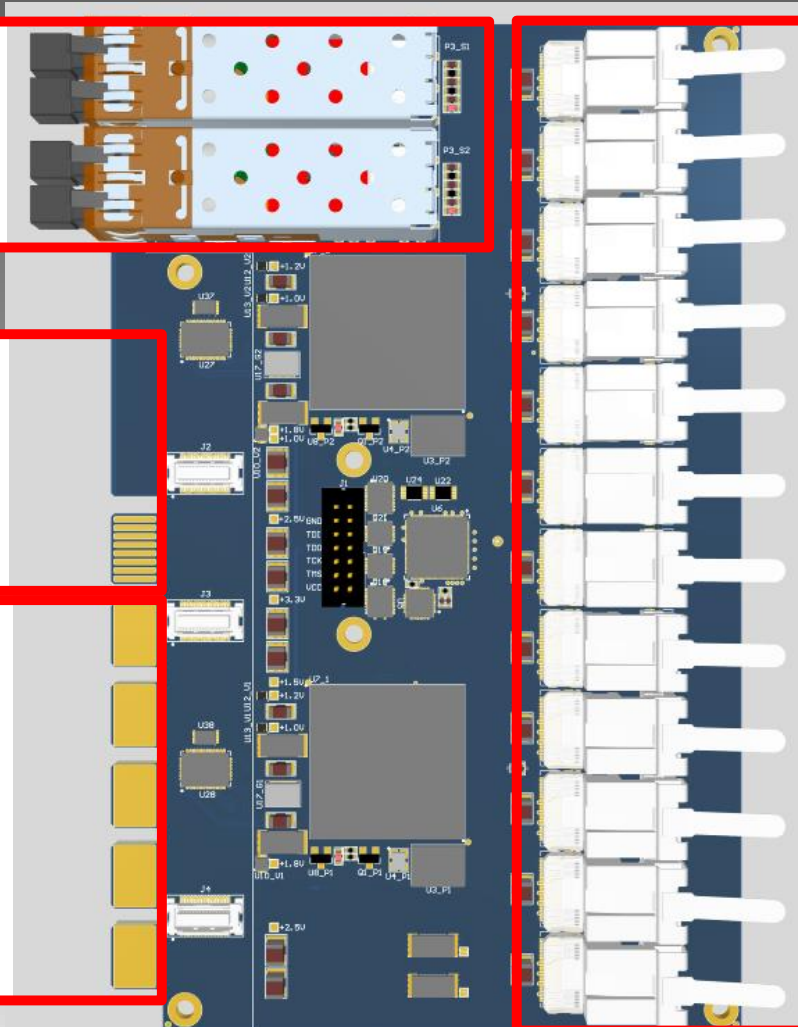
- SFP/VL compatible
- VL – obsolete

Electrical interface

- Configuration
- Reboot
- SEU handling
- Auxiliary

Power

- +1.0V – 4A (FPGA - INT)
- +1.5V – 1A (FPGA – GTX)
- +2.5V – 1A (FPGA – IO)
- +3.3V – 1A (PLL)
- +3.3V – 5A (FireFly)



I/O options:

1. Optical interface (ECUO)

(FireFly™ Active Optical Micro Flyover System™)

- 6 TX modules (72 ch.) and
- 6 RX modules (72 ch.)

2. Electrical interface (ECUE)

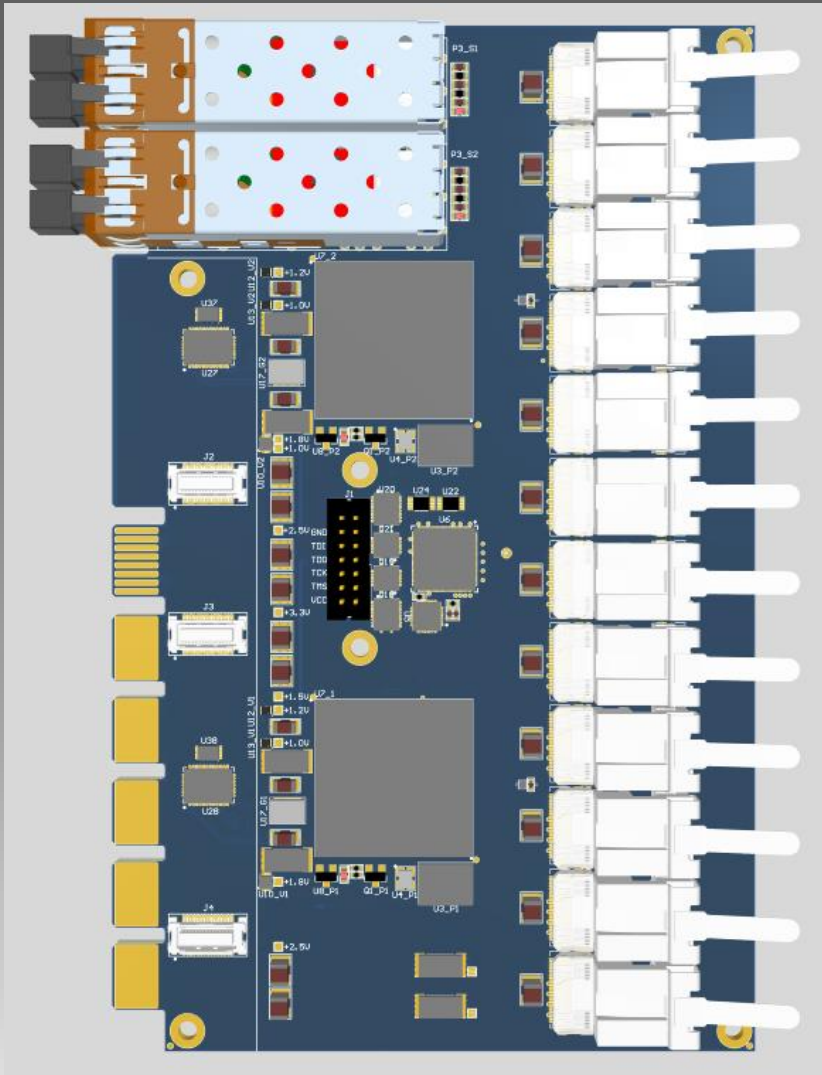
(FireFly™ Low Profile Micro Flyover System™ Cable Assembly)

- 12 Firefly modules
(144 LVDS channels)

3. Custom interface/connector

(to be developed on demand)

LVDS DC



Readout Board obtained from the 64-channel ADC for the EMC Forward Endcap

Issues, which were discussed:

- Electrical specifications
 - Power supply (internal/external)
 - SFP/VL/VL+
 - Additional functions
- Mechanical specifications
 - Encapsulation
 - Placement

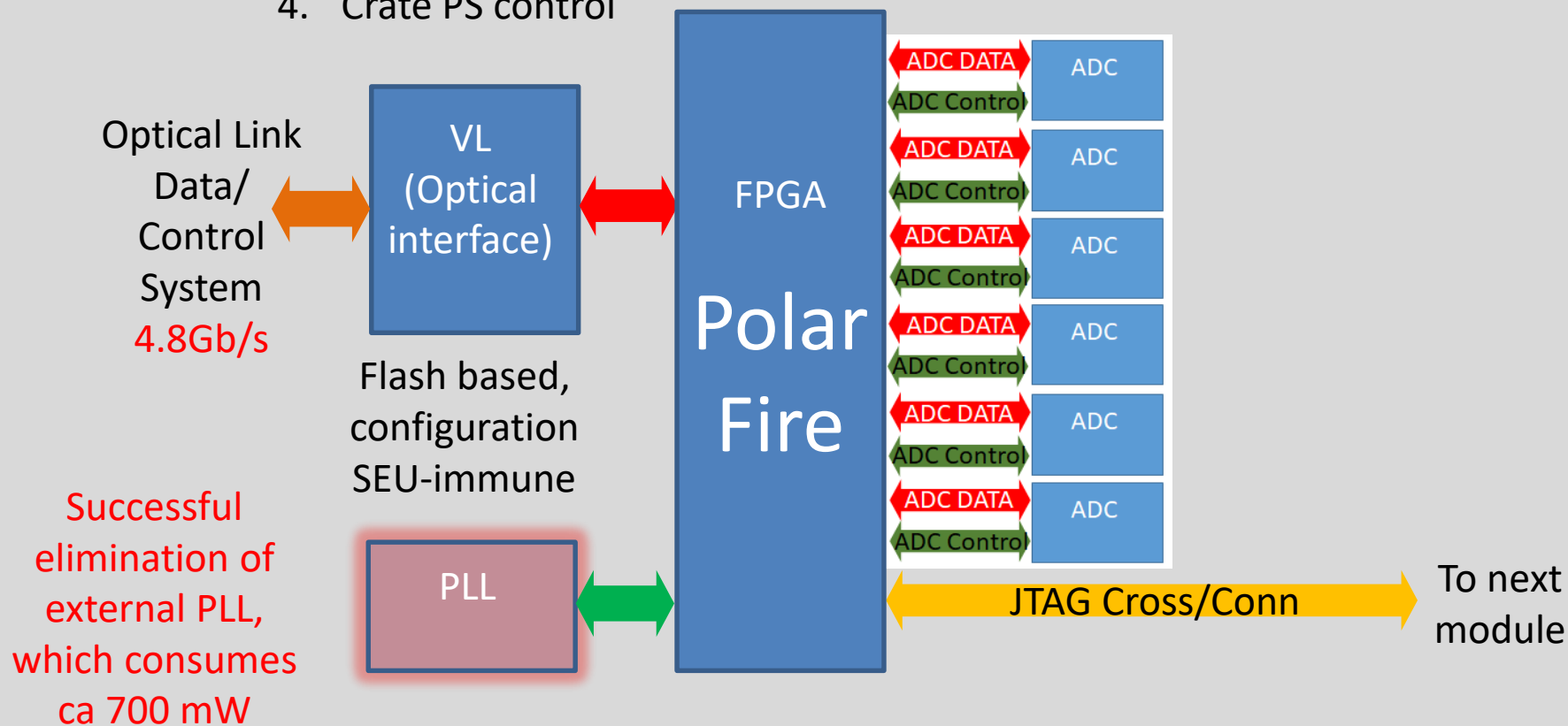
Status:

- Re-design completed
- **Ready for production**
- **Components need to be ordered before expected price “adjustment”**

CRATE CONTROLLER

Polar Fire – based Crate Controller

1. Direct JTAG configuration of individual ADCs
2. Reaction to SEU
3. Health control of ADCs (voltages, currents, temperatures)
4. Crate PS control





CRATE CONTROLLER

- Evaluation card with Libero development system

Libero - C:\Users\install\Desktop\sina\projects\Libero\Polar\XCVR - 5G-2G-PERFECT\XCVR.prj*

Project File Edit View Design Tools Help

Design Flow

Top Module(root): TOP

Active Synthesis Implementation: CHIPSCOPE

Tool

- Create Design
 - Create SmartDesign
 - Create HDL
 - Create SmartDesign Testbench
 - Create HDL Testbench
 - Verify Pre-Synthesized Design
 - Simulate
- Constraints
 - Manage Constraints
- Implement Design
 - Open Netlist Viewer
- Synthesize
 - Verify Post-Synthesized Design
 - Generate Simulation File
 - Simulate
- Place and Route
 - Verify Post Layout Implementation
 - Verify Timing
 - Open SmartTime
 - Verify Power
 - Open SSN Analyzer
- Configure Hardware
 - Programming Connectivity and Interface
 - Configure Programmer
 - Select Programmer
- Program Design
 - Generate FPGA Array Data
 - Configure Design Initialization Data and Memories
 - Generate Design Initialization Data
 - Configure I/O States During JTAG Programming
 - Configure Programming Options
 - Configure Security
 - Generate Bitstream
 - Configure Actions and Procedures
 - Run PROGRAM Action
 - Program SPI Flash Image
 - Generate SPI Flash Image
 - Run PROGRAM_SPI_IMAGE Action
- Debug Design

Design Flow Design Hierarchy Stimulus Hierarchy Catalog Files

Message

Messages Errors Warnings Info Manage suppressed messages

Message

- Forward annotating clock ident_coreinst.comm_block_INST.dr2_tck on drive pins would add that clock to 1363 clock pins including ide
- Forward annotating clock ident_coreinst.comm_block_INST.dr2_tck on input pins
- Found clock ident_coreinst.comm_block_INST.dr2_tck with period 1000.00ns
- Found inferred clock PF_XCVR_ERM_C1_I_XCVR_PF_XCVR[LANE0_tx_rclkint_input_net_inferred_clock with period 10.00ns. Please declare

Place and Route [TOP]

Please refer to the log file for details about 7 Info(s)

Generate Bitstream [TOP]

Message Log Cores

X Find: Next Previous Find All Search in: Match case Match whole word

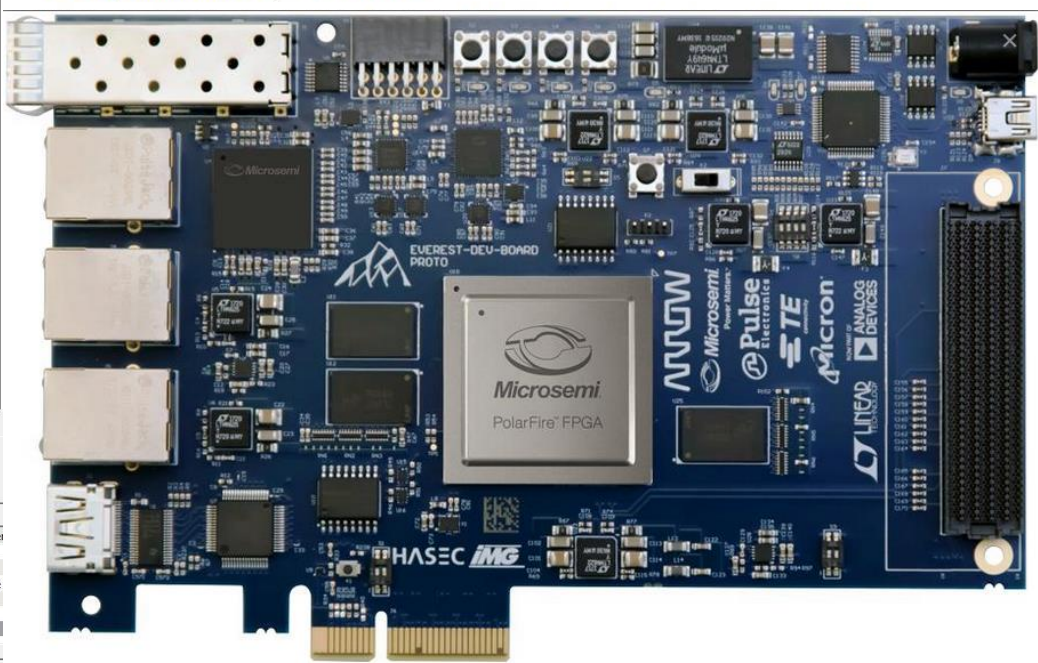
Links

- Welcome to Libero SoC
- Libero SoC Quickstart
- Libero SoC Interface Description
- Libero SoC Release Notes on the Web
- Libero Tutorials
- Product Tutorials
- Training Webcasts
- Microsemi SoC Website

Libero SoC Quickstart

What would you like to do?

- View the Libero SoC Design Flow (link opens Design Flow summary topic in Help) - Use the links below to create your design.
- Create a SmartDesign Component - Enables you to take configured cores, IP cores, macros from the Catalog, and user-created HDL source files and instantiate them into your design.
- Create HDL - Creates a new HDL file and opens it in the HDL editor; useful if you prefer to work in HDL in conjunction with SmartDesign.
- Import existing files into this project.
- View/Configure Firmware Cores - Opens the Firmware view



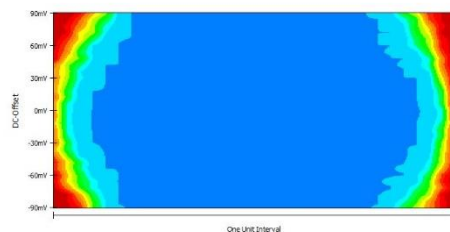
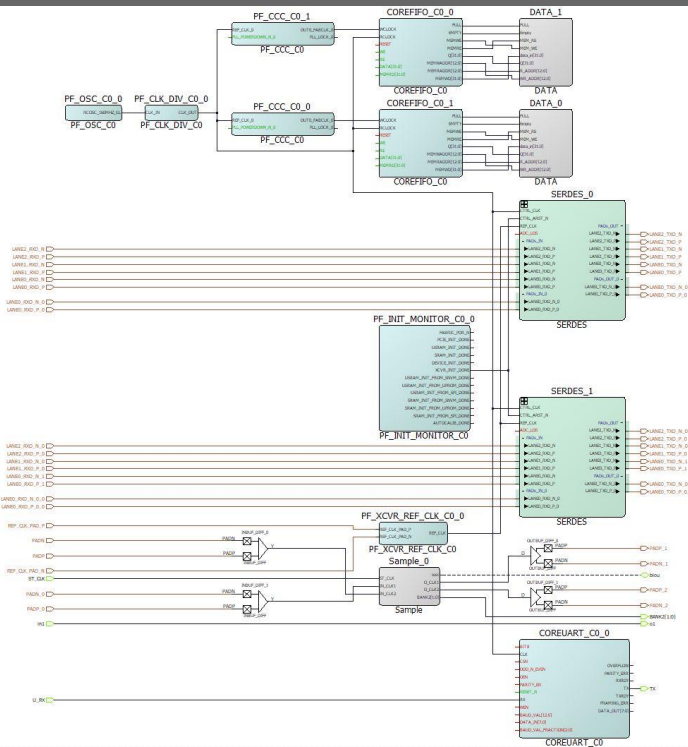
Fam: PolarFire Part: MPF300T-1FCG1152E VHDL

A project containing 6 channels 2Gb/s and 2 channels 6.25 Gb/s (**time deterministic**)

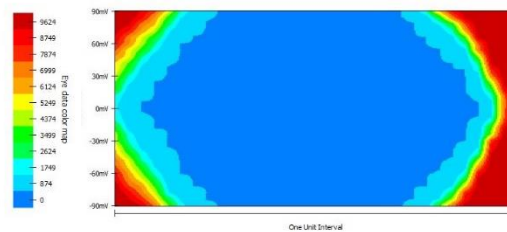
Status

Firmware:

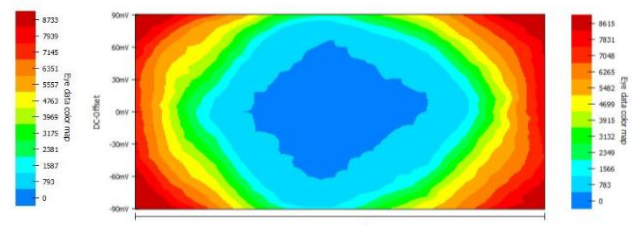
- Canvas project in Libero is ready (mux 3 x 2 Gbit/s → 6.25 Gbit/s)
- Successful elimination of external PLL, which consumes ca 700 mW
- Successful time deterministic tests of bilateral communication to ADC



2 Gb/s

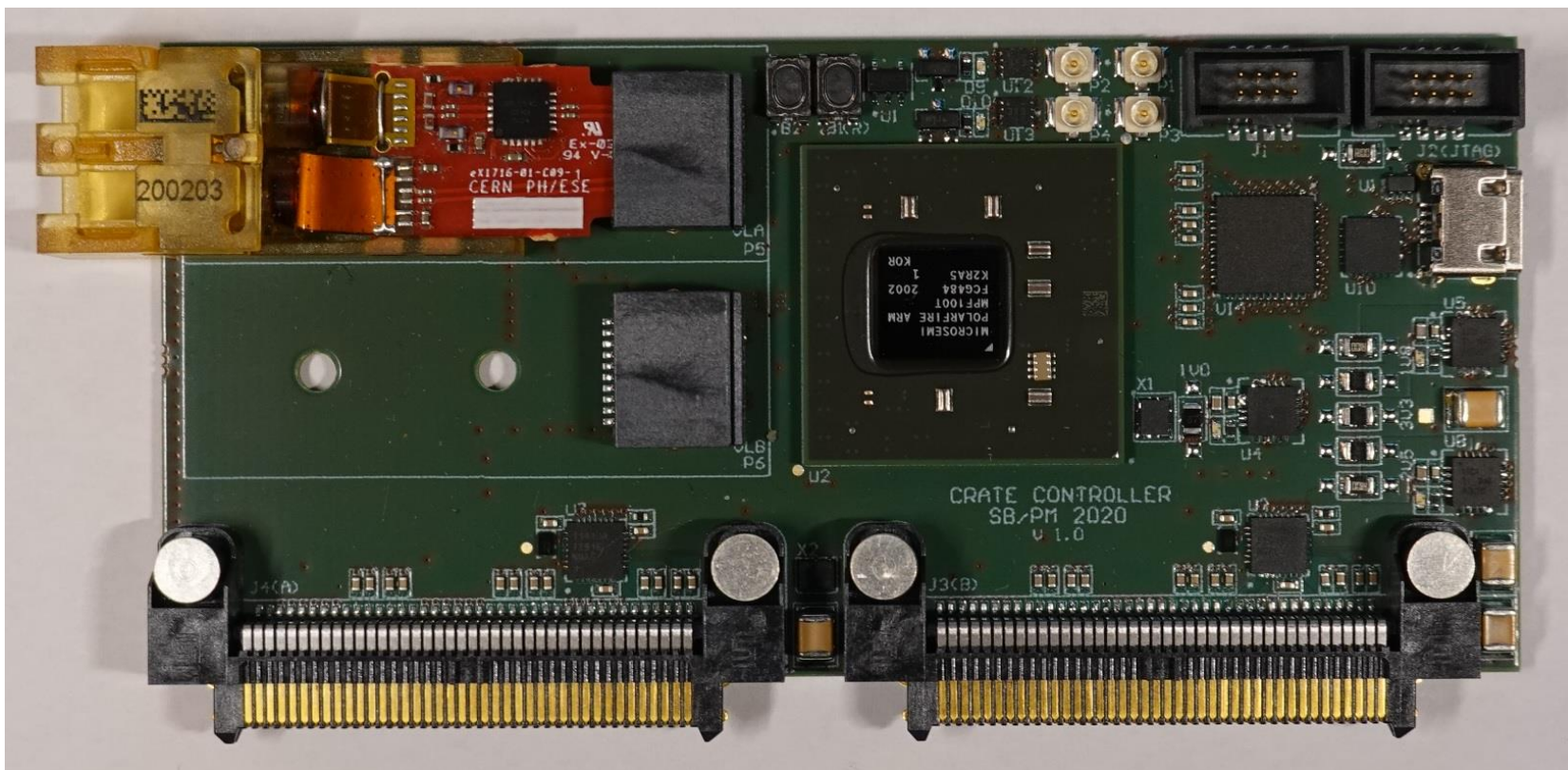


6.25 Gb/s



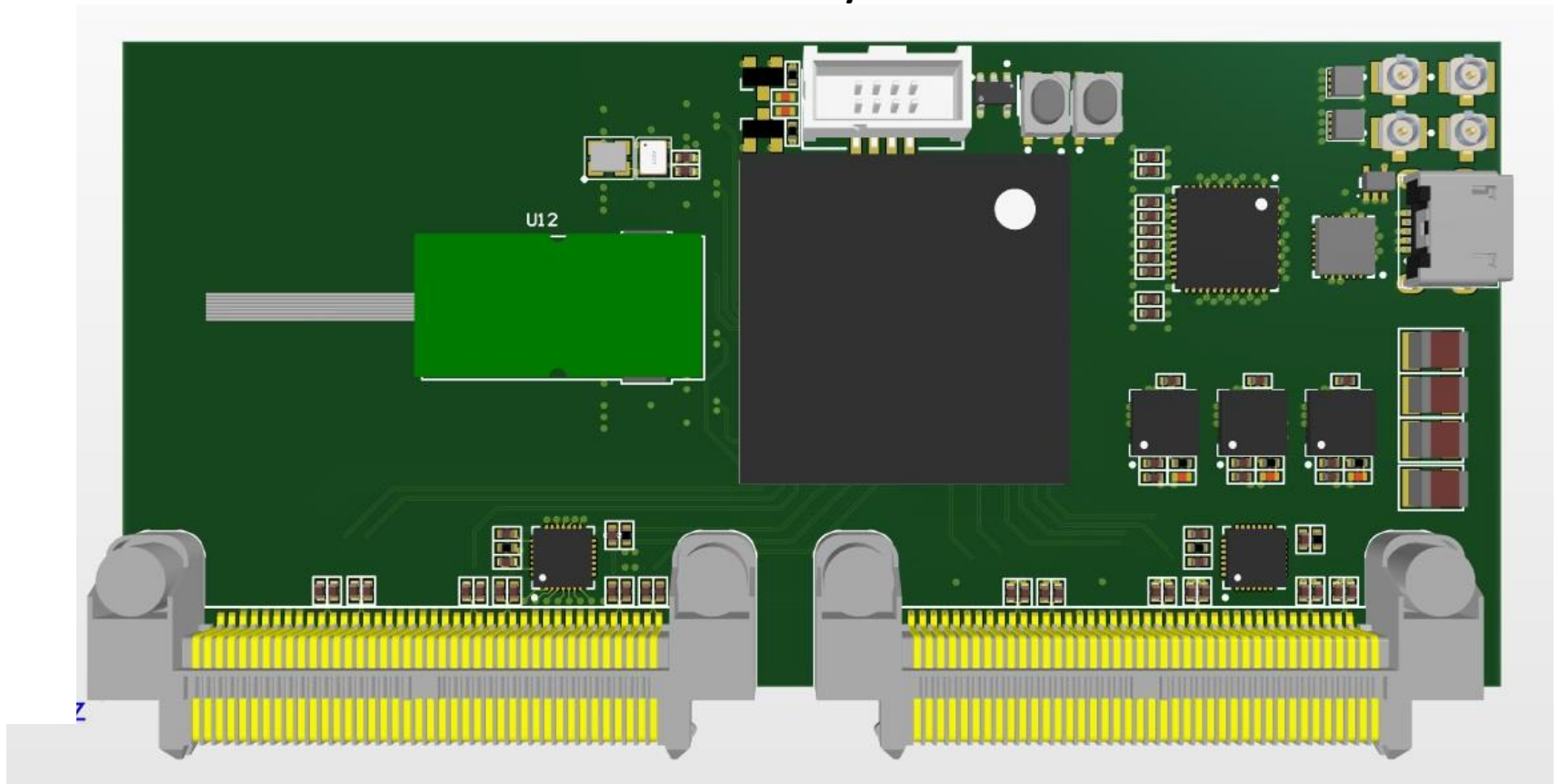
10 Gb/s

Dual channel VTRx
Test version, 2 x 4,8 Gb/s



The first prototype with VTRx

**Future plans:
Dual channel VTRx+
2 x 10 Gb/s**



Old artwork of the future Crate Controller
VTRx+ will be produced 2021



- ADC – production for Shashlik, tests – Jan..Aug 22
 - Production needs quite urgent decision due to planned component price changes
- Ev. ADC redesign for barrel – Aug 21..Aug 22
 - Decision depends on the Pulse Detection Asic progress
- PANDA DC – test Jan21..Dec 22 master, phd
 - Basic debugging started, manpower will be needed in the future
- - Second prototype, volume Aug 21..Aug 22
 - Based on the outcome of the first tests
- LVDS DC – tests Apr 21..Aug 22
 - Device was discussed and approved by the collaboration. It will go to prototype production
 - FPGA for the bulk needs to be ordered until April 2021
- Crate controller – Jan..Jun 21 – master
 - Debugging started, but the envisaged master student has left. I will continue anyhow.
- Power Supply – tests Feb 21
 - Unclear situation, since new call for experiments at AGOR left no time for an application
- Backplane – Jun..Dec 21
 - New backplane is ready and will be sent along with the LVDS-DC for production



Thank You !