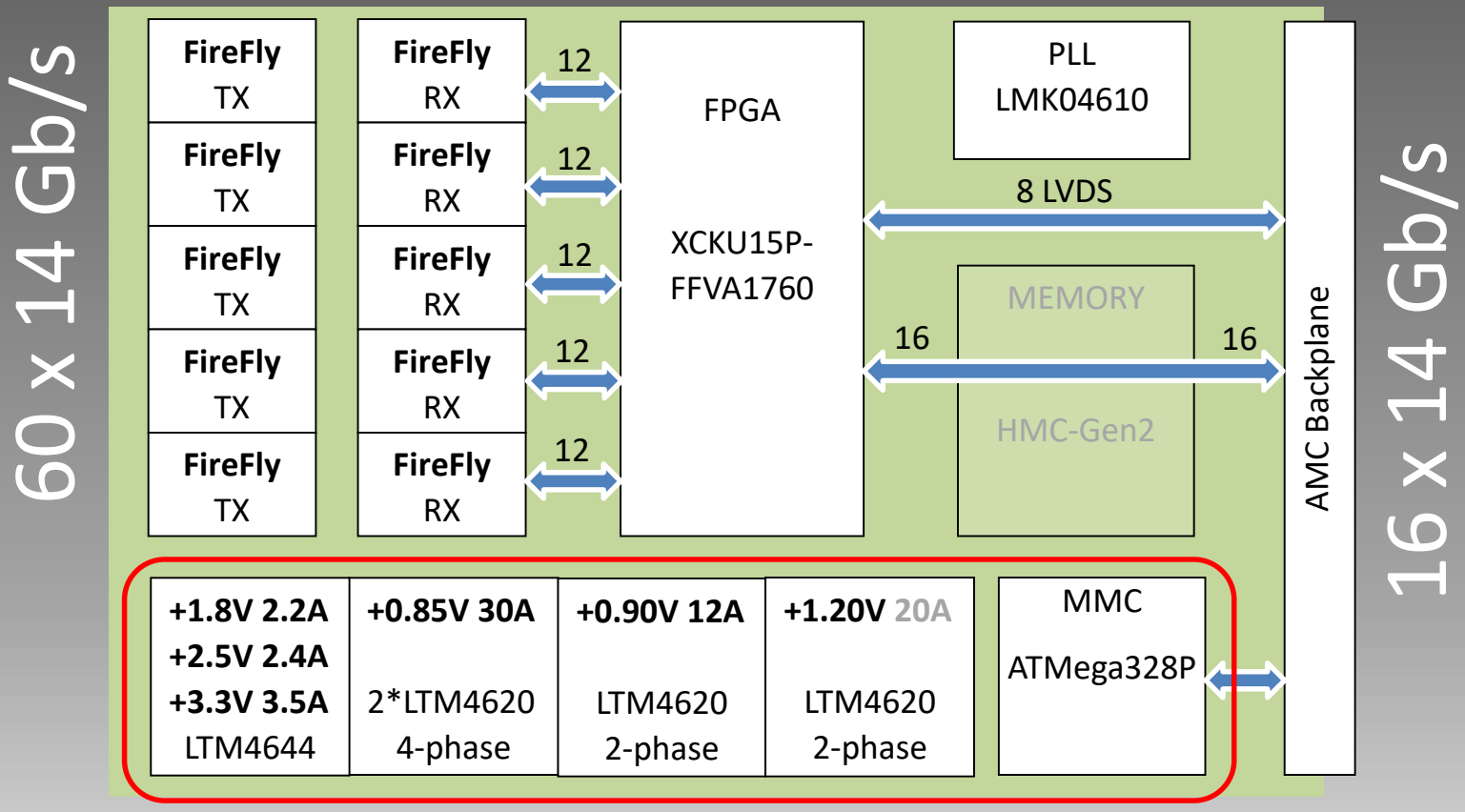
Status of the DAQ electronics for the PANDA-EMC

- PANDA DC
- LVDS ROB
- Crate Electronics
  - Backplane
  - Power Supplies
  - Crate Controller

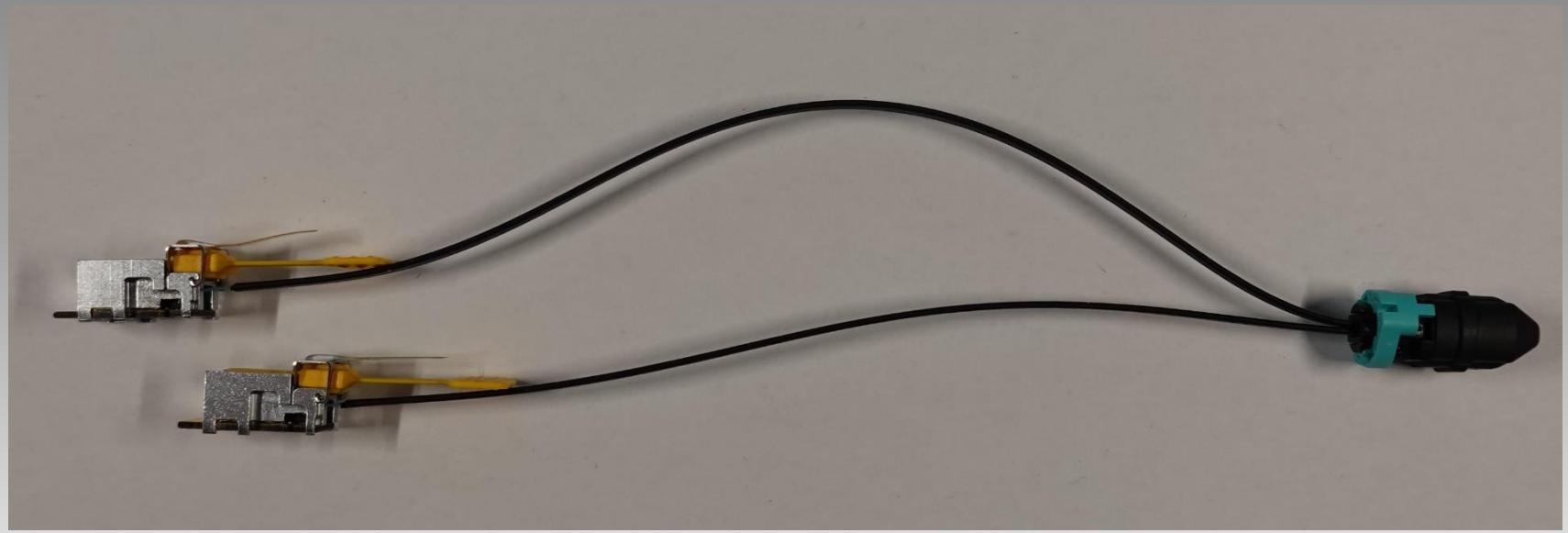
Panda DC


60 x 14 Gb/s
FireFly TX
FireFly TX
FireFly TX
FireFly TX
FireFly TX
FireFly RX
FireFly RX
FireFly RX
FireFly RX
FireFly RX
12
12
12
12
12
FPGA
XCKU15P-FFVA1760
PLL LMK04610
8 LVDS
MEMORY
HMC-Gen2
16
16
AMC Backplane
16 x 14 Gb/s
+1.8V 2.2A
+2.5V 2.4A
+3.3V 3.5A
LTM4644
+0.85V 30A
2*LTM4620
4-phase
+0.90V 12A
LTM4620
2-phase
+1.20V 20A
LTM4620
2-phase
MMC
ATMega328P

PANDA DC

Production and component stock

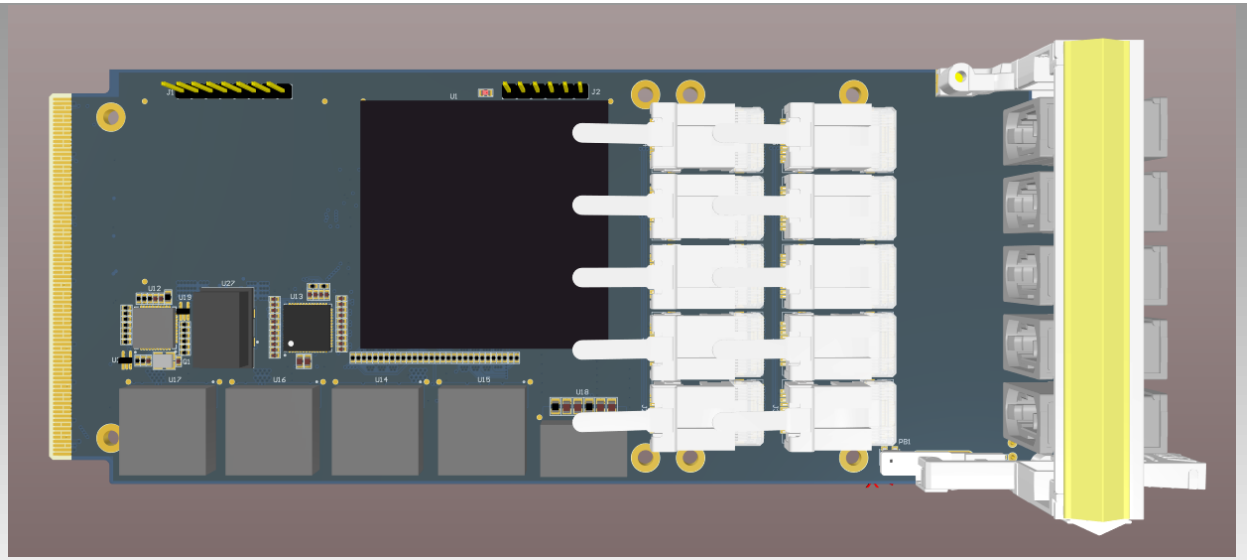
1. The device has been manufactured and delivered to Uppsala
2. All components purchased for 10 pcs.
3. The FireFly modules (non-standard pig-tail lengths) are purchased for two pcs. The rest is negotiated between Uppsala, CERN and Samtec.



PANDA DC

First tests

1. First tests show problems with power supply. They are being investigated in Warsaw (Semicon).
2. The second pcb has been assembled with power supply only and still shows problems, which are not trivial to understand.
3. We suspect problems are coming from the fragile laminate (Megtron 7)
4. A new Power test pcb (FR4) is on the way



LVDS DC

A readout board/data concentrator/feature extraction device

Input/output toward FE:

As many inputs/outputs as possible handling up to 600 Mbit/s

Optical interface (ECUO)
(FireFly™ Active Optical Micro Flyover System™)

or

Electrical interface (ECUE)
(FireFly™ Low Profile Micro Flyover System™ Cable Assembly)

or

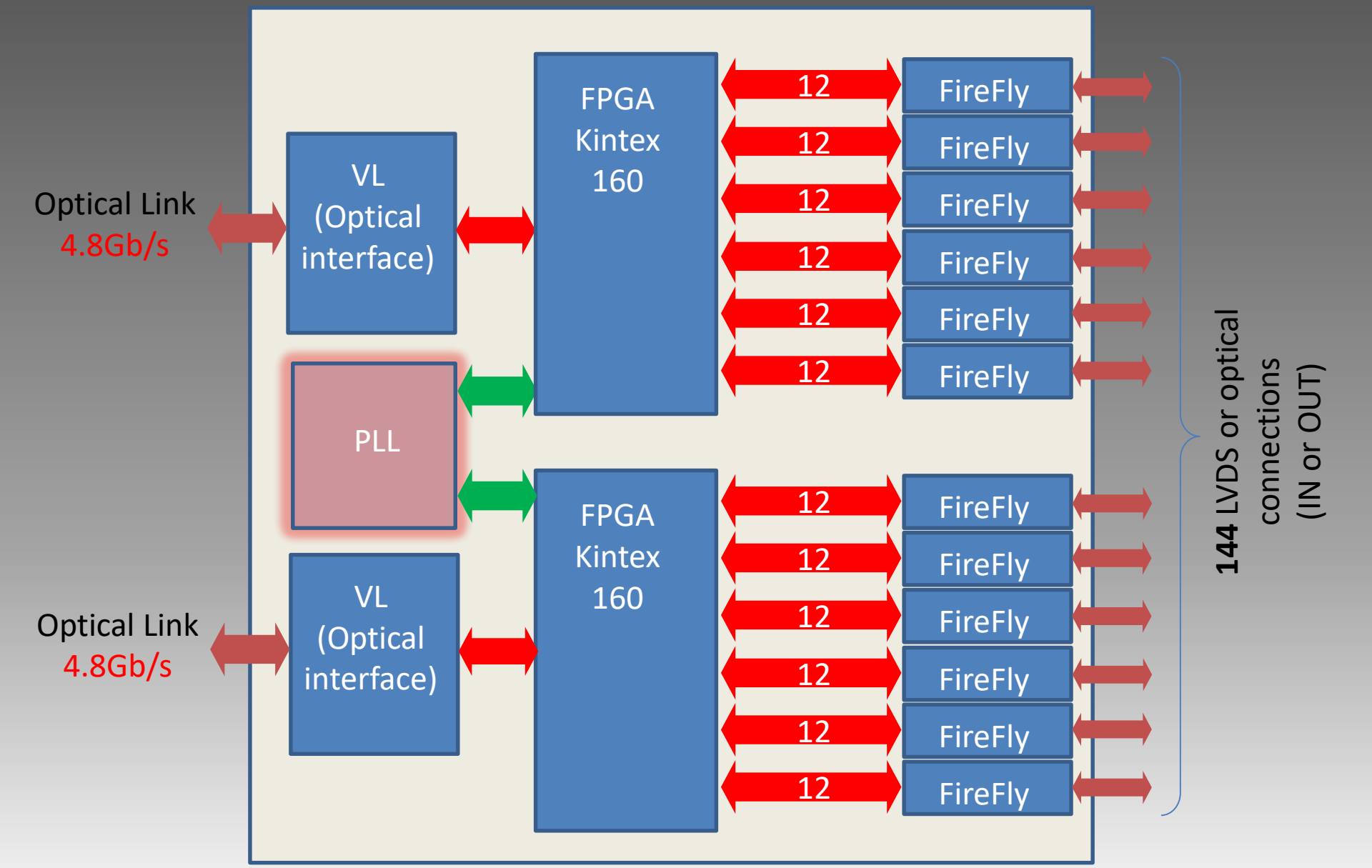
Custom interface/connector
(to be developed on demand)

Input/output toward DAQ

1 or 2 optical interfaces up to 4 Gbit/s

Optical interface:
SFP/VL compatible

LVDS DC


Optical Link
4.8Gb/s
VL
(Optical
interface)
PLL
FPGA
Kintex
160
12
FireFly
Optical Link
4.8Gb/s
VL
(Optical
interface)
FPGA
Kintex
160
12
FireFly
144 LVDS or optical
connections
(IN or OUT)

LVDS DC

Optical interface:

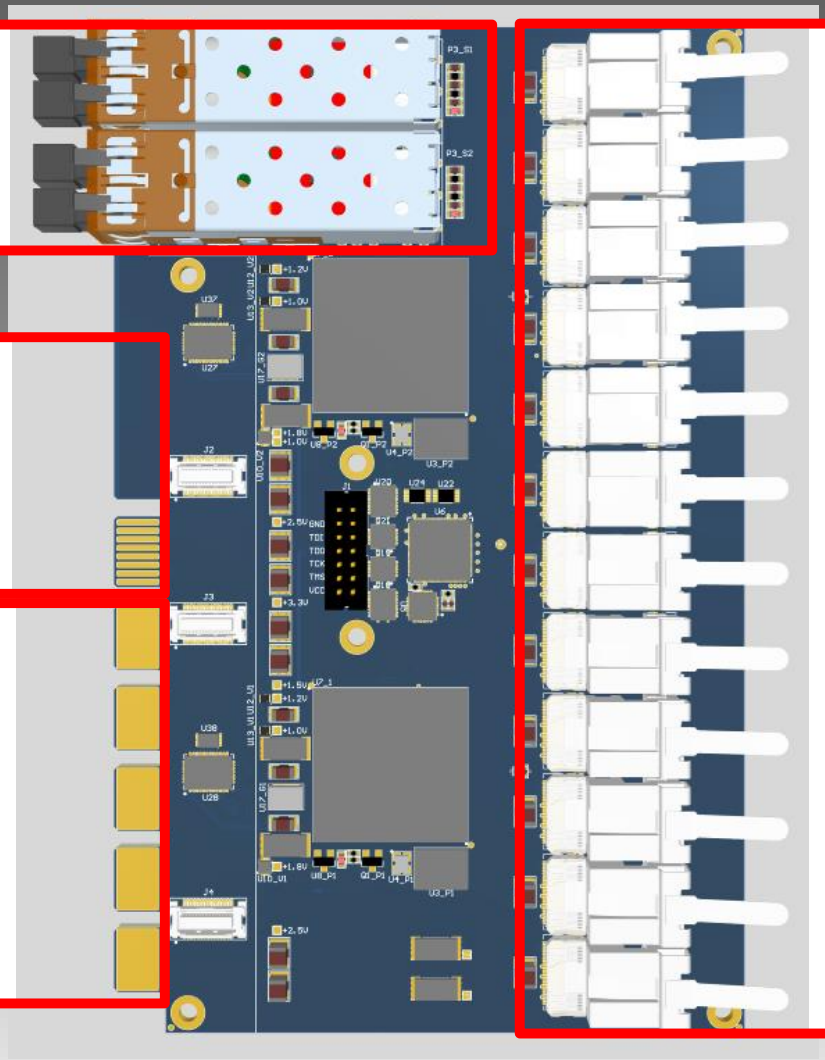
- SFP/VL compatible
- VL – obsolete

Electrical interface

- Configuration
- Reboot
- SEU handling
- Auxiliary

Power

+1.0V – 4A (FPGA - INT)
+1.5V – 1A (FPGA – GTX)
+2.5V – 1A (FPGA – IO)
+3.3V – 1A (PLL)
+3.3V – 5A (FireFly)



I/O options:

1. Optical interface (ECUO)

(FireFly™ Active Optical Micro Flyover System™)

- 6 TX modules (72 ch.) and
- 6 RX modules (72 ch.)

2. Electrical interface (ECUE)

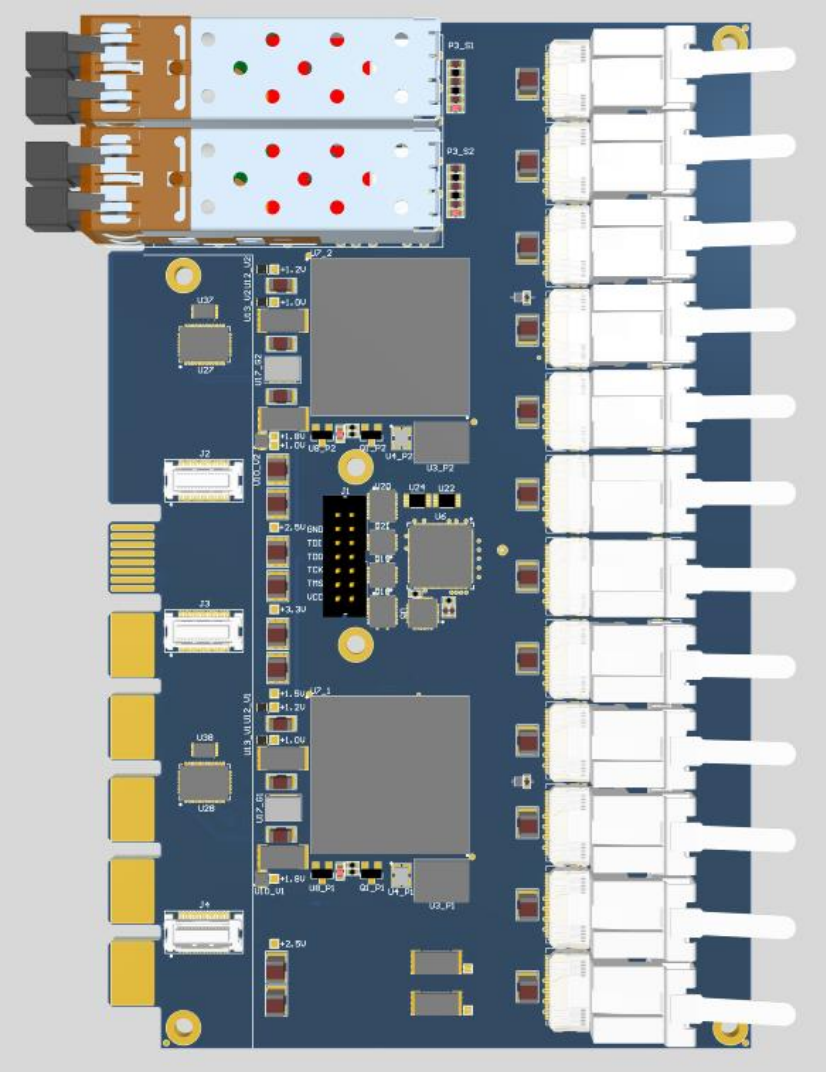
(FireFly™ Low Profile Micro Flyover System™ Cable Assembly)

- 12 Firefly modules (144 LVDS channels)

3. Custom interface/connector

(to be developed on demand)

LVDS DC



Readout Board obtained from the 64-channel ADC for the EMC Forward Endcap

Issues, which were discussed:

- Electrical specifications
  - Power supply (internal/external)
  - SFP/VL/VL+
  - Additional functions
- Mechanical specifications
  - Encapsulation
  - Placement

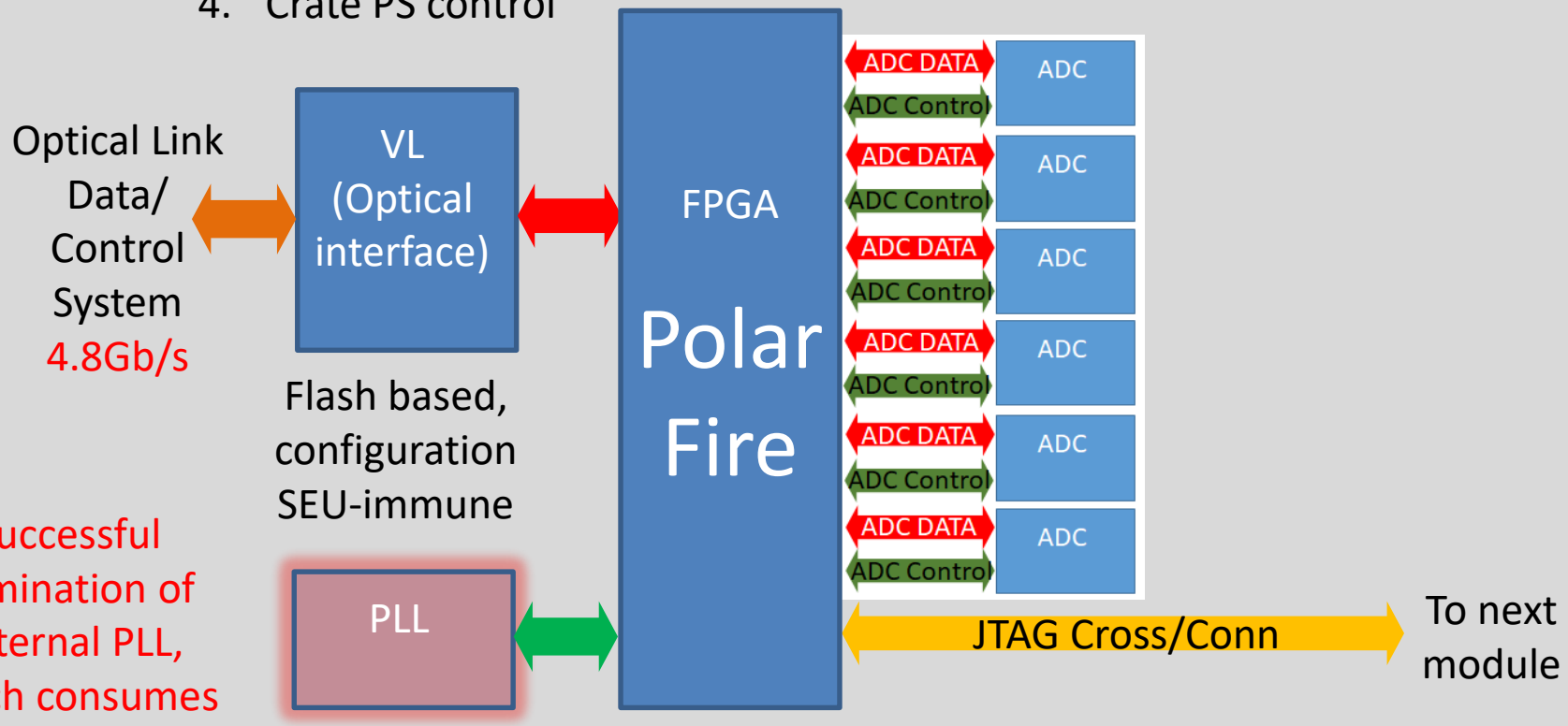
Status:

- Re-design completed
- Ready for production
- Components need to be ordeded before expected price “adjustment”

CRATE CONTROLLER

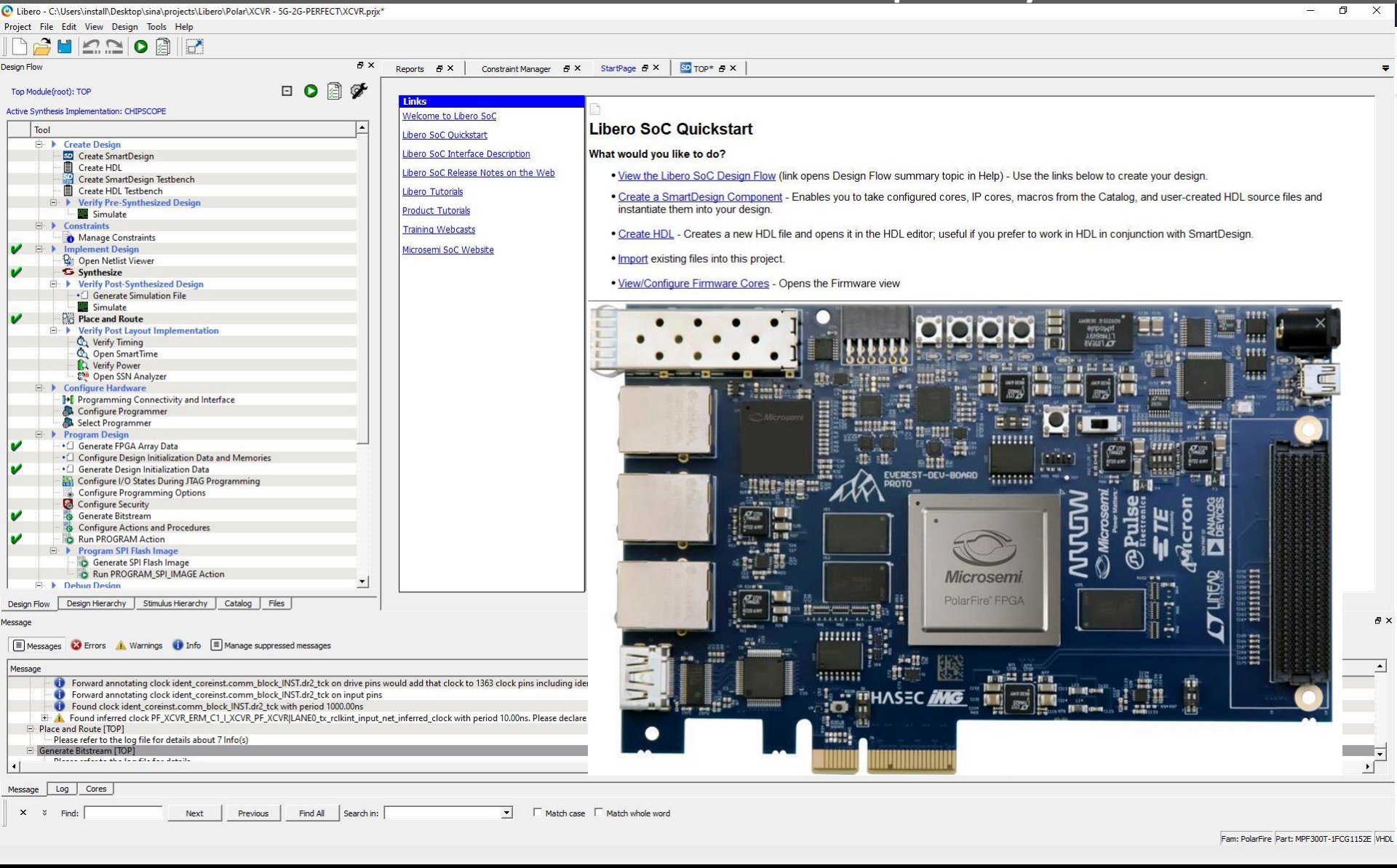
Polar Fire – based Crate Controller

1. Direct JTAG configuration of individual ADCs
2. Reaction to SEU
3. Health control of ADCs (voltages, currents, temperatures)
4. Crate PS control



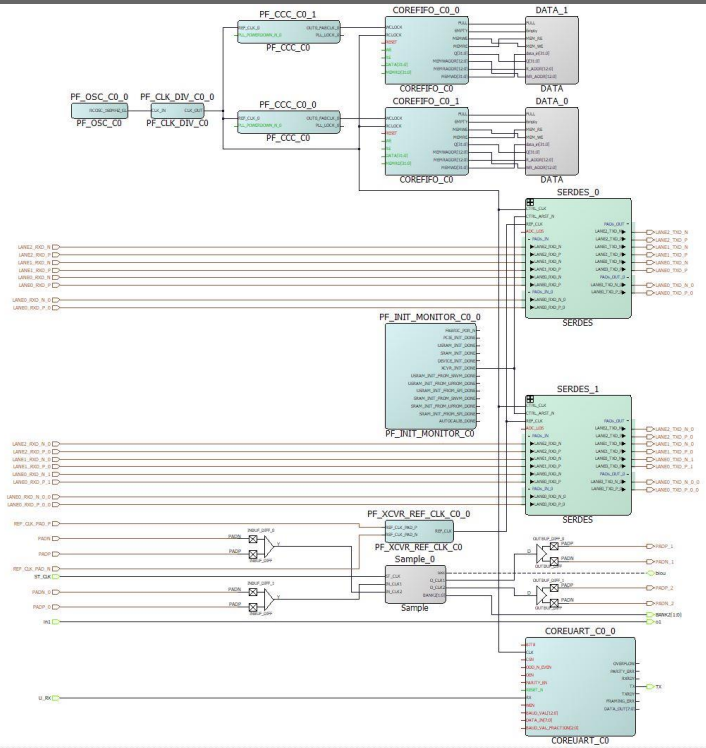
CRATE CONTROLLER

- Evaluation card with Libero development system



CRATE CONTROLLER

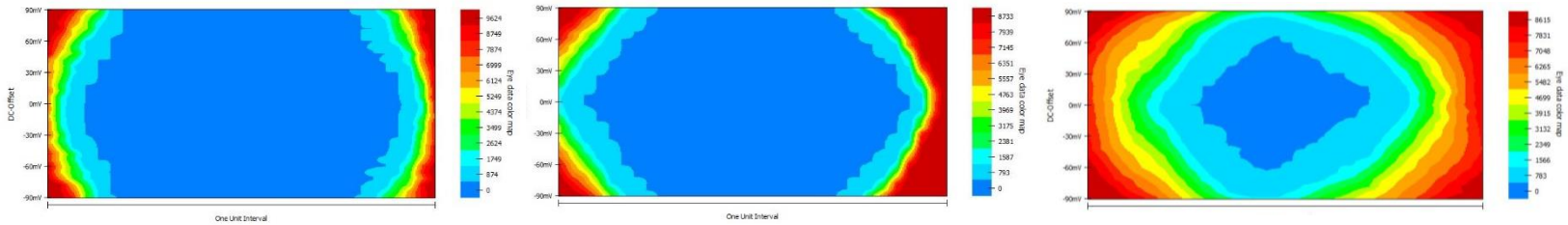
A project containing 6 channels 2Gb/s and 2 channels 6.25 Gb/s (time deterministic)



Status

Firmware:

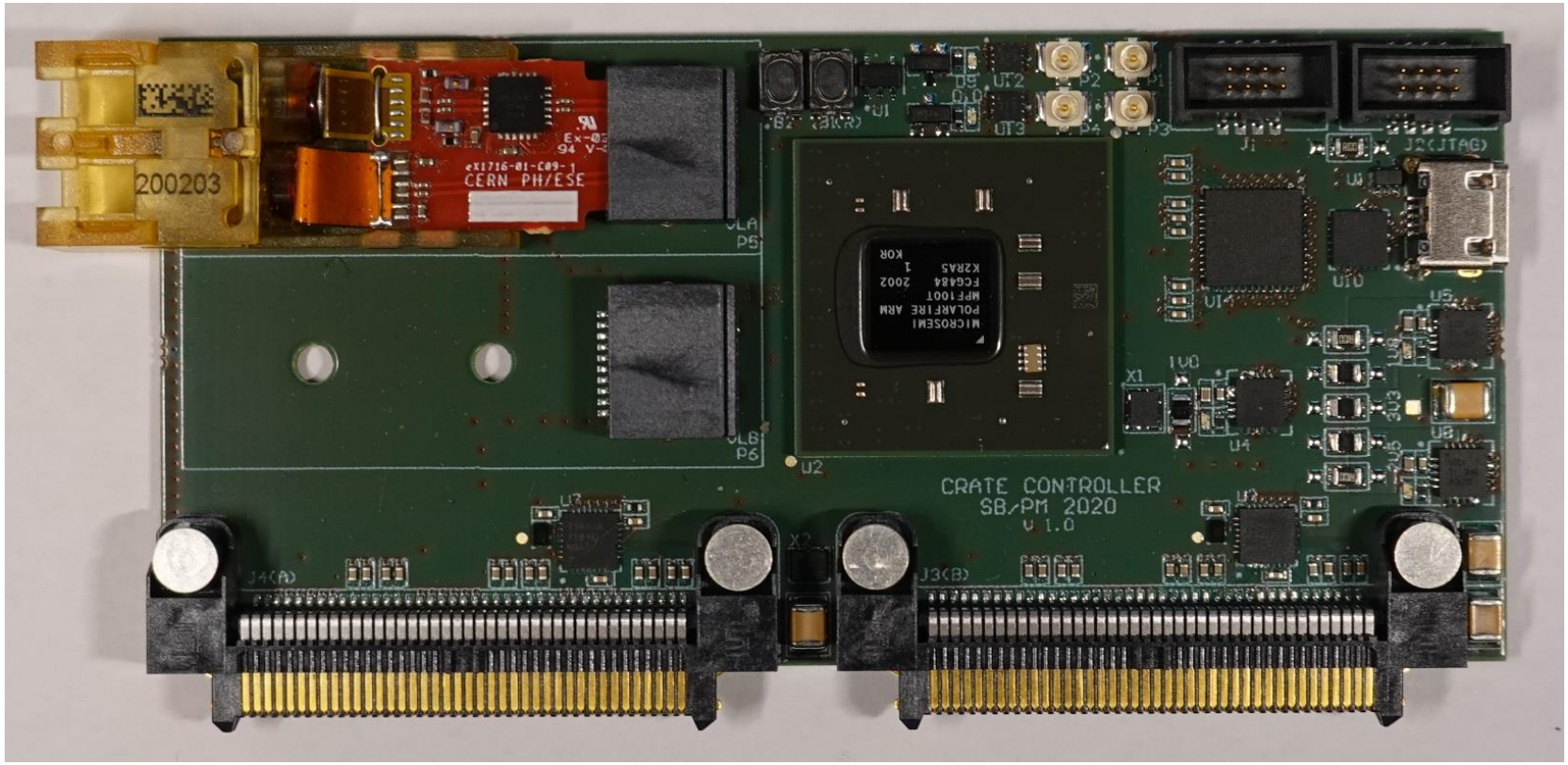
- Canvas project in Libero is ready (mux **3 x 2** Gbit/s → **6.25** Gbit/s
- Successful elimination of external PLL, which consumes ca 700 mW
- Successful time deterministic tests of bilateral communication to ADC



2 Gb/s 6.25 Gb/s 10 Gb/s

Crate Controller

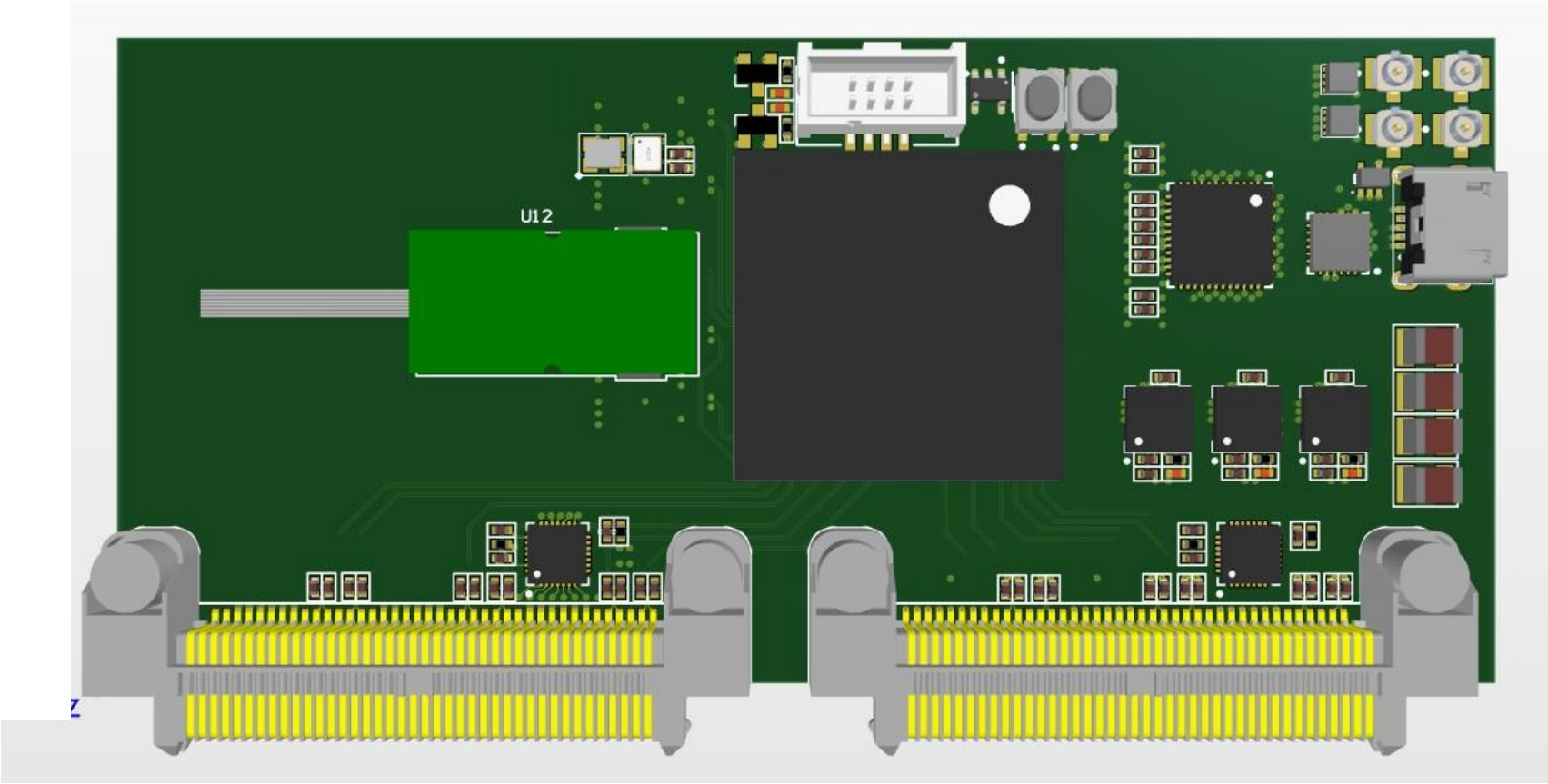
Dual channel VTRx
Test version, 2 x 4,8 Gb/s



The first prototype with VTRx

Crate Controller

Future plans:
Dual channel VTRx+
2 x 10 Gb/s



Old artwork of the future Crate Controller
VTRx+ will be produced 2021

Updated plans

- ADC – production for Shashlik, tests – Jan..Aug 22
  - Production needs quite urgent decision due to planned component price changes
- Ev. ADC redesign for barrel – Aug 21..Aug 22
  - Decision depends on the Pulse Detection Asic progress
- PANDA DC – test Jan21..Dec 22 master, phd
  - Basic debugging started, manpower will be needed in the future
- - Second prototype, volume Aug 21..Aug 22
  - Based on the outcome of the first tests
- LVDS DC – tests Apr 21..Aug 22
  - Device was discussed and approved by the collaboration. It will go to prototype production
  - FPGA for the bulk needs to be ordered until April 2021
- Crate controller – Jan..Jun 21 – master
  - Debugging started, but the envisaged master student has left. I will continue anyhow.
- Power Supply – tests Feb 21
  - Unclear situation, since new call for experiments at AGOR left no time for an application
- Backplane – Jun..Dec 21
  - New backplane is ready and will be sent along with the LVDS-DC for production

Thank You !