ToASt ASIC development status

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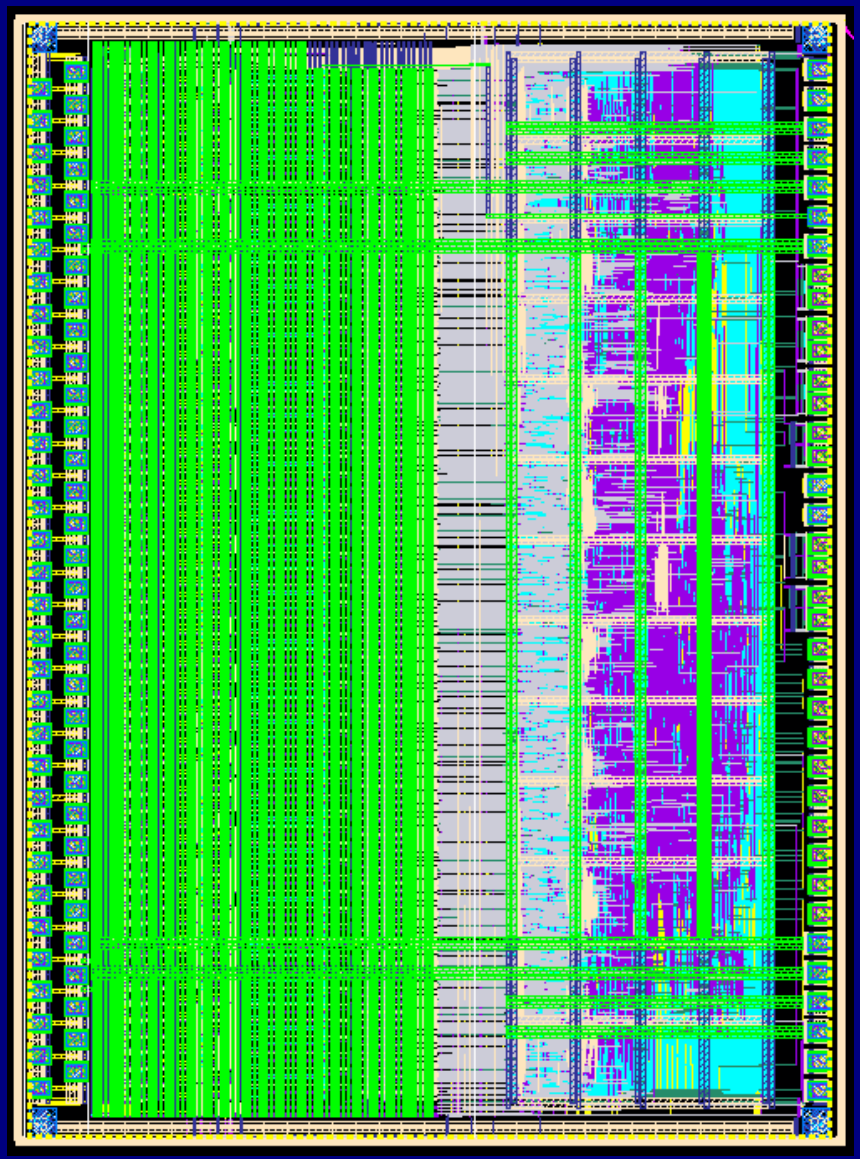
Specifications

Specification	Min	Max	Unit
Input capacitance	2	17	pF
Max rate per strip		40	kHz
Input charge	1	40	fC
Noise		1500	e^-
Preamp peaking time	50	$\geq$ 100	ns
Channels per chip	64		
Reference clock		160	MHz
Charge resolution	8		bits
Time resolution (pk-pk)		6.25	ns
Time resolution (r.m.s.)		1.8	ns
Power consumption		256	mW
Chip dimensions	4.2 $\times$ 3.5		mm^2
Pads position	On two sides only		

ToASt main characteristics

- 64 input channels
- Time of Arrival (ToA) and Time over Threshold (ToT) measurements
- Master clock frequency : 160 MHz
- Region : groups of 8 channels with local FIFO
- Second level FIFO buffering for the 8 regions
- Two output serial links at 160 Mb/s
- Serial configuration protocol at 80 Mb/s
- Full SEU protection via Triple Modular Redundancy
- CMOS 0.11 μm technology

ToASt layout



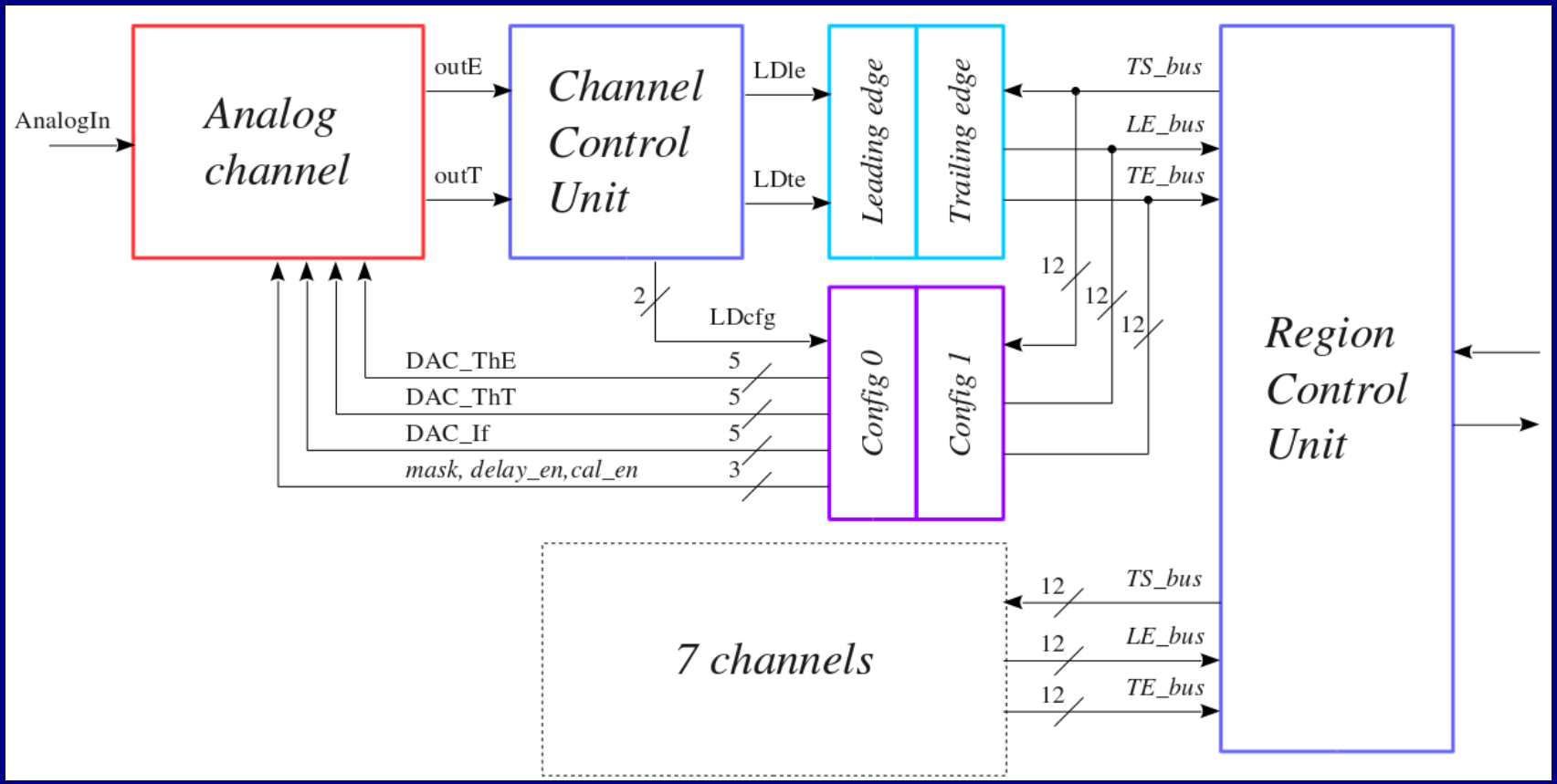
- CMOS UMC 0.11 μm technology
- Digital-on-top design flow
- Die size : 3.24×4.41 mm^2
- Left pads pitch (on two rows) : 63 μm
- Right pads pitch : 90 μm
- Three power domains : analog, digital, digital pads *(all supply voltages at 1.2 V)*
- One external analog reference ($V_{BG} = 600$ mV)
- SLVS driver/receivers

Status

- FE design : completed
  - minor optimization ongoing (mainly adding filter capacitors)
- BE design : signoff and final verifications done, timing closure ok
- FE+BE integration done, DRC and LVS ok
  - full chip verification ongoing
  - power analysis ongoing
- *Submission foreseen for April 28th 2021*
- To be evaluated (not for this submission) whether the full triplication results in a too high power penalty
- Other possible power consumption mitigation strategy : digital supply voltage reduction to 1 V.

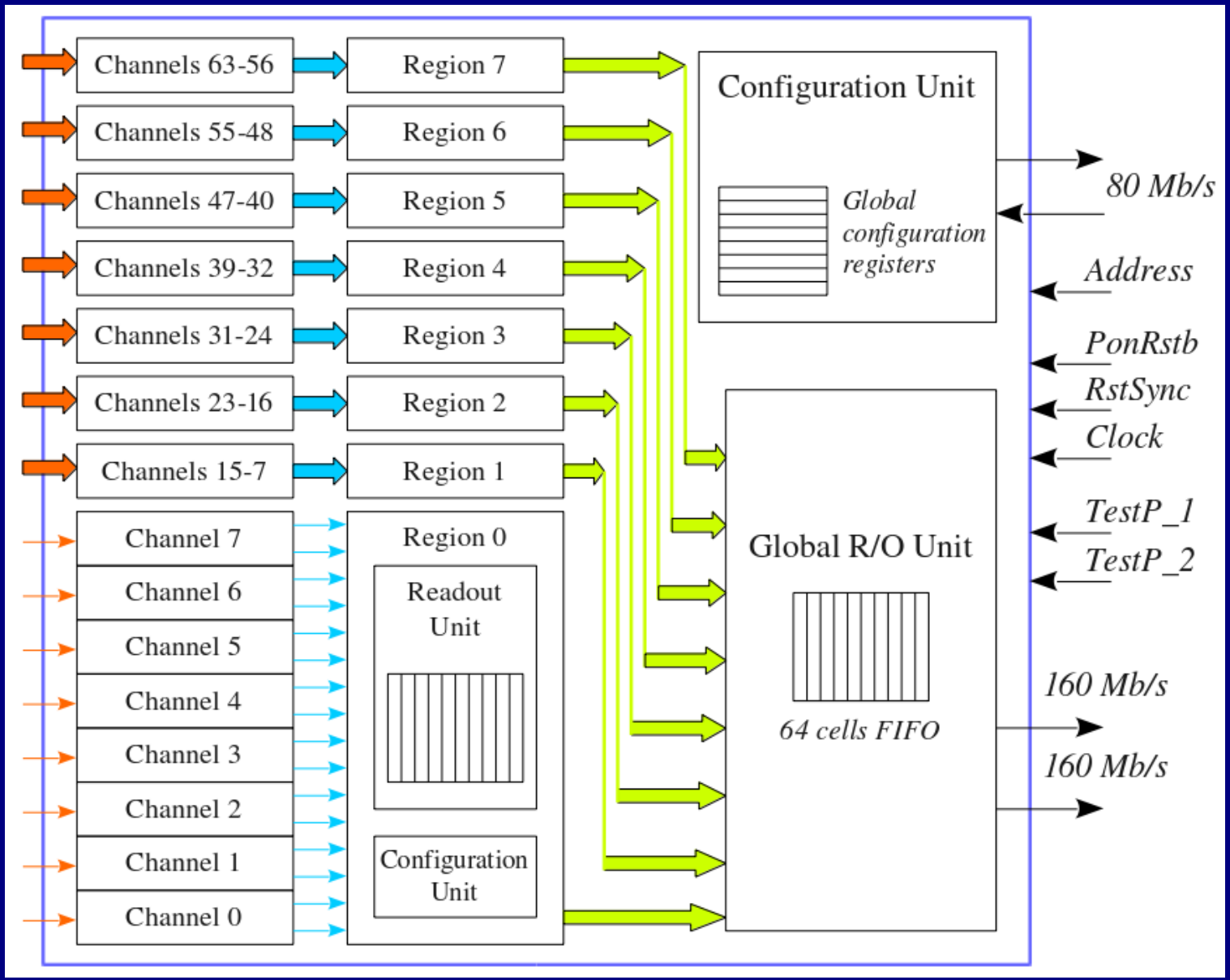
Spare slides

ToASt channel schematic



- Common time reference : 12 bits time stamp distributed to all channels
- Time stamp can be Gray-encoded
- LE and TE registers latch time stamp at comparator rising/falling edges

ToASt architecture



ToASt pinout

Pin name	Direction	Description
in[63:0]	In	Analog inputs
pon_rst	In	Power on asynchronous reset
SyncReset	Rx	Synchronous reset
ChipAddr[6:0]	In	Chip address
TestPulse	In	Digital test pulse
CfgRx	Rx	Configuration receiver
CfgTx	Tx	Configuration transmitter
TxOut_0	Tx	Data serial output 0
TxOut_1	Tx	Data serial output 1
V_{BG}	In	Analog bandgap reference
V_{DDA},V_{SSA}	IO	Analog supply and ground
V_{DDD},V_{SSD}	IO	Digital supply and ground
V_{DDE},V_{SSE}	IO	Pads supply and ground