Update on hardware activities

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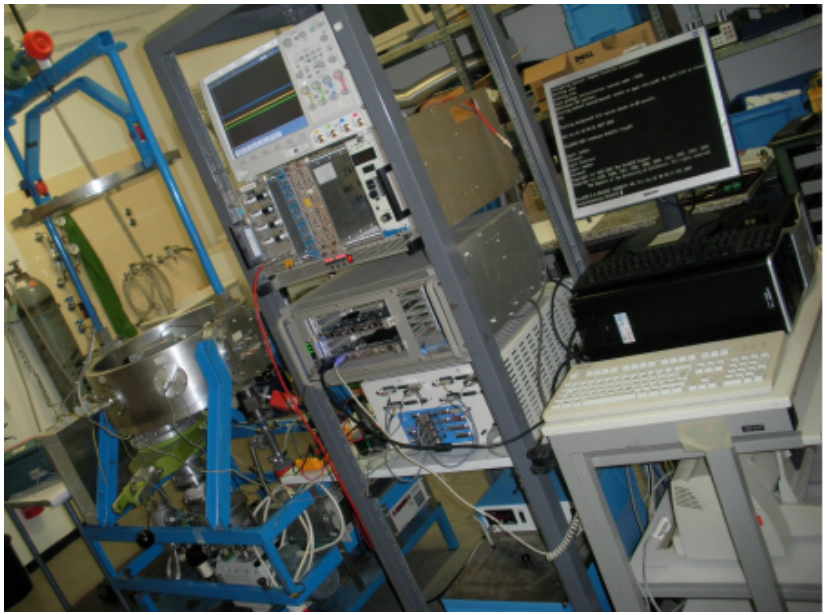
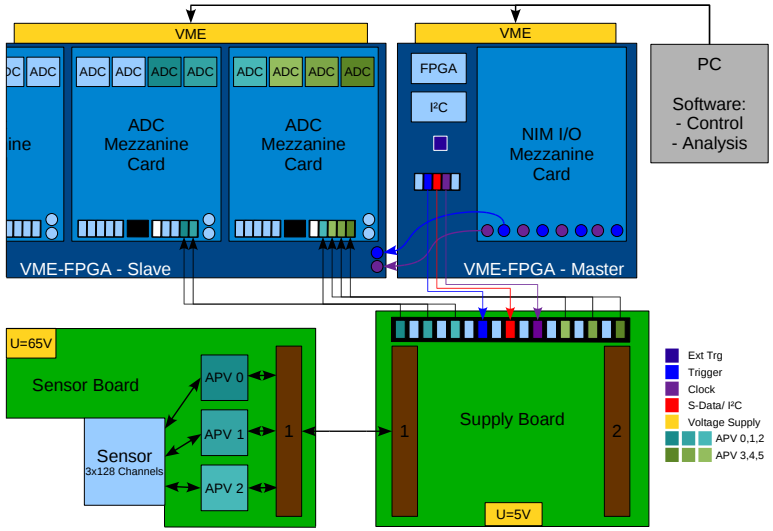
Status in November, 2010





test setup consisting of

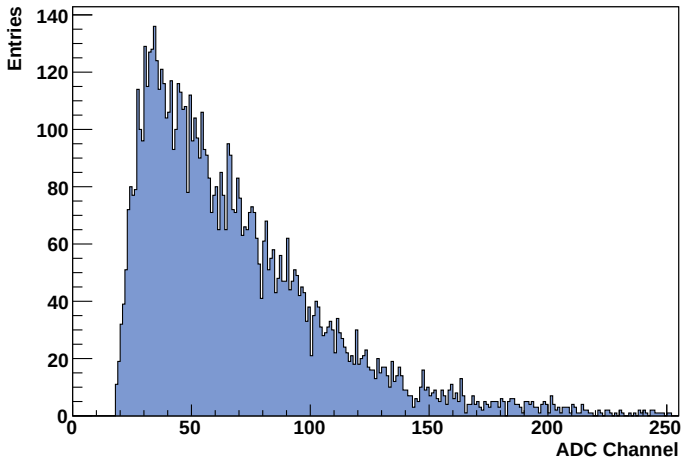
- silicon test sensor from ATLAS
- APV25-S1 front end chip
- VME-FPGA readout by Bonn group

built up and working

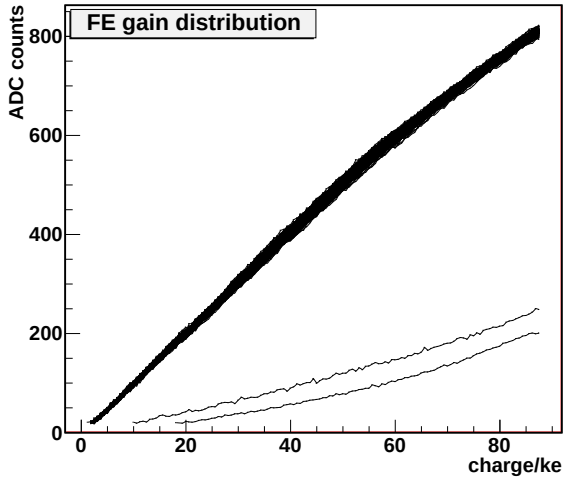
To-Do:

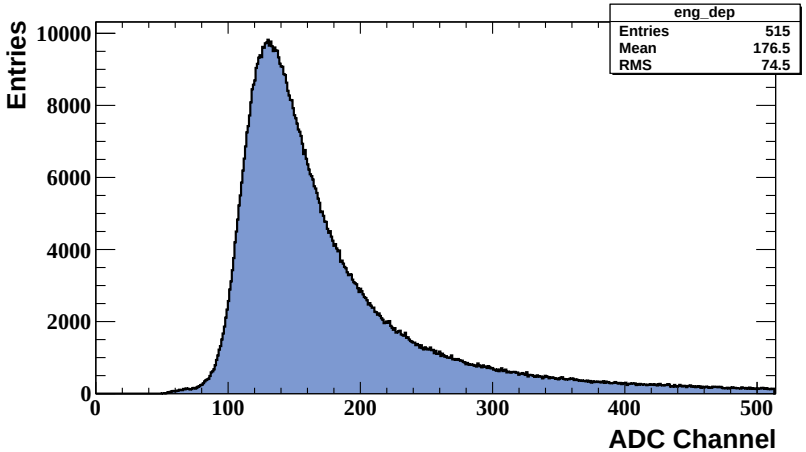
- find source of voltage increase at APV
- take first measurements(energy loss, beam profile)

ADC spectrum and calibration



ADC spectrum of single APV channel

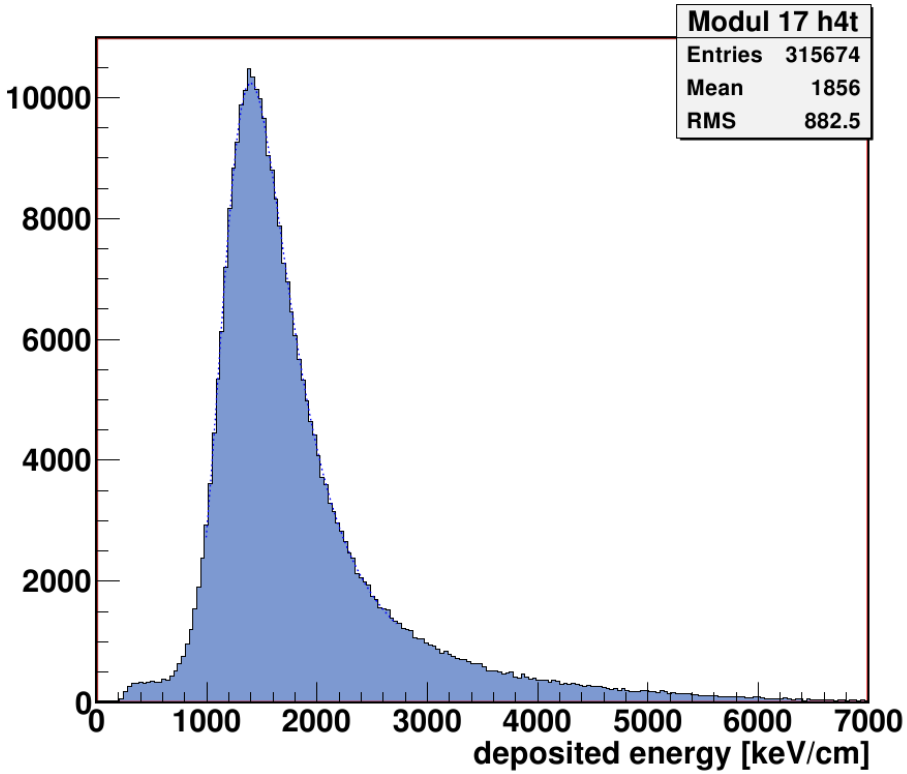




ADC spectrum of all channels

- ADC spectra show expected landau shape
- charge conversion not linear for charges $>$ 60 ke

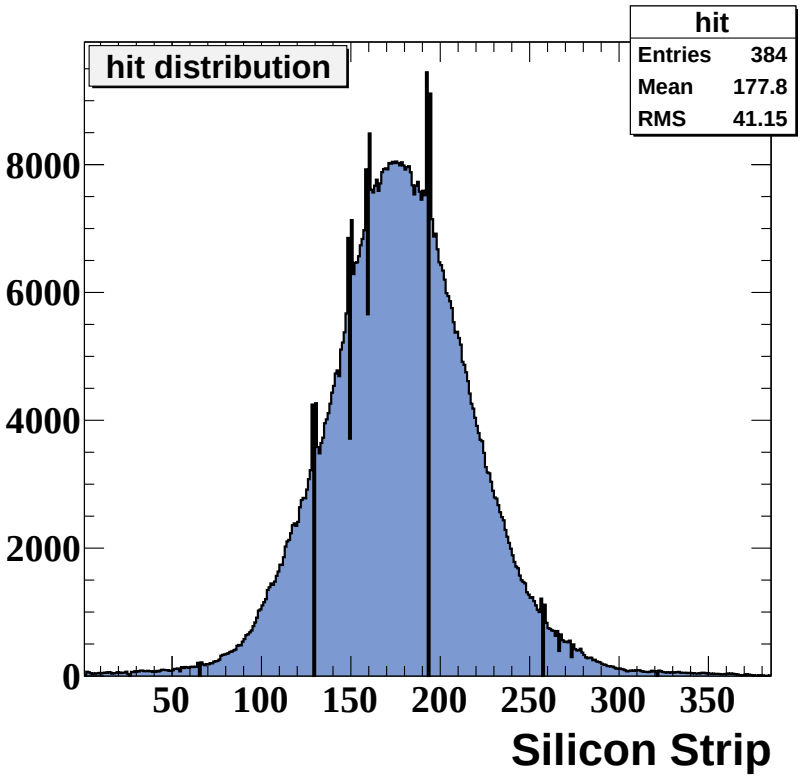
energy loss



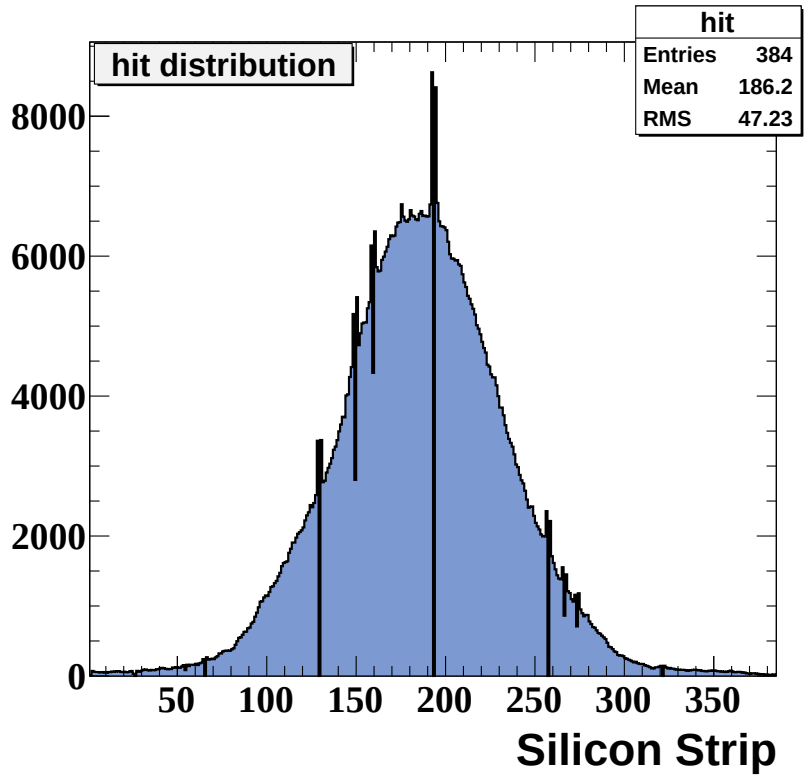
- measured energy loss: 1600 keV/cm
- expected energy loss from Bethe-Bloch: $\approx$ 3600 keV/cm
- source of discrepancy not understood

beam profile

Distance source to sensor: $d = 60\,\text{mm}$



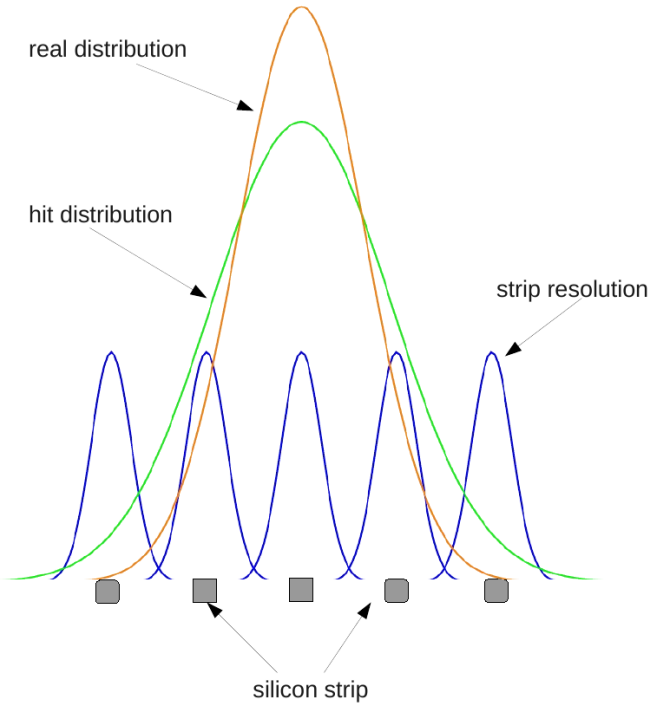
$d = 85\,\text{mm}$



➥ extract spatial resolution from hit distribution

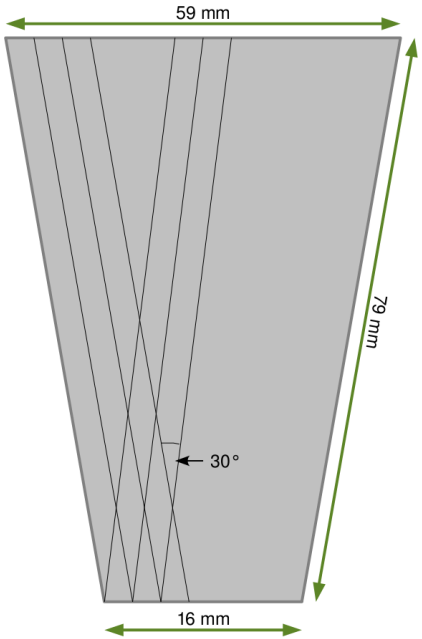
spatial resolution

- **Idea:** hit distribution is convolution of the real particle distribution and spatial resolution of silicon sensor



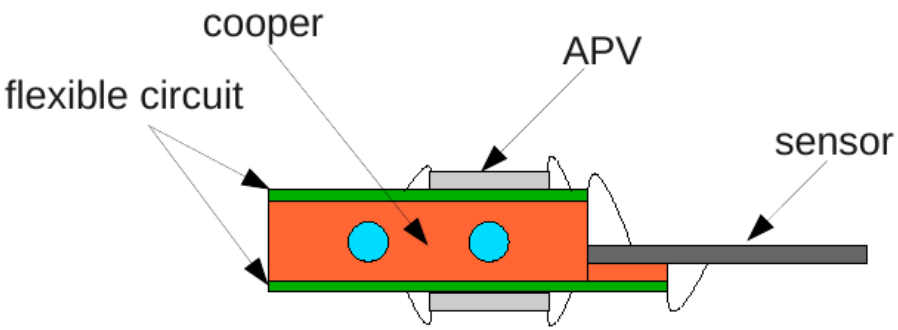
- measure hit distribution for different displacements of source and senor ⇒ spatial resolution
- first simulation conducted

YY2 silicon sensor

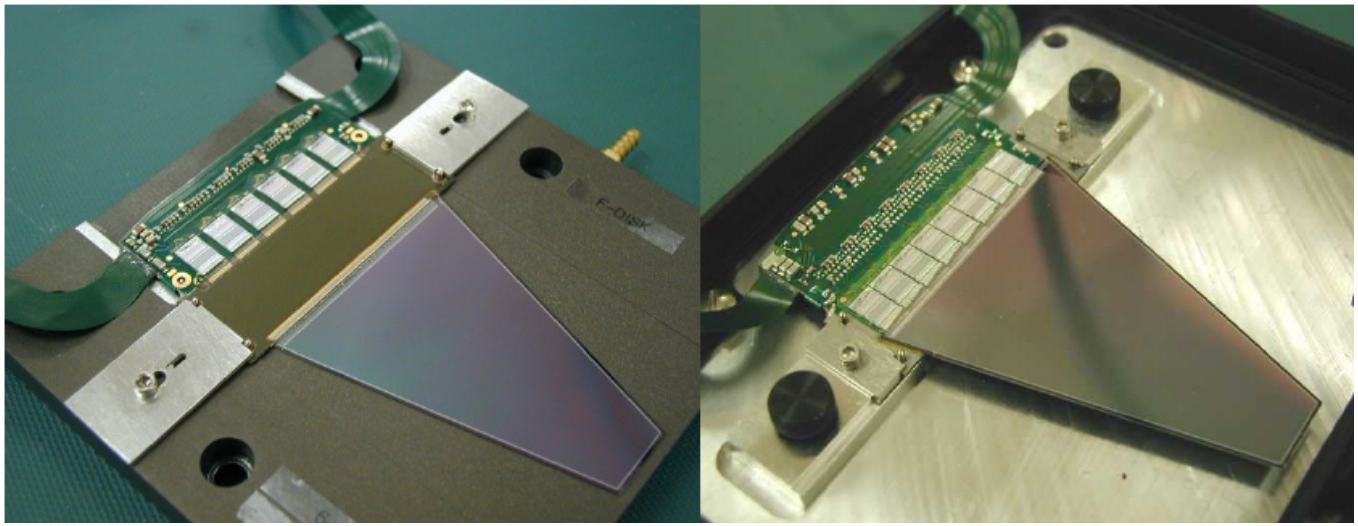


- double sided silicon sensor from D0
- 140/300 μm thick, 50 μm pitch
- 1024 strips, 30° stereo angle
- two seperated rows of readout pads on n-side

mechanics and front end cooling

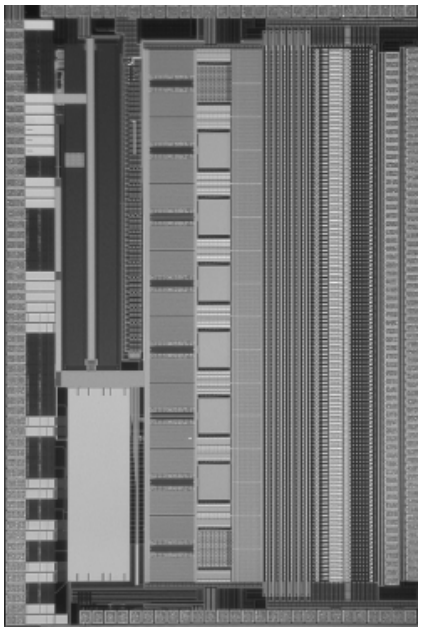


- capton based flexible circuit glued to cooper base
- use YY2 sensor
- design of a flexible circuit for the APV
- Overall design close to design of F-disc from D0/Fermilab



FSSR2 front end chip

- designed for silicon strip detectors
- 3-bit ADC with adjustable thresholds
- digital data output
  - only channels with hit
  - timestamp
- self triggered ⇒ more suitable for luminosity monitor
- possible to get some spare chips from CLAS



- contact with JLab about FSSR2 testboard
  - FPGA based readout system
  - first noise and register tests performed
- develop own readout system using the JLab testboard