Readout-Controller design for the MVD silicon strip sensors

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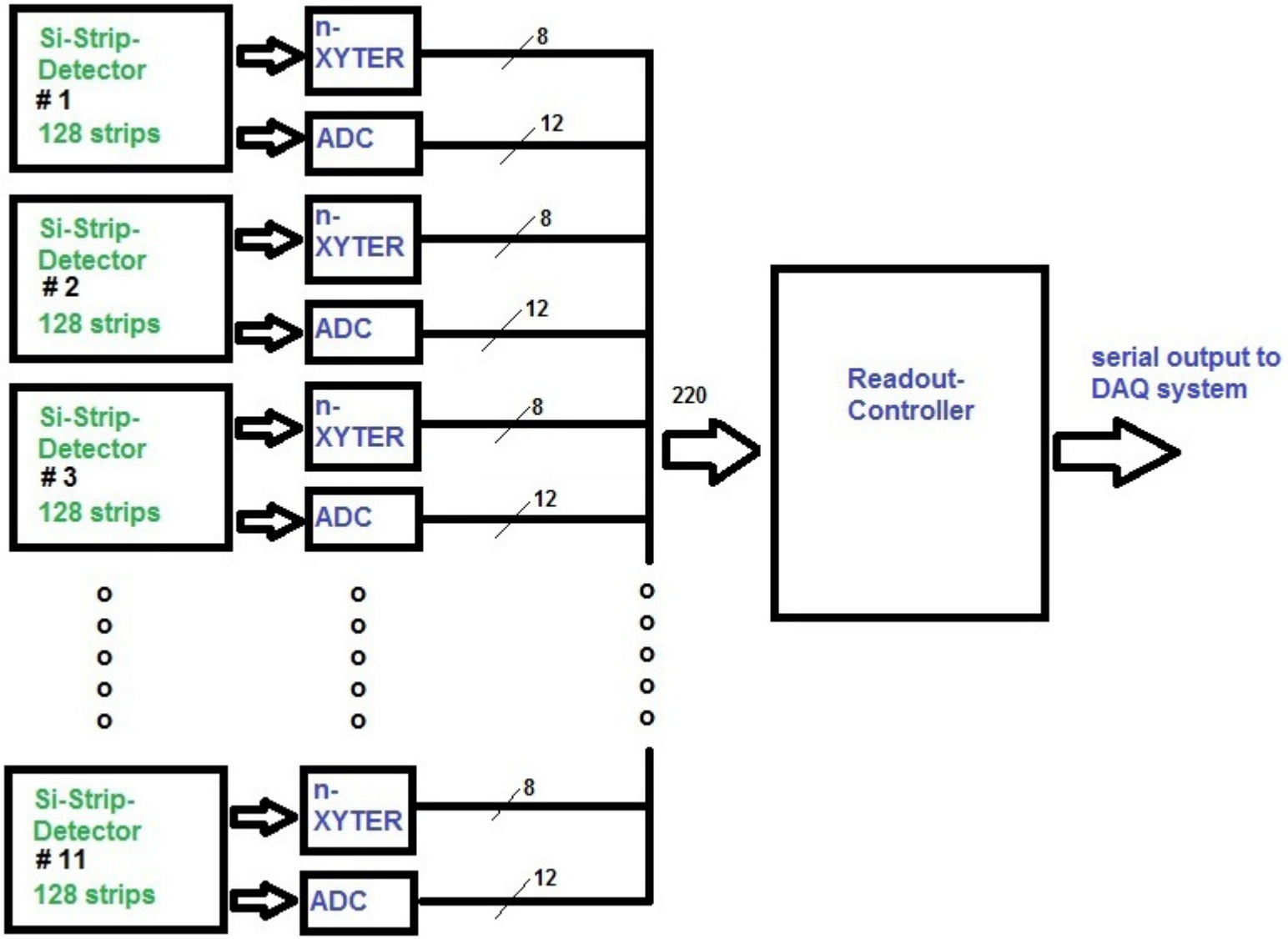
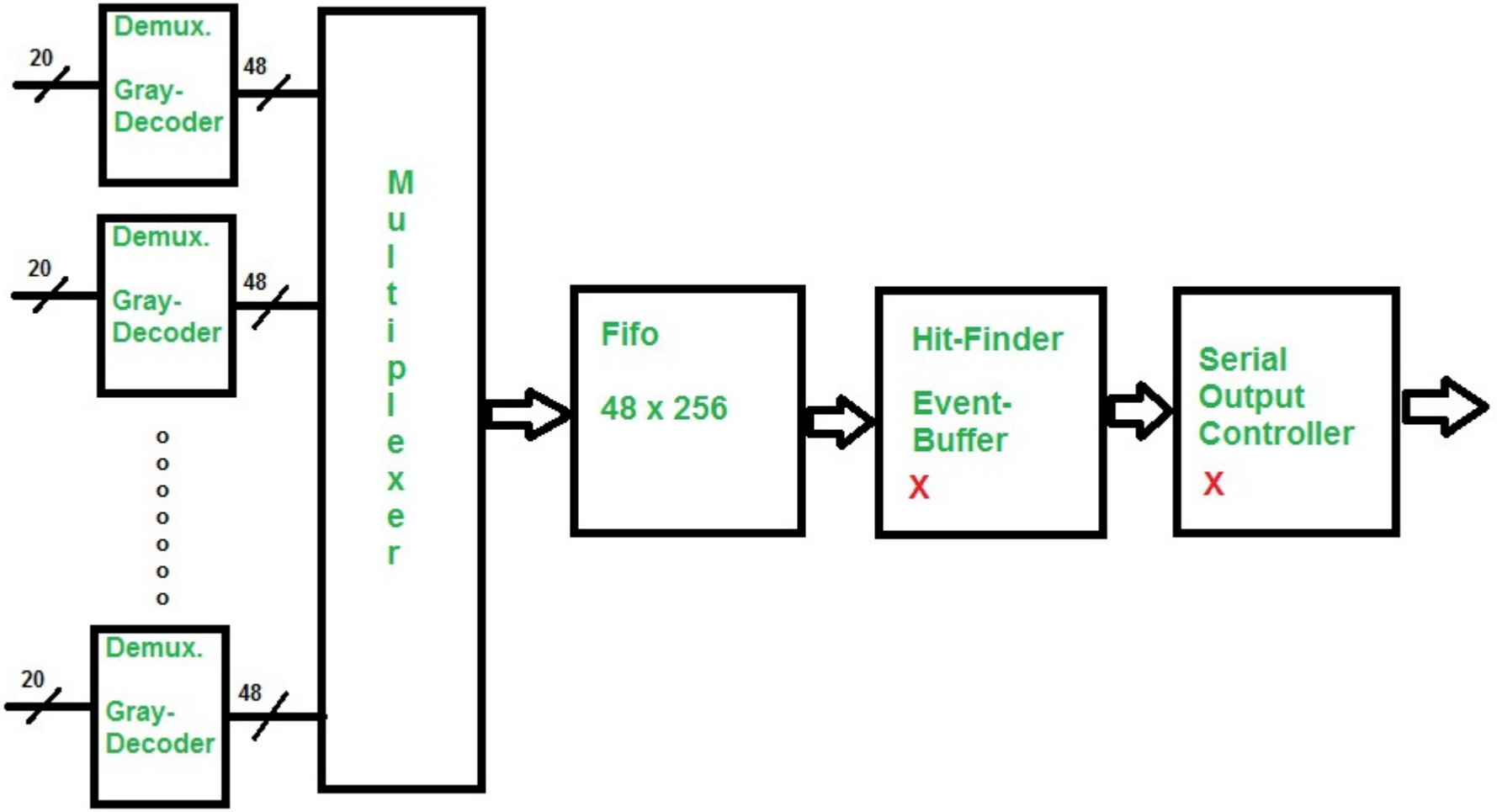
- one element of the strip detector section consists of 7 horizontally and 4 vertically aligned sensors (128 strips each)
- the n-Xyter (1) is designated as frontend readout chip
- self-triggered readout
- 11 n-Xyter's plus 11 ADC's are needed for one detector element

(1) The n-XYTER Reference Manual chip-version 1.0 , A.S. Brogna et al., Physikalisches Institut Heidelberg (2009)

7 x 5 Si-Detector Modules 896 x 512 strips



Readout - Controller Internals



X : to be done

Preset state:

- **a modular VHDL-based FPGA-design is in progess**
- **5 simultaneous hits per sensor and event can be processed at n-Xyter-clock speed (128 MHz) loss-free**
- **multiplexing hits of 11 sensors takes ≈ 150 ns (simulation using Xilinx Spartan 6 XC6SLX75 FPGA)**
- **pedestal handling, hitfinding and output to DAQ t.b.d.**
- **testing will be performed using the Bonn-Si-sensor test system a.s.a.p.**