Status CRI

CRI THROUGHPUT (Only for one FPGA super region!)

Maximal throughput PCI Express Generation 3 , x8 lanes is 7,877 GBytes/s (wikipedia)
Maximal theoretical throughput from one GET4 2370 KHits
Mean value per channel 200 Khits (total 800 KHits)
Hit message length is 64-bits
There are 24 optical links or GBTx

	Maximal	Mean (200/ch)
GET4 Throughput (Khits)	2370	800
GET4 Hit length 64-bits [Bytes]	19M	6.4M
24 GBTx x 40 GET4 (Bytes)	18,2G	6,14G
PCIe 3.0 x8	7,8G	

CRI vs AFCK Resources

		AFCK (XC7K325T)	CRI (KU115)	Factor
Logic Cells		326080	1451100	x4,4
Configurable Logic Bolcks	**Slices**	50950	165.84	x3,2
	“FFs”	407600	1326720	x3,25
	LUTs	203800	663360	x3,25
	Distri RAM Kb	4000	18300	x4,6
DSP Slices		840	5520	x6,6
Block RAM Blocks	**18 Kb**	890	4218	x4,7
	36 Kb	445	2019	x4,7
	Max Kb	16020	75924	x4,7
CMTs		10 (1MMCM, 1 PLL)	24 (1MMCM, 2 PLL)	
PCIe		1	6 (PCIe Gen3 x8)	x6
Gigabit Trans		16 (GTX 12.5Gbps)	64 (GTH 16.3Gbps)	x4
CLB		8xLUTs + 16xFFs	8xLUTs + 16xFFs	

Configurable Logic Block (CLB) estimation

I tried to extract the resources pro GET4 and GBTx but is not possible because the FPGA replicate resources to achieve the Timing Constraints.

AFCK

#GBTx=6
#GET4 = 48 GBTx x 40 GET4/GBTx = 240

CRI

#GBTx = 48
#GET4 = 48 GBTx x 40 GET4/GBTx = 1920

There is a factor 8 more links but only a factor 3 or 4 in resources!
If we take only one BRAM pro GET4 and one BRAM pro GBTx 1968 from 2019 are gone!

New technology will help with the timing!

Kintex 7 is 28 nm
Ultrascale is 20 nm