EMC Front-End Electronics Meeting
Report

M. Kavatsyuk

for the PANDA collaboration

KVI, University of Groningen, Groningen, The Netherlands

EMC-FEE Meeting
(Groningen 18-19 of October)

The goals of the meeting:

- Discuss FEE-development strategy
- Identify possible problems of integration
- Define milestones

Indico: PANDA → Detector → EMC → PANDA EMC FEE

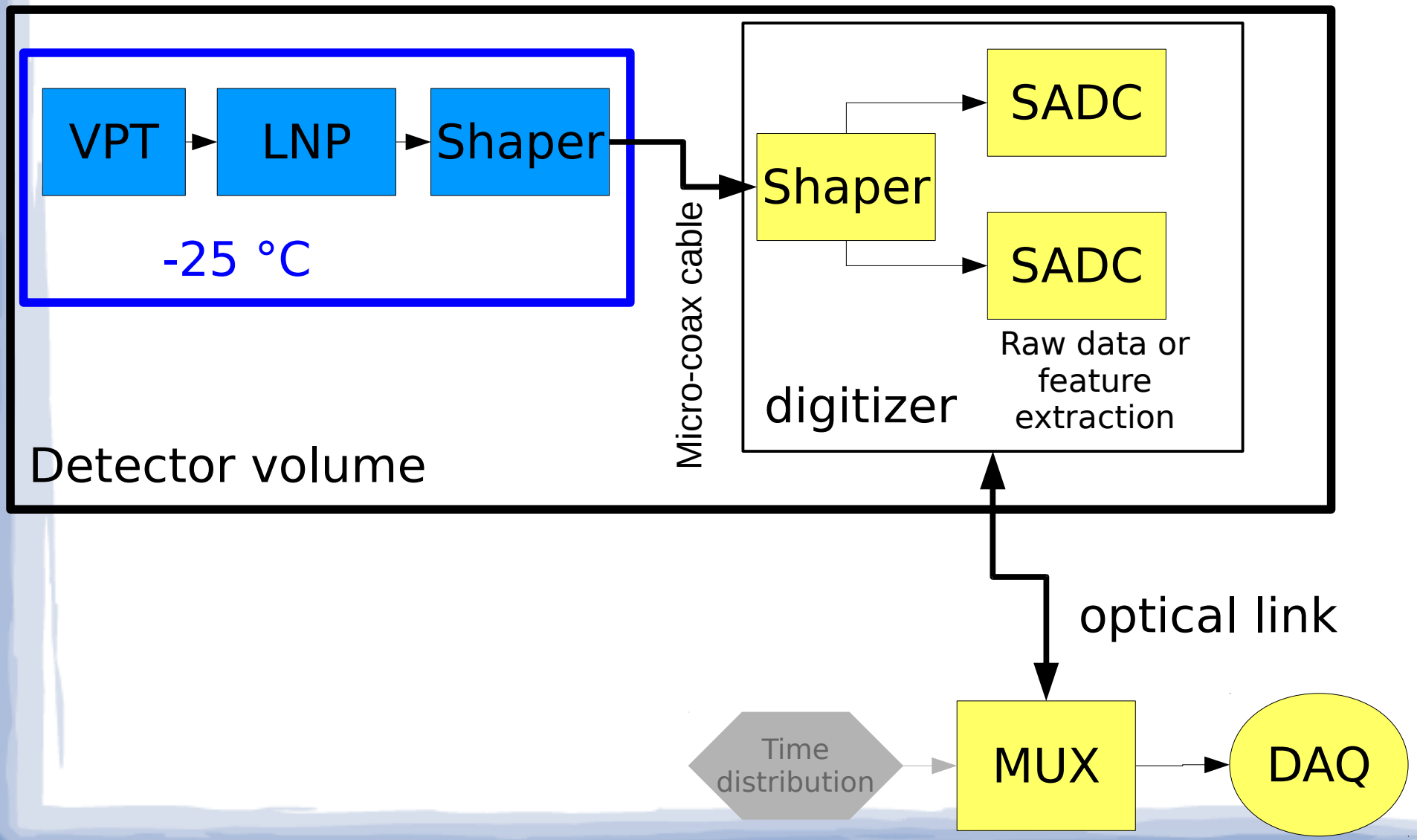
EMC-FEE

The main goal of the development:

- By 2014 have ready front-end electronics based on the commercially-available components and the trigger-less data acquisition

EMC Readout Scheme
Forward Endcap

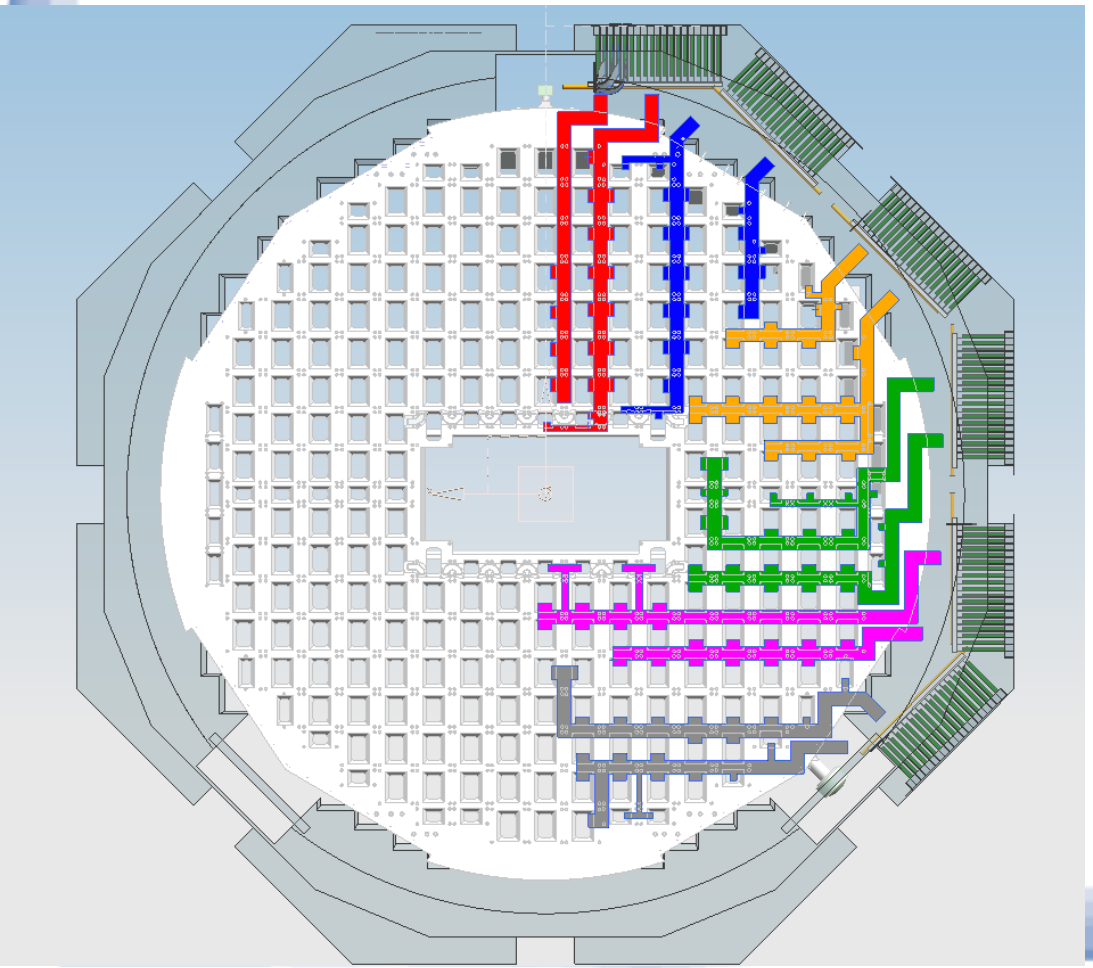
The readout scheme for test beams at Jülich

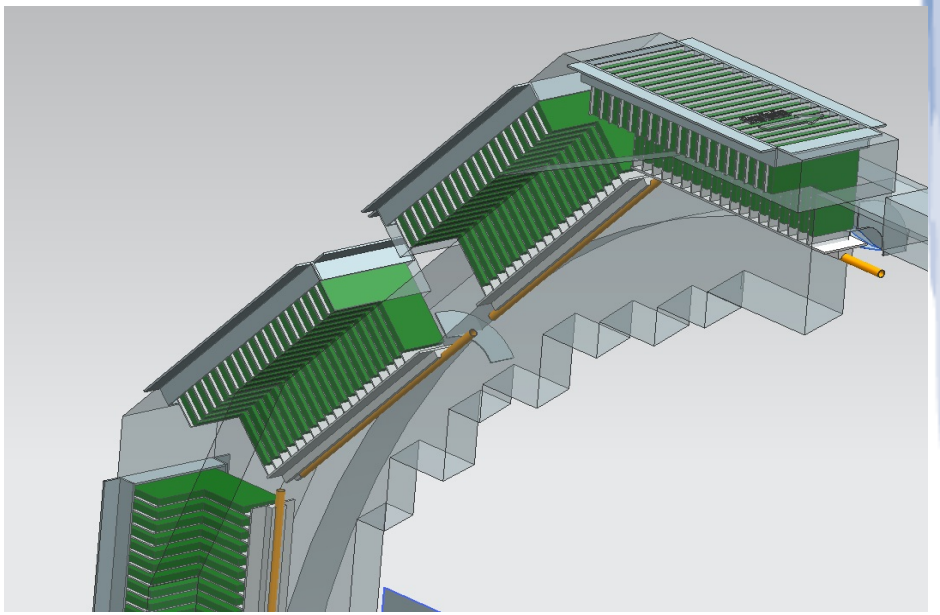


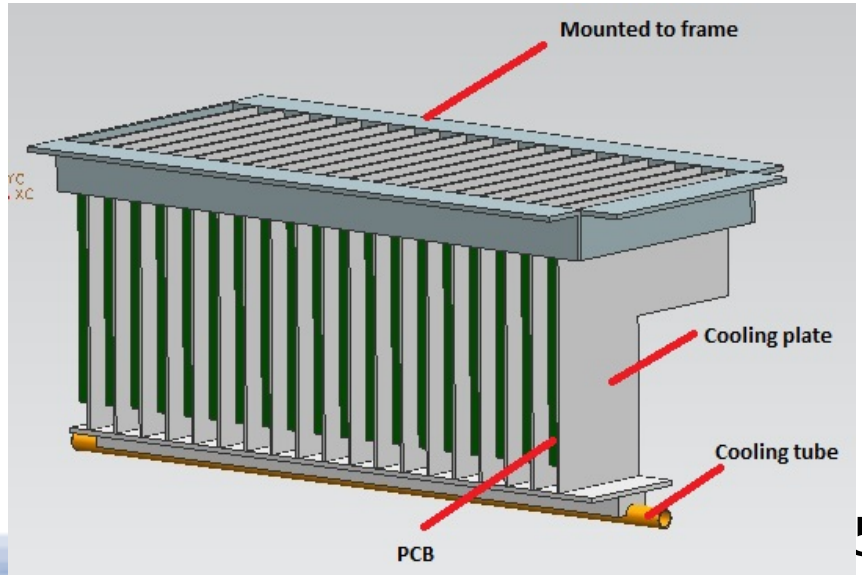
Forward Endcap
Space for Electronics

R. Veenstra

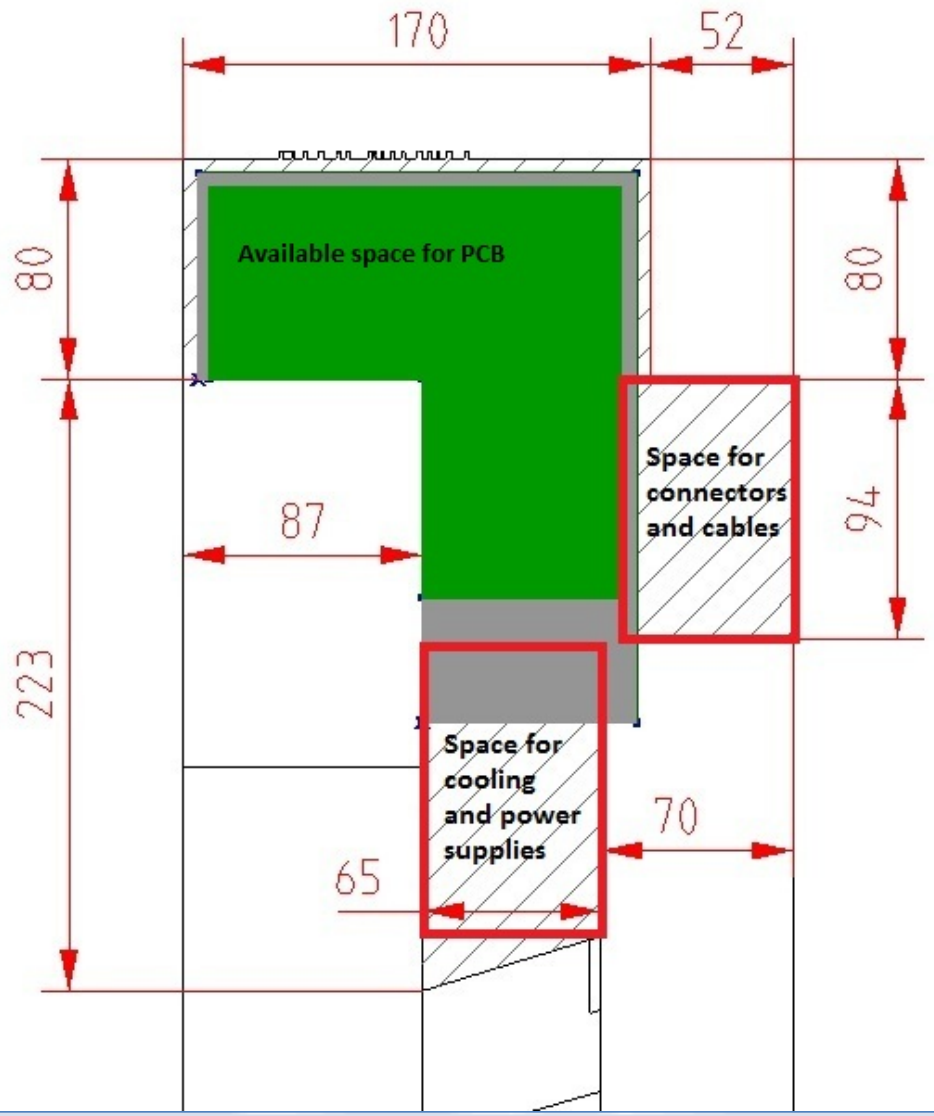
First conceptual design







Forward Endcap
Space for Electronics



Possible dimensions of the digitizer module

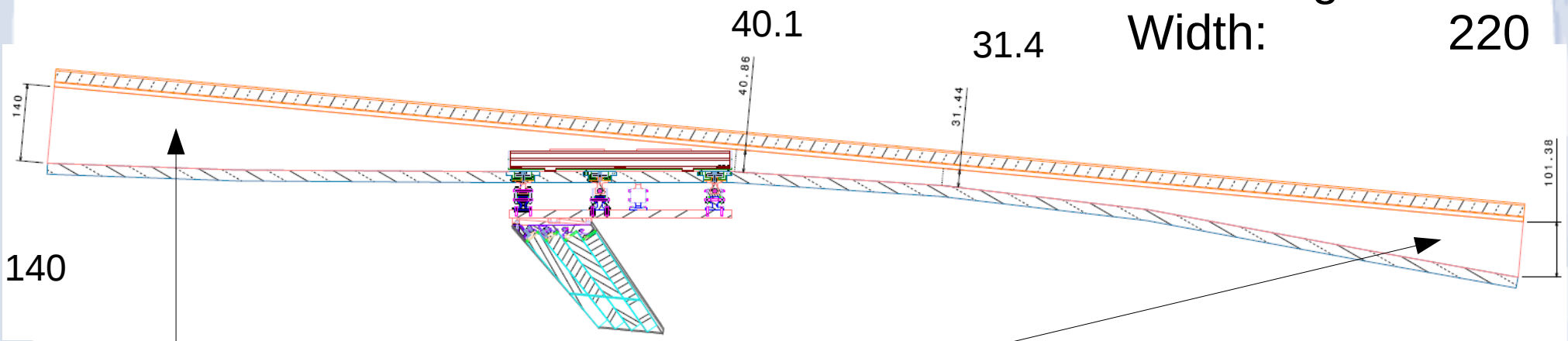
Forward Endcap
Discussed topics

- The analogue shaper should be integrated partially into LNP preamplifier and into the input buffer of the SADC (prototyping done by spring 2011)
- Explore a possibility of the placement of the electronics in such way that it can be easy accessible for maintenance
- Possible cases for the digitizer module layout:
  - 64 ch., 11-bit SADC; LAAPD readout (2 LAAPD, dual gain);
  - 32 ch., 14-bit SADC; LAAPD readout (2 LAAPD, single gain);
  - 32 ch., 11-bit SADC; LAAPD readout (2 LAAPD with analogue summation before SADC , dual gain);
  - 32 ch., 11-bit SADC; VPT readout (1 VPT, dual range);

Barrel
Space for Electronics

Support beam structure

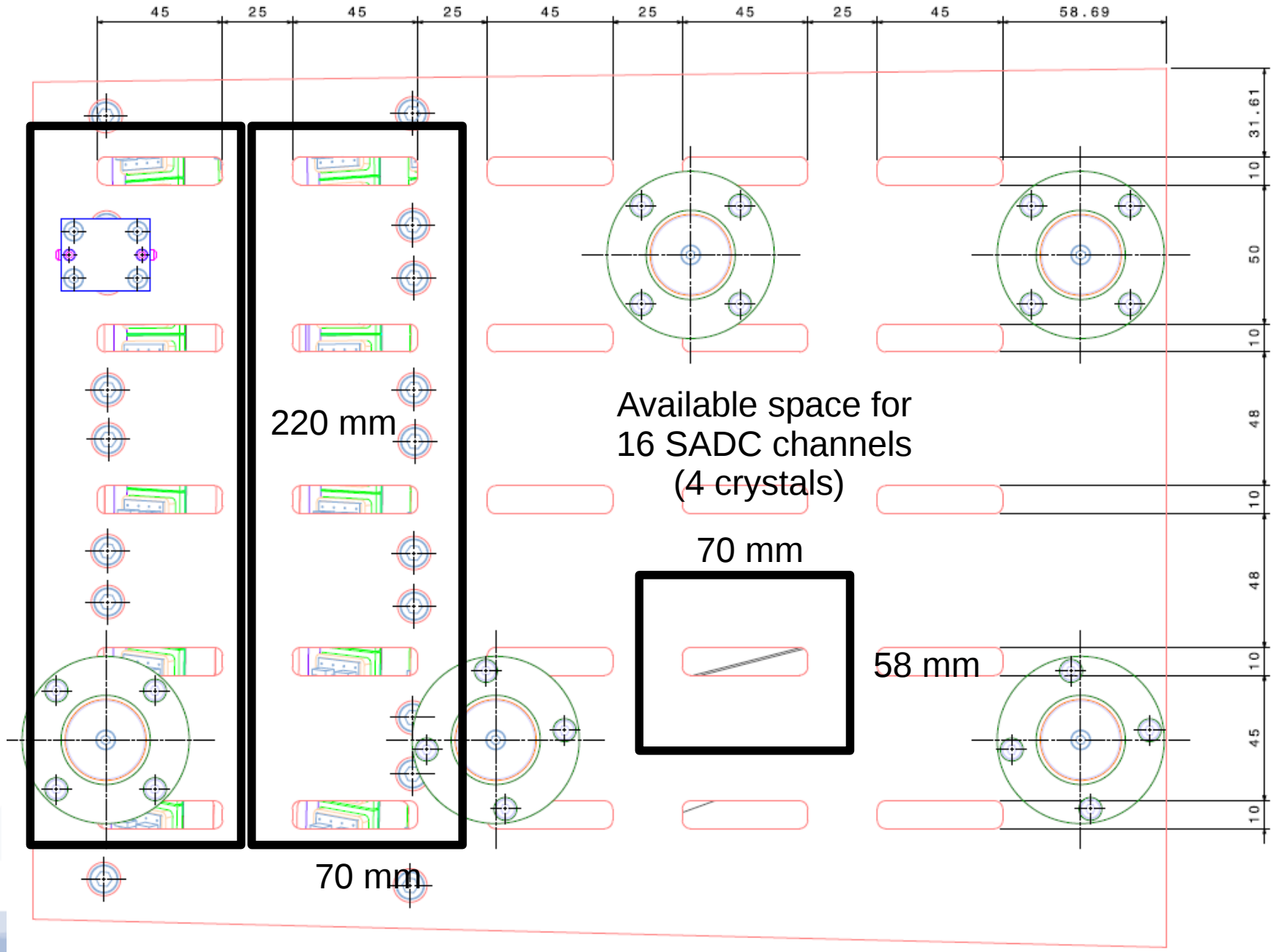
Total length: 2680
Width: 220



Space for the electronics

Total number of crystals: 10×71 = 710 (2840 SADC channels)

Barrel
Space for Electronics



Barrel
Discussed topics

- The space available in the support beam is very limited (70 x 220 mm², height 31 mm: 80 SADC channels):
  - This space should be used only for digitizers
  - The cables/PCBs for bias voltages and the ASIC-power should be placed between the cooling plate and the support beam
- To eliminate input buffers of SADC, the direct DC coupling of APFEL ASIC to the SADC chip should be investigated
- An analogue addition of the signals from two LAAPDs may be considered if the required channel-density of digitizer module can not be reached.

Digitizer Module

- Mechanical dimensions are defined (forward endcap, barrel)
- The design of input buffers is in progress
- The EMC-digitizer prototypes are expected end by the end of 2011
- The existing SADC module (design of Pawel Marciniewski) will be used to develop firmware (time-synchronization and data-transfer protocol; test feature-extraction; etc)
- The STRUK SIS3302 commercial SADC modules with modified firmware will be used for test experiments

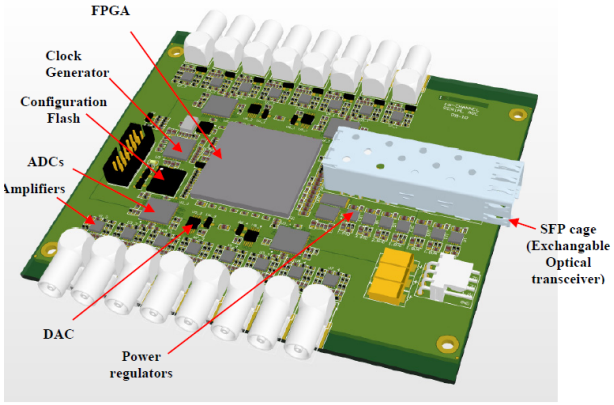
Multiplexer

- For the test experiments the multiplexer should have an interface to existing data-acquisition system.
- For the purpose of protocol development/test experiments it is possible to use existing optical link interface boards with VME/PCIE bus, prototype of the PANDA computing node?

Other Issues

Milestone

- Build first working prototype of readout chain (digitizer + multiplexer): **by the end 2011**



Hardware:

- SADC: 16 channels, 14 bit, 125 MHz, SODA compatible
- PANDA computing node as a multiplexer

First step: Definition of protocols (**collaboration with common with other subsystem?**)

Open-source firmware?

- The STRUK SIS3302 commercial SADC modules with modified firmware will be used for test experiments

Firmware development policy:

- open-source or closed source?
- Shell we use GPL/LGPL license?

Time-distribution System

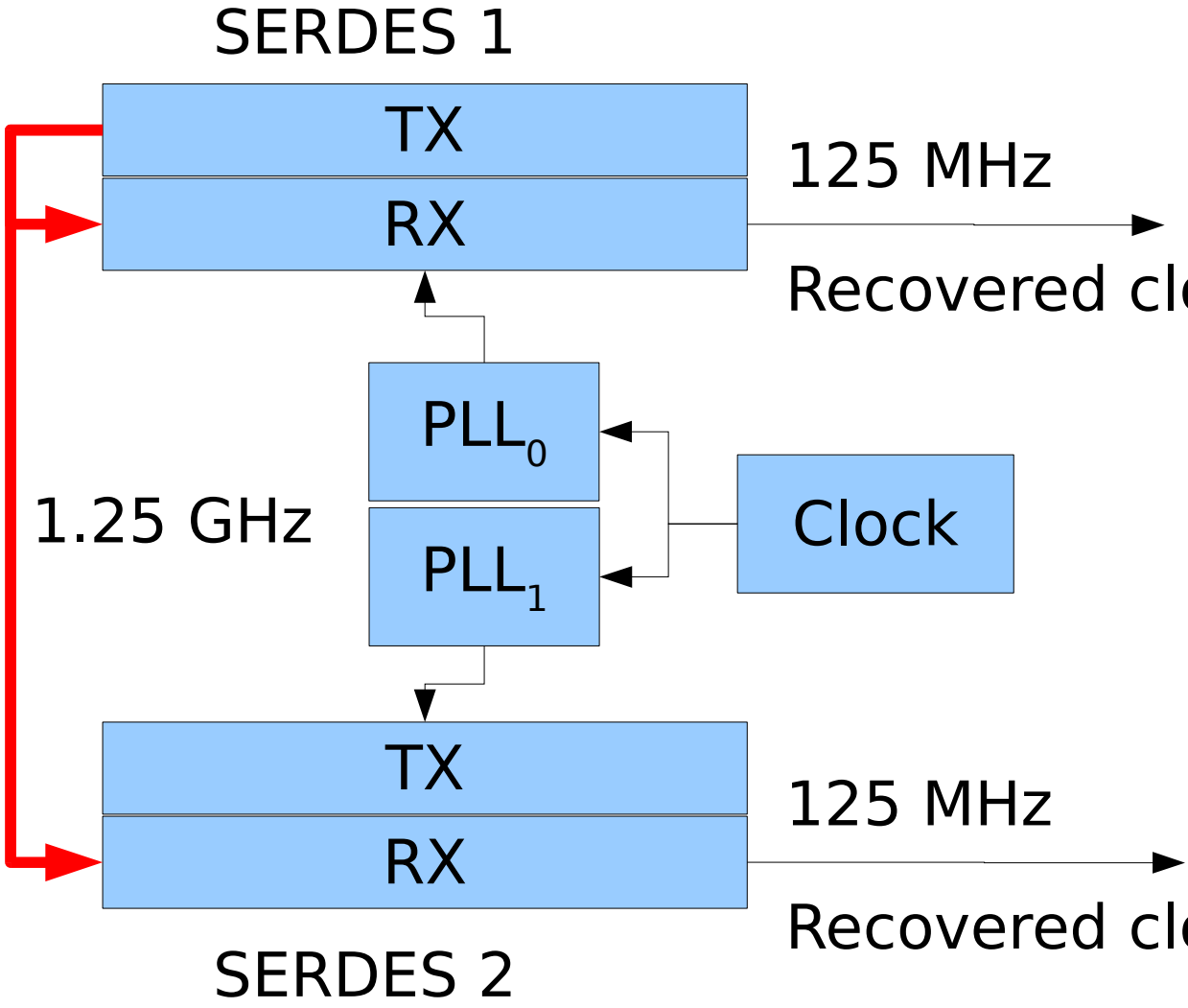
Is the clock-synchronization via optical link possible using Xilinx FPGA SERDES?

The investigation is done at KVI using Spartan-6 GPT SERDES

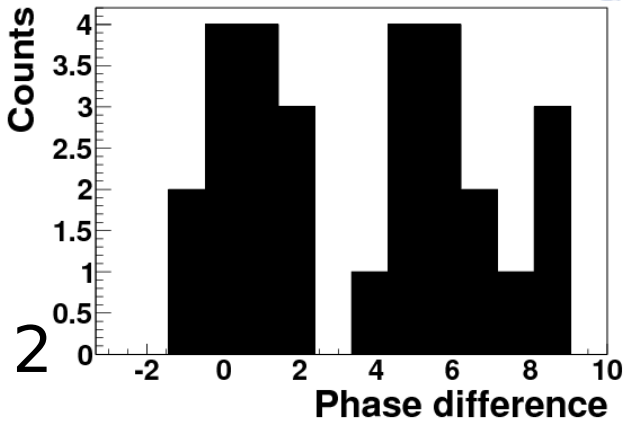
Test Setup

Spartan-6 FPGA
has 2 GTP SERDES

There is unambiguity in the phase of recovered clock (10 different possibilities)!



Phase difference after power cycles of the second SERDES



Test Setup

Further steps:

- Use two different test boards (to avoid using same clock for transceiver and receiver)
- Test the phase-difference detector unit (implemented in VHDL; is working in simulation)
- Apply same procedure for the Virtex RockedIO

KVI

university of groningen

GSI

Thank You for your Attention