Update on Readout for STS1 and Straws Detectors

Paweł Kulessa
(FZJ, IKP)

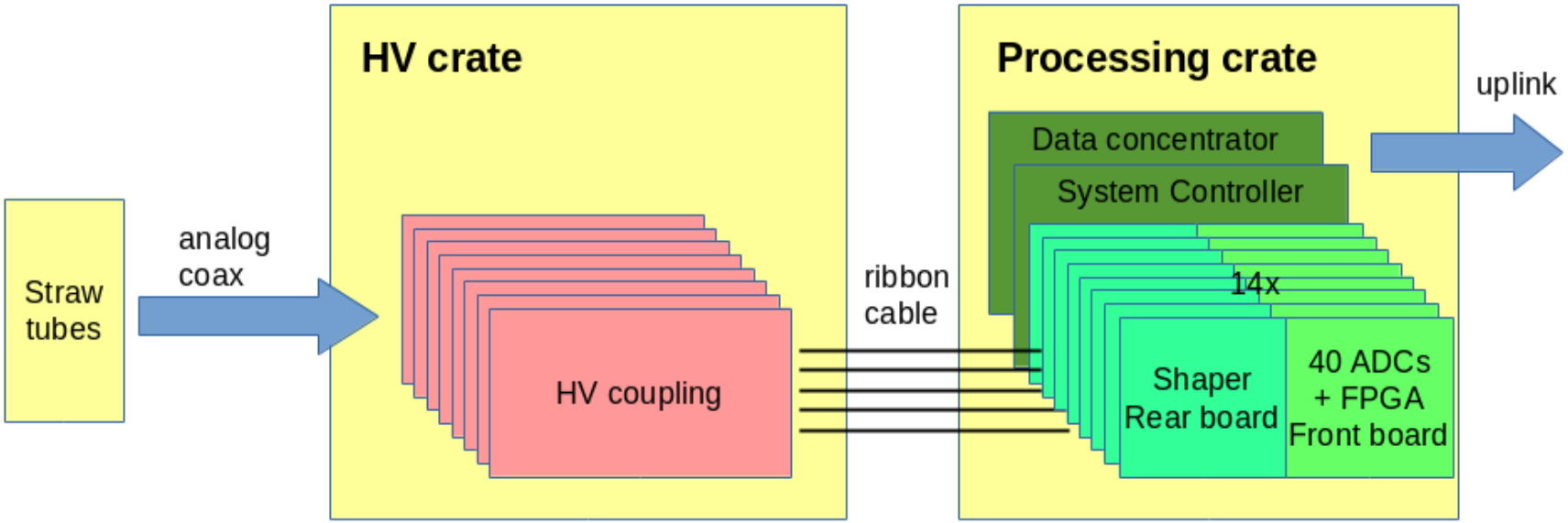
TOPICS

1. Front-end free sADC readout
   – HV decoupling crate modification

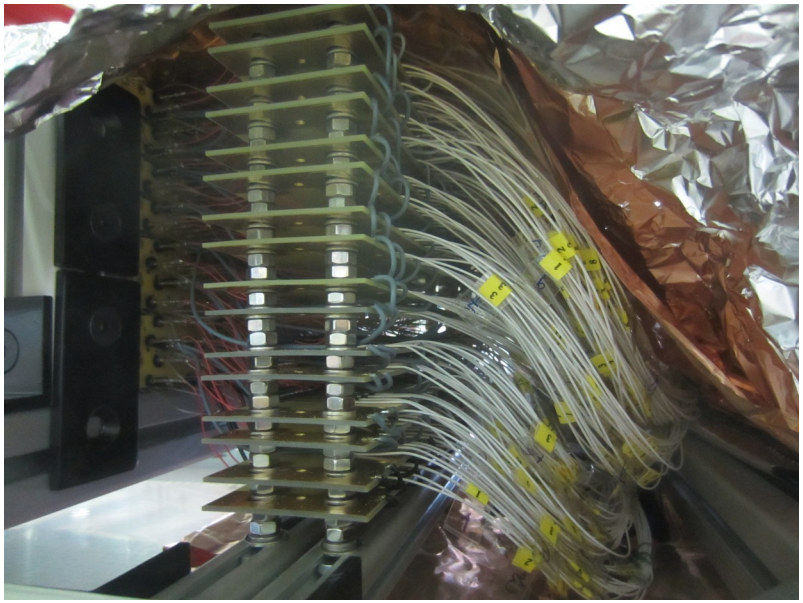
2. STS1 TRB3 readout
   – TRB3 crate modification for "advanced" triggers
   – trigger topology for STS1 tests
   – firmware modification (Jan Michel)
   – dabc/stream extension (Sergey Linev)

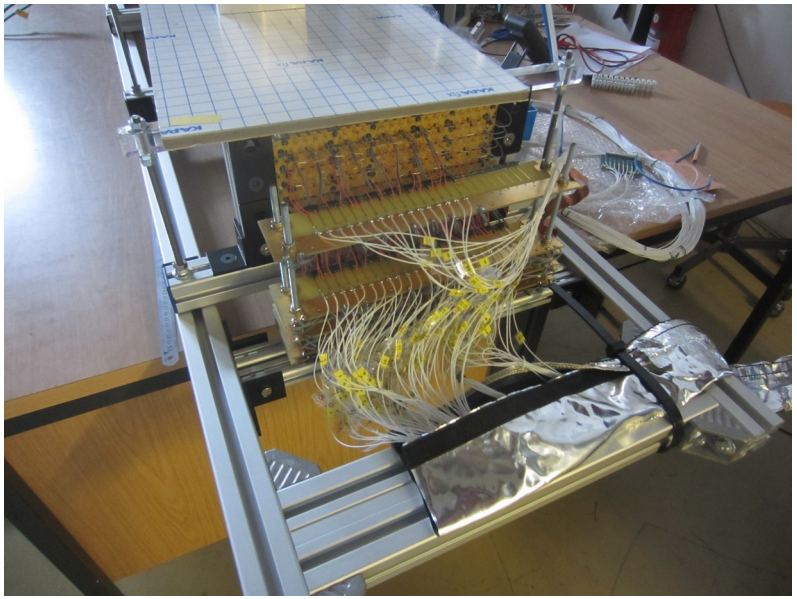
3. Summary

System overview I



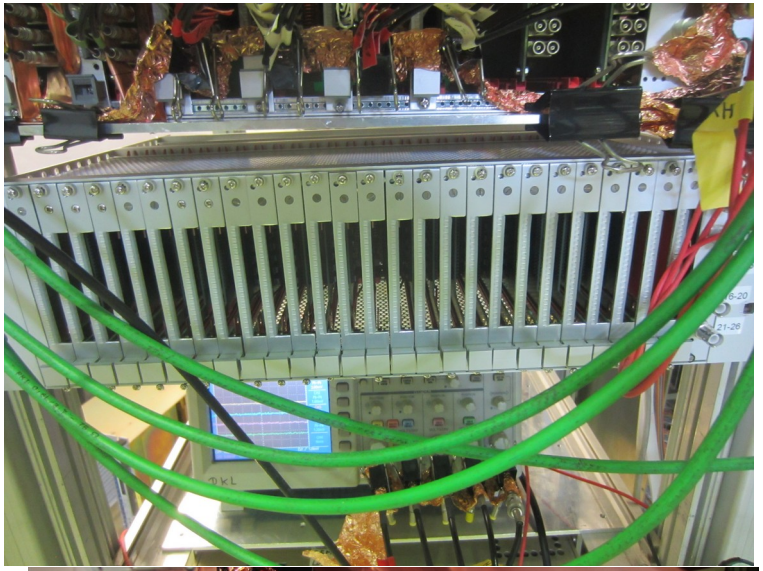
System overview II: detector side

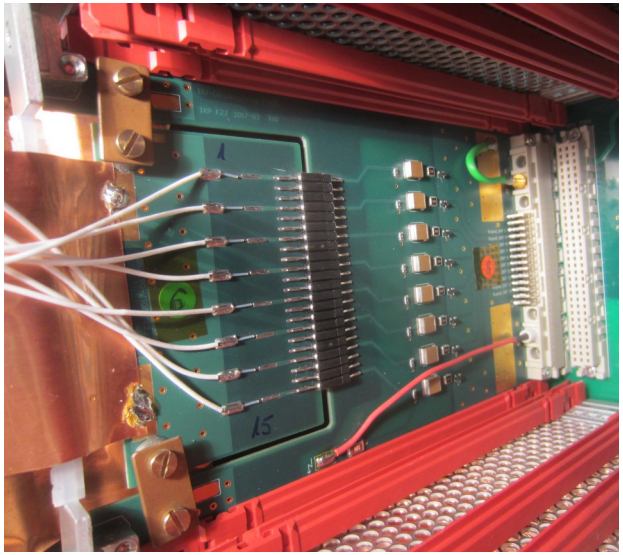


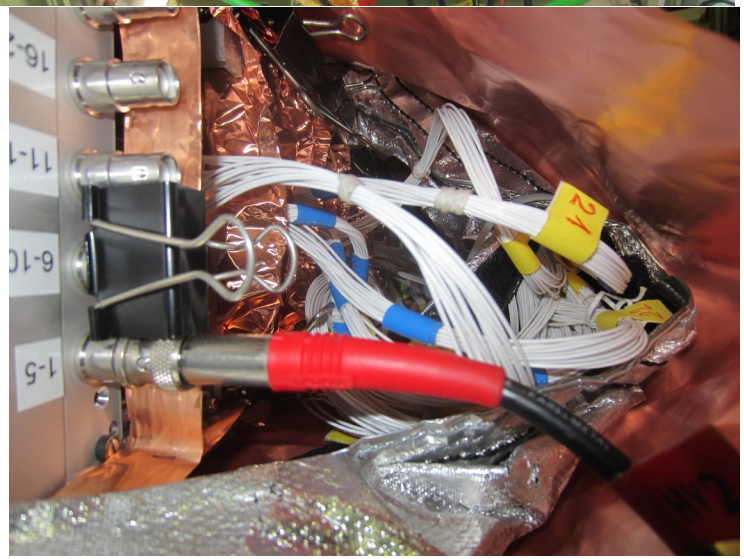


– no electronic components inside:
– no heat productions
– radiation hardness
– HV/signal granularity – single straw

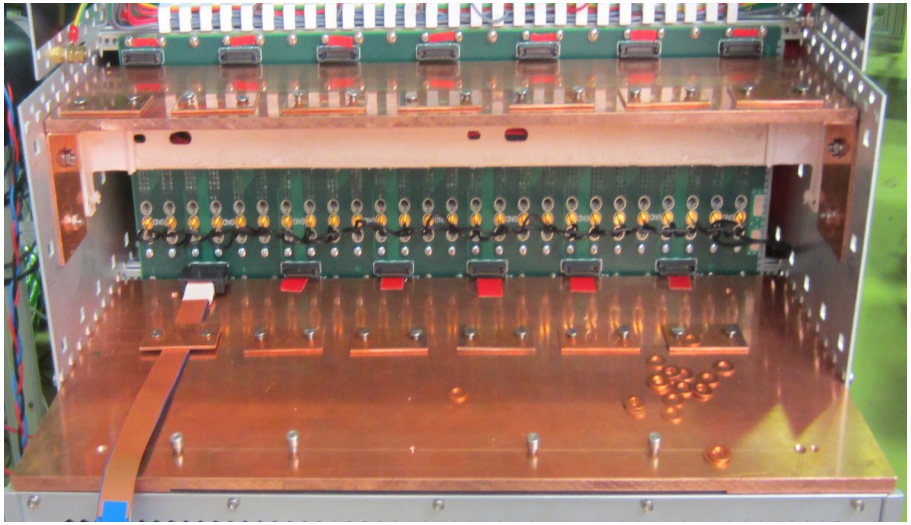
HV crate

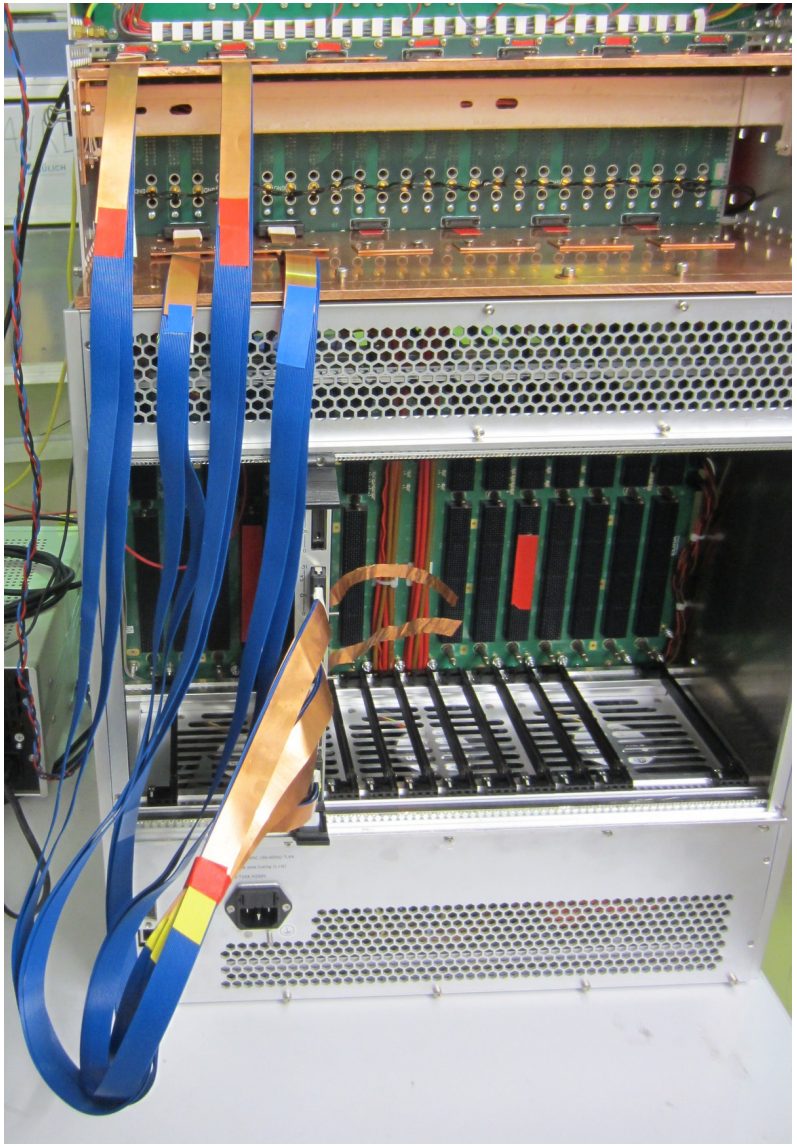




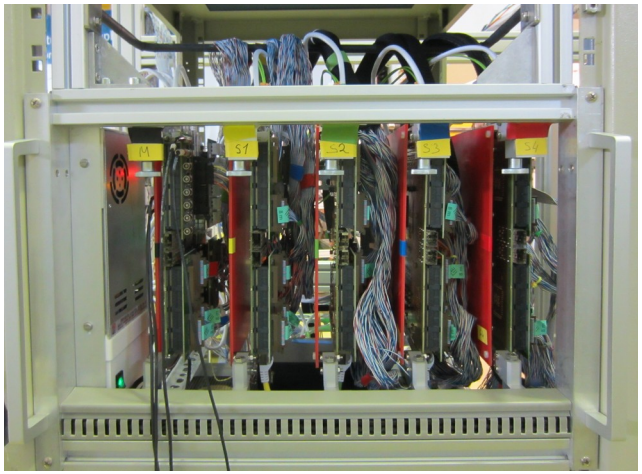


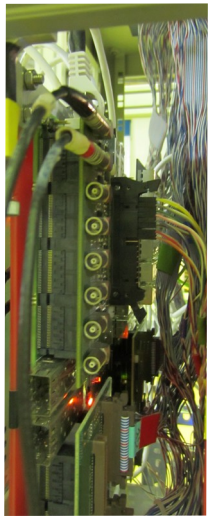
HV crate after modification:

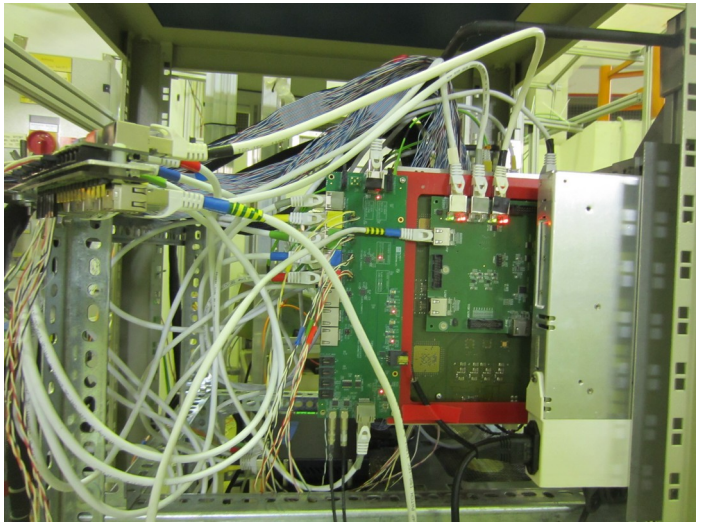


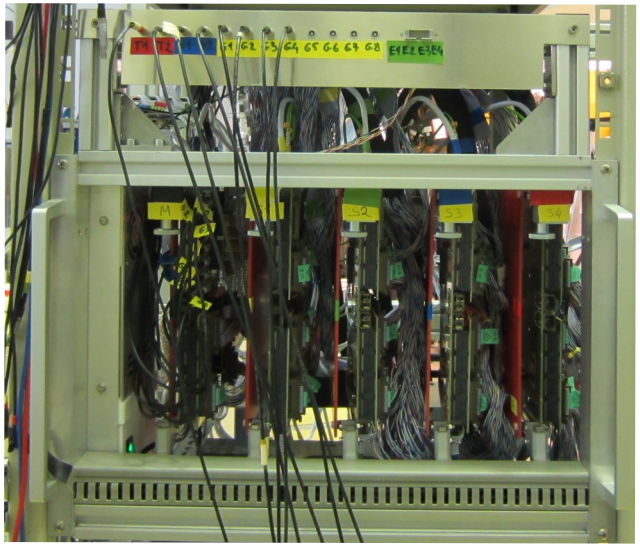


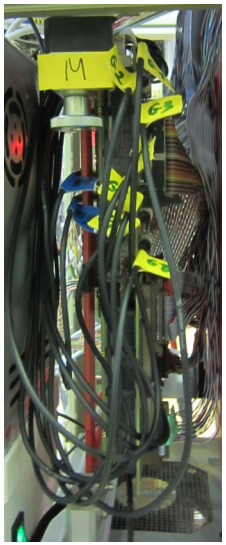
TRB3 crate additional modifications – input panel

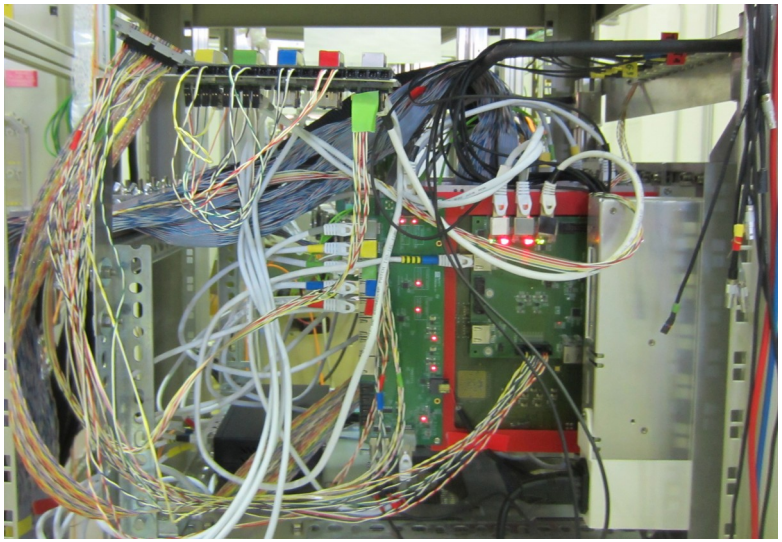




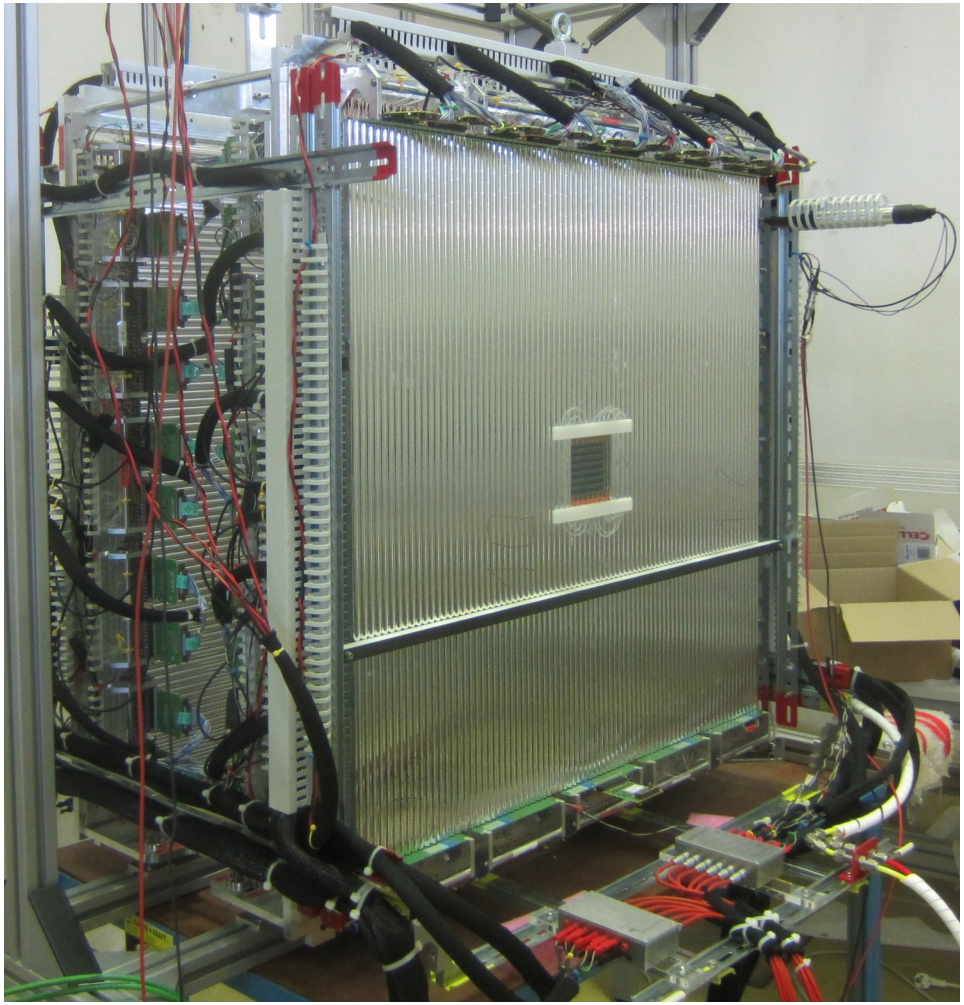






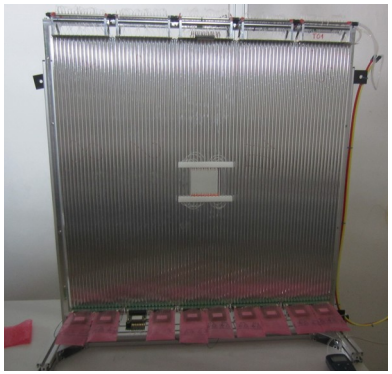
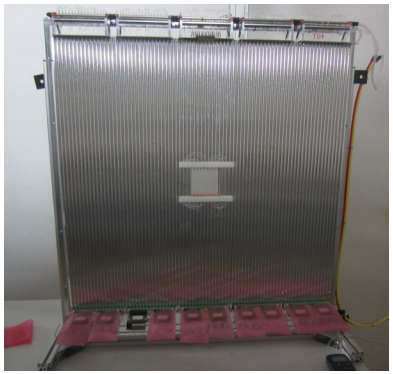
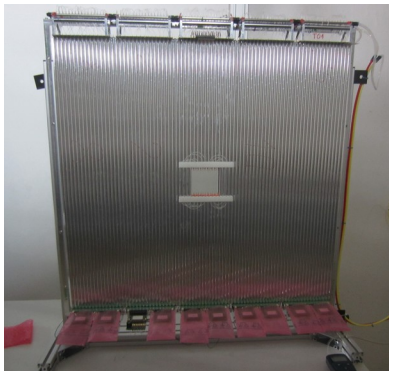
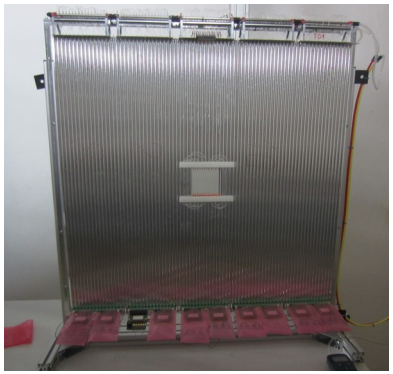


Detector layout

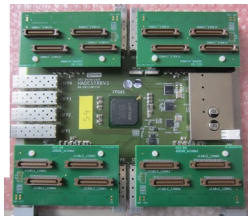
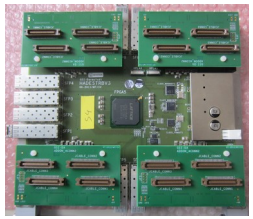
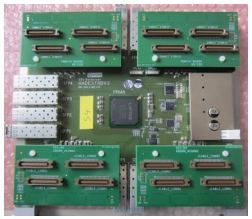
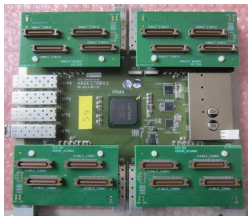


– 8 layers
– 4 planes – one double layer
– 16 “cuted” straws
– 11 ASIC per plane
– one TRB3 board per plane
– 3x3 + 1x2 ASIC per TDC
– all planes have same geometry and readout topology

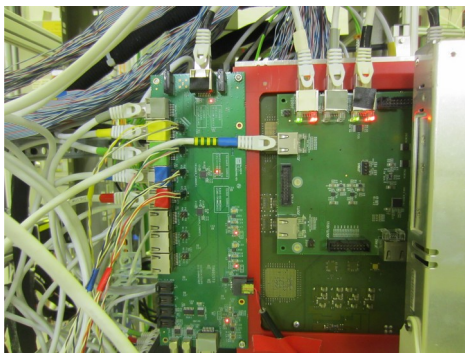
Readout topology I

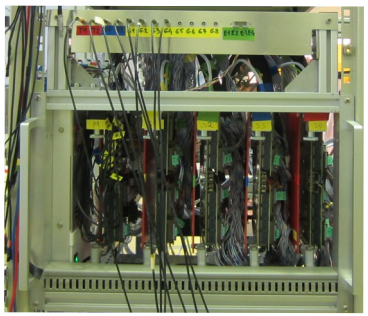





TDC
4x4
Tout

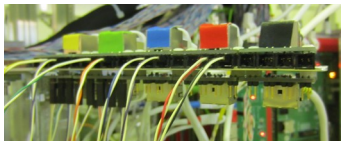





CTS
16Tin
4 NIM
4 ECL






Readout topology II



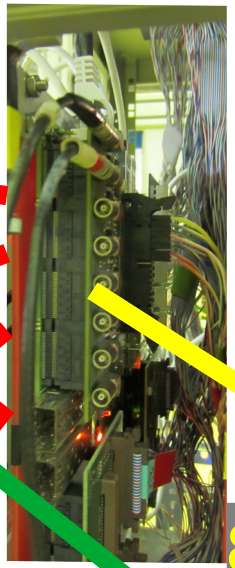
4x48--52

4x48--52

4x48--52

4x48--52

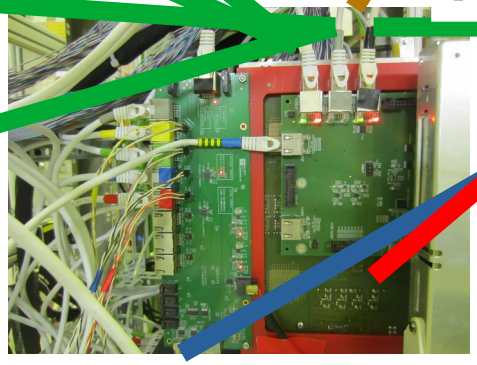
4x2

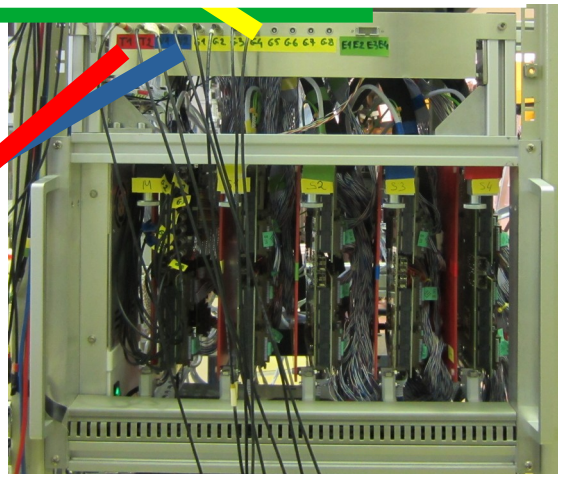


8 NIM

CTS

4 ECL + 2x2 NIM





4x2

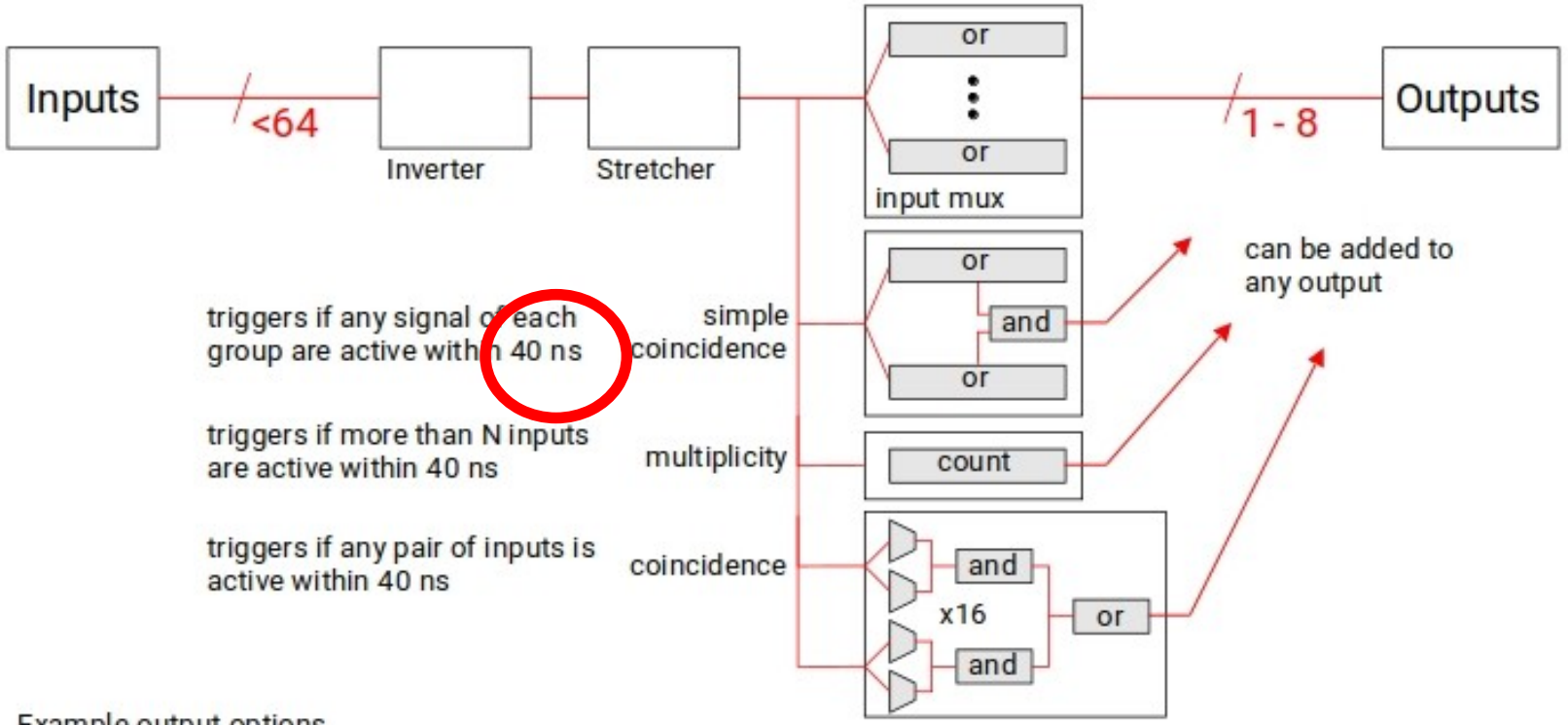
Triggers:

TDC and central FPGA:
- **straws OR for each layer**
- **AND between first and last straws in plane**
- **multiplicity per TDC**

GPIN:
- **plane trigger (OR of layers)**

CTS:
- **trigger from scintilators (AND, OR ..)**
- **coincidences between scintilators and straws**

TDC and central FPGA trigger logic – old design

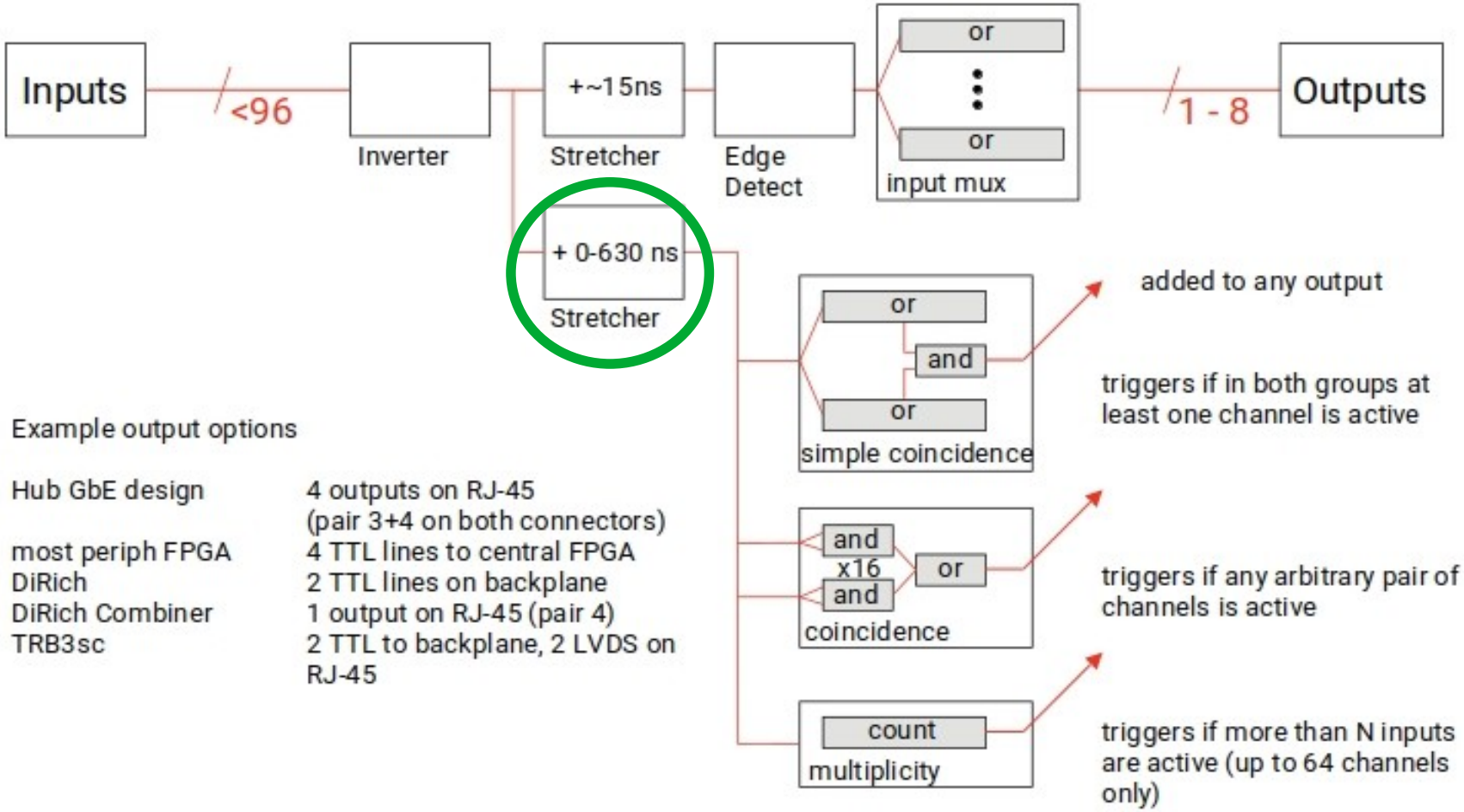


Example output options

Hub GbE design	1 output on RJ-45 (pair 3)
most periph FPGA	4 TTL lines to central FPGA
DiRich	2 TTL lines on backplane
DiRich Combiner	1 output on RJ-45 (pair 4)
TRB3sc	2 TTL on backplane, 2 LVDS on RJ-45

trigger generator
version 2017-02-03

TDC and central FPGA trigger logic – new design



Example output options

Hub GbE design	4 outputs on RJ-45 (pair 3+4 on both connectors)
most periph FPGA	4 TTL lines to central FPGA
DiRich	2 TTL lines on backplane
DiRich Combiner	1 output on RJ-45 (pair 4)
TRB3sc	2 TTL to backplane, 2 LVDS on RJ-45

Other modifications:

GPIN:

– same modifications as for TDC

CTS:

– correction of CTS addon inputs
– longer coincidence window (>600ns)
– different trigger channels allocation

Software modifications:

- additional “Monitor” module – possibility for include counters values in .hld files using trbcmd, readout period configurable

- additional option in dabc for stopping data taking after selected number of events

Summary

Front end free sADC readout

- **new better grounding in HV decoupling crate**

STS1 TRB3 readout

- **modifications in TRB3 firmware for straw tubes (CTS, TDC, GPIN, central FPGA) gate length, 4 trigger outputs per TRB3 board**
- **dabc/stream software modification for storing counter rates in .hdl files**

- **TRB3 using for new HADES detector test (SIMP with PADIWA)**

Thank you