Update - LHCb OT in PANDA

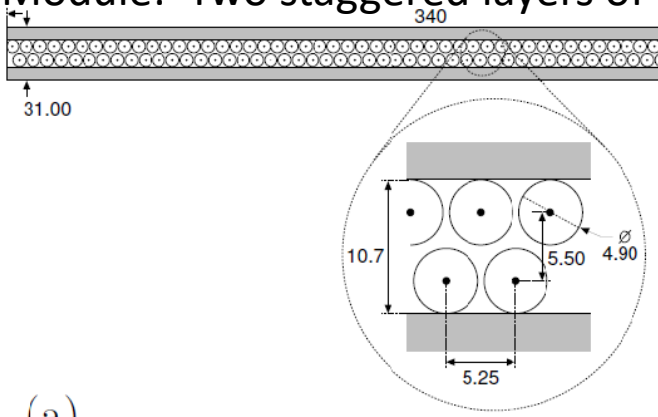
Components at GSI

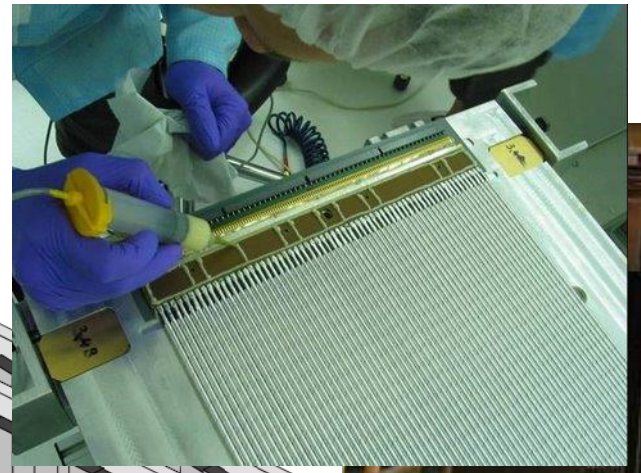
Update on FEE Interface

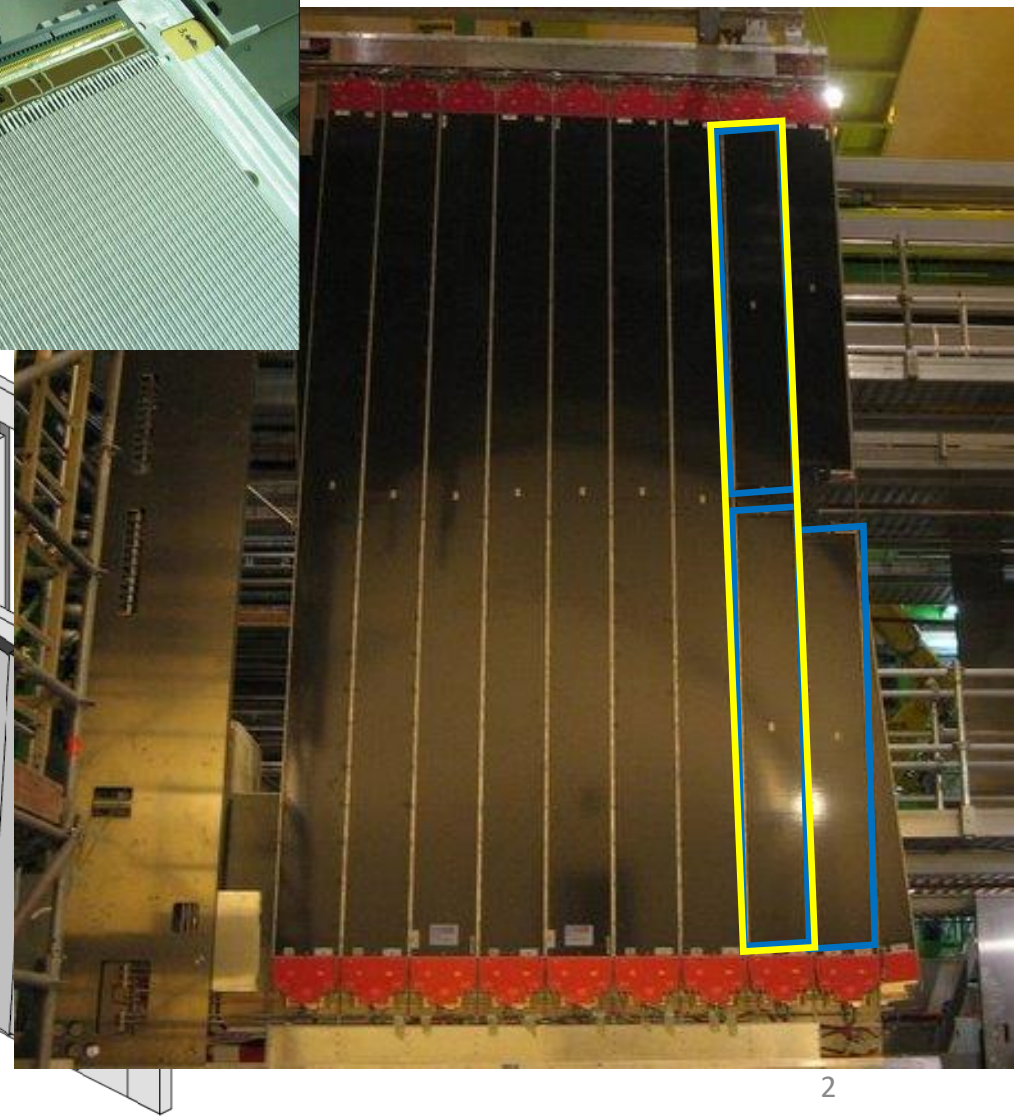
Work in Progress

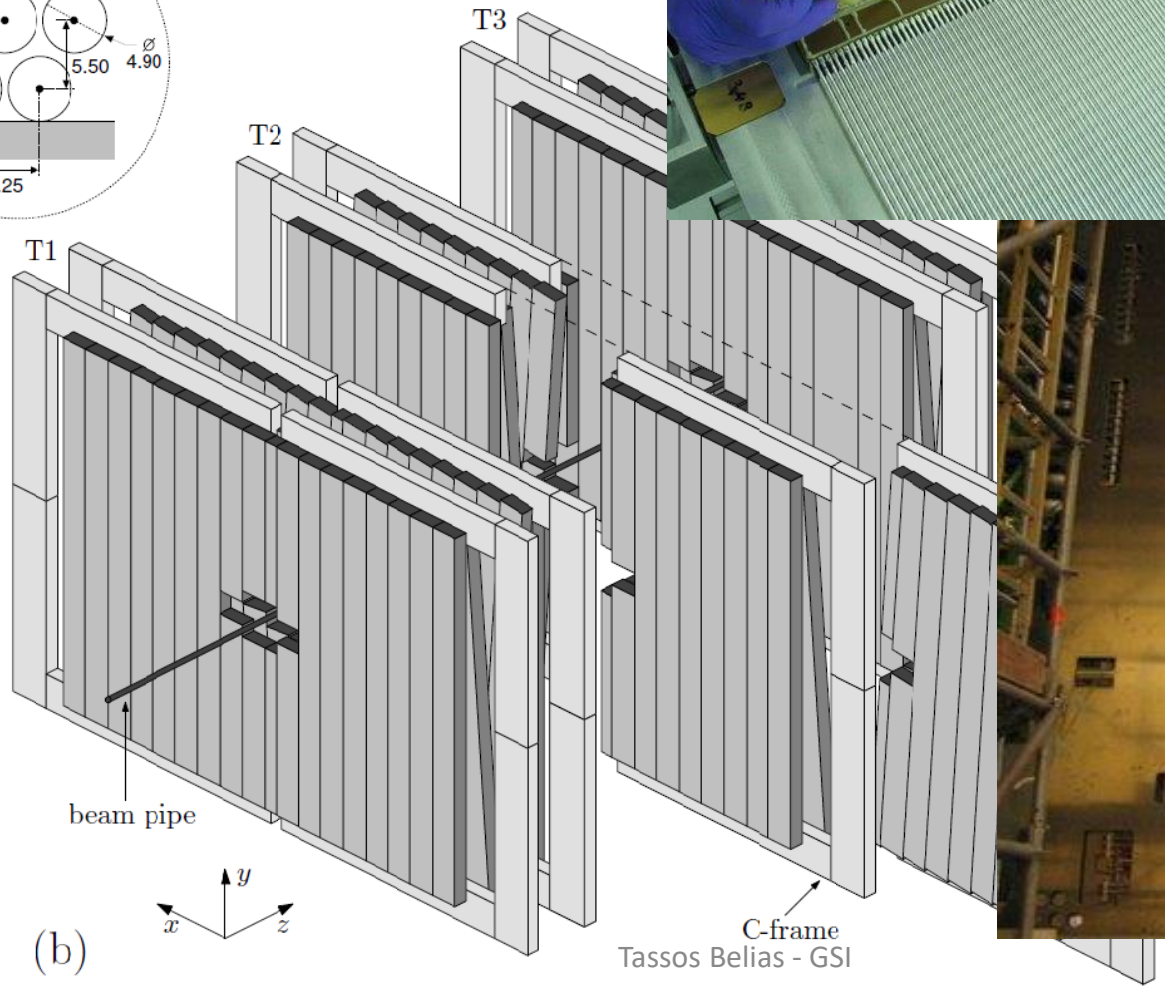
LHCb – Outer Tracker (OT)

Module: Two staggered layers of 64 straw tubes







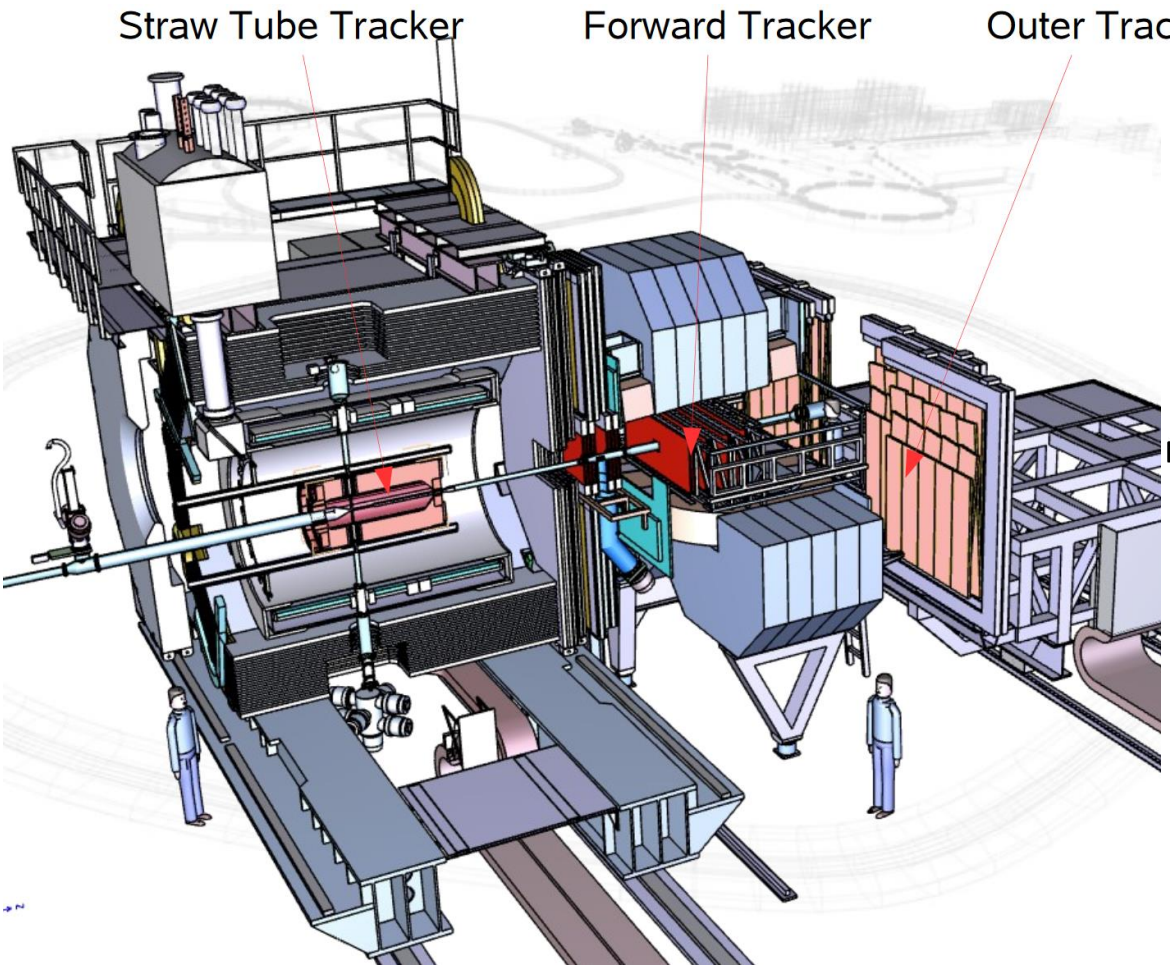


Straw tubes are arranged in a gas-tight enclosure.

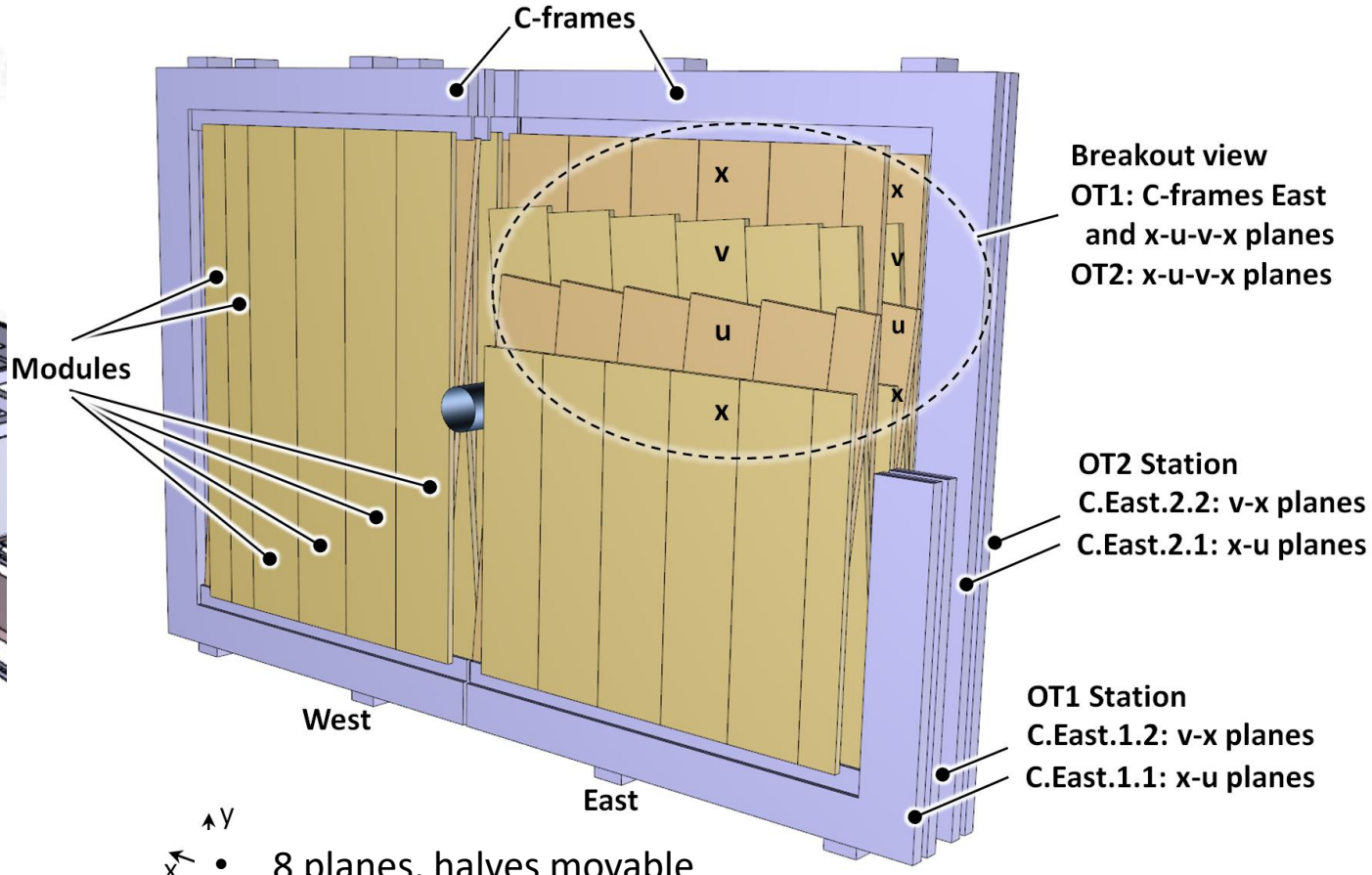
Enclosure height: 5m !

Enclosures close to the beam pipe can be safely separated to get two **short modules for use in PANDA**.

LHCb OT short modules in PANDA as FT5/6 on Day-1

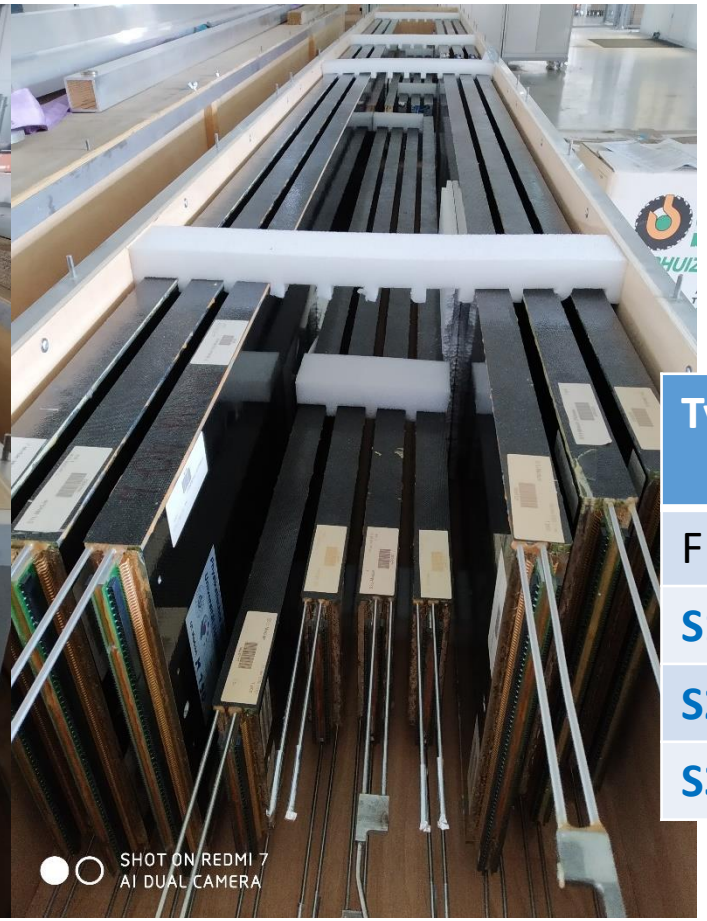


PANDA Stations of short OT modules – CAD drawing



- 8 planes, halves movable
- 4.4 x 2.3 m^2 (w x h) /plane
- x, u, v, x (0°,±5°, 0°)

OT – Detector modules spares at GSI



LHCb OT spares of
30 modules are at GSI.

The S-type modules will
be prepared for PANDA.

Type	Length (m)	Width (m)	Count
F	4.8	0.34	30
S1	2.4	0.34	12
S2	2.3	0.34	10
S3	2.3	0.17	8

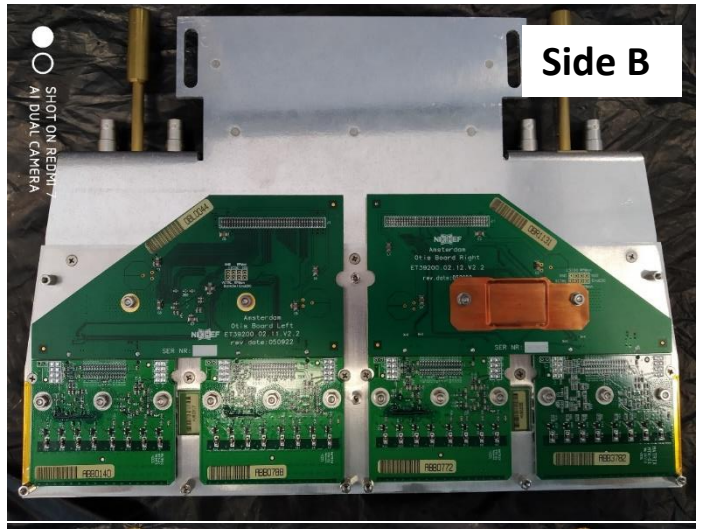
OT – HV units

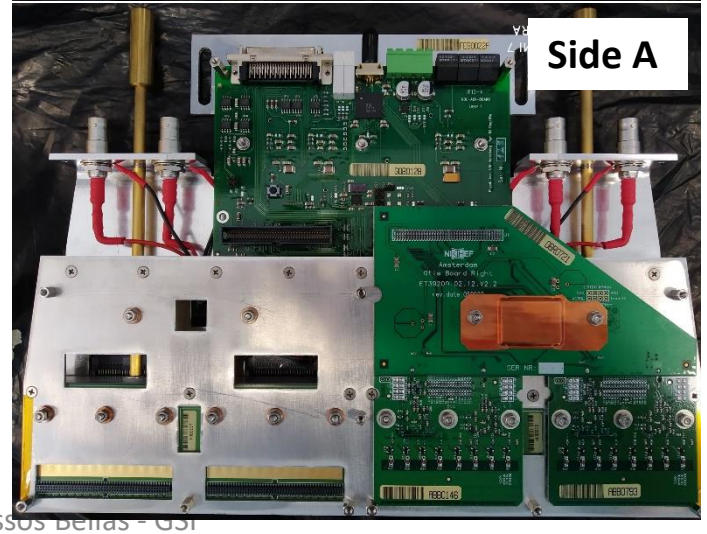
LHCb OT actual HV units
and modules are at GSI.

Two mainframes
CAEN SY1527LC
and eight HV units
CAEN A18338PLC
and a cable junction-box.

These units were used
for the whole OT.

OT – Readout Units





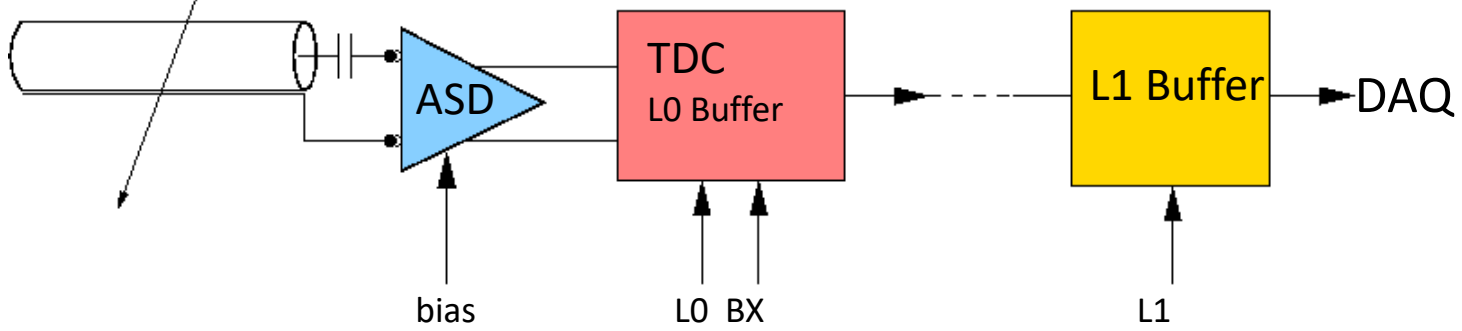
LHCb OT spares of
14 readout units at GSI.

The S-type modules
envisaged for PANDA
use one-sided readout.

The readout box contains
HV cabling and FEE boards.

The box geometry and the
mechanics inside must be
kept to fit on a module.

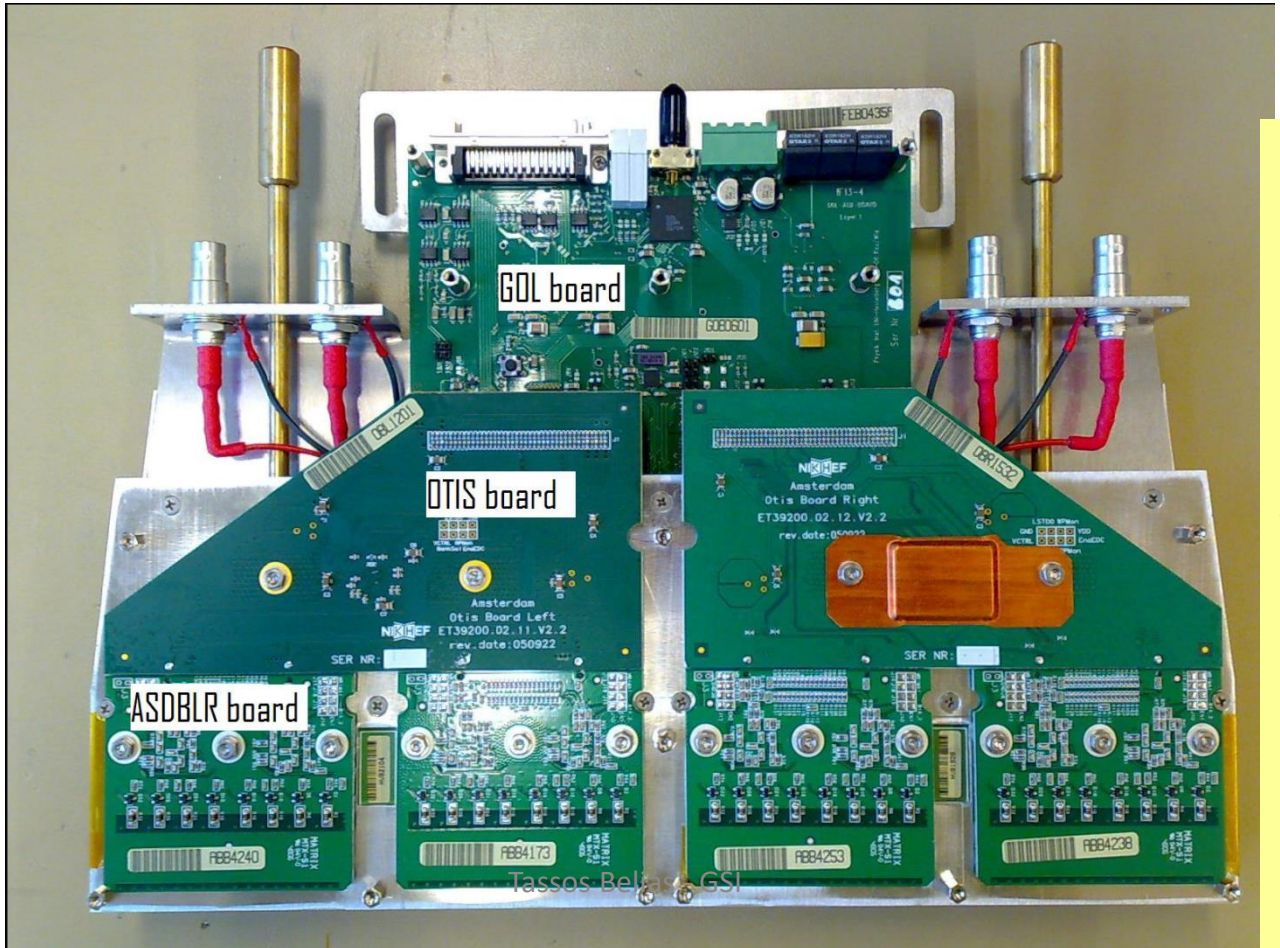
LHCb OT - Readout



GOL - opt. link out, interface controls and power

OTIS - TDC ASIC, 32 input ch., drift time measure, keep data until L0 trig.

Amplifier Shaper Discriminator BLR ASIC, 8 input ch., dig. drift time signals out (thr.: 3fC, 40mW/ch.)



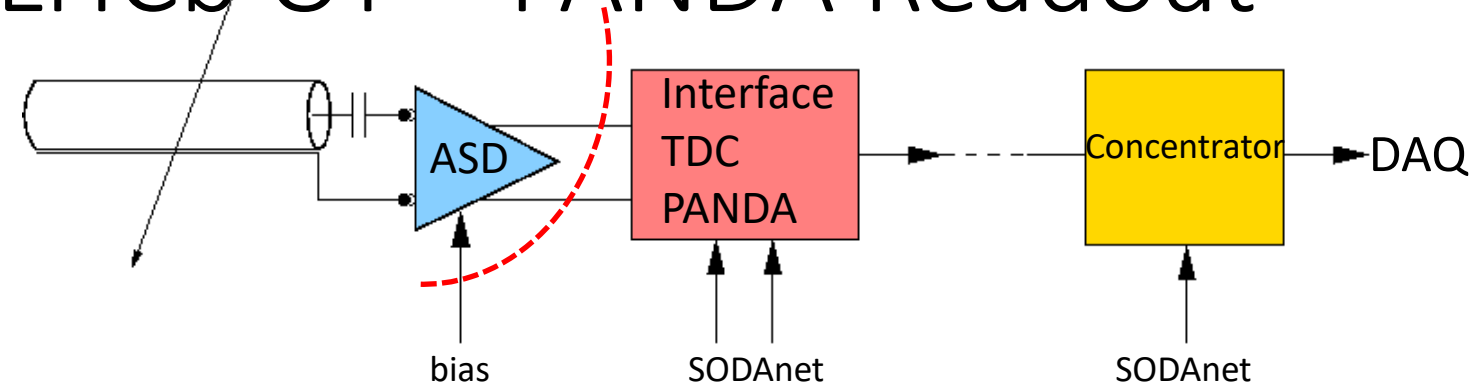
1 optical link, 1.28 Gbit/s

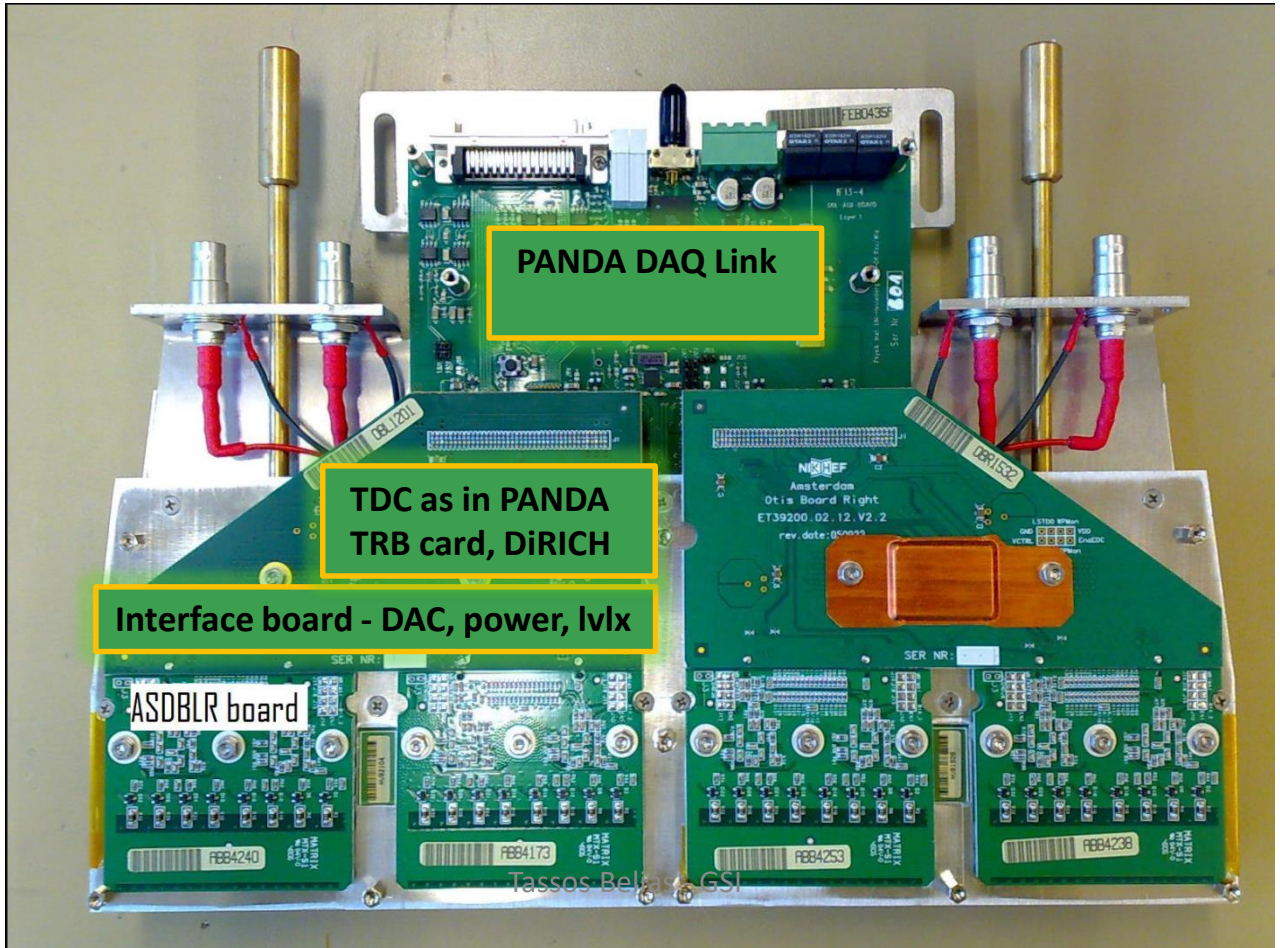
4 OTIS TDC chips, 32 ch./chip

16 ASDBLR chips, 8 ch./chip (2 chip/board)

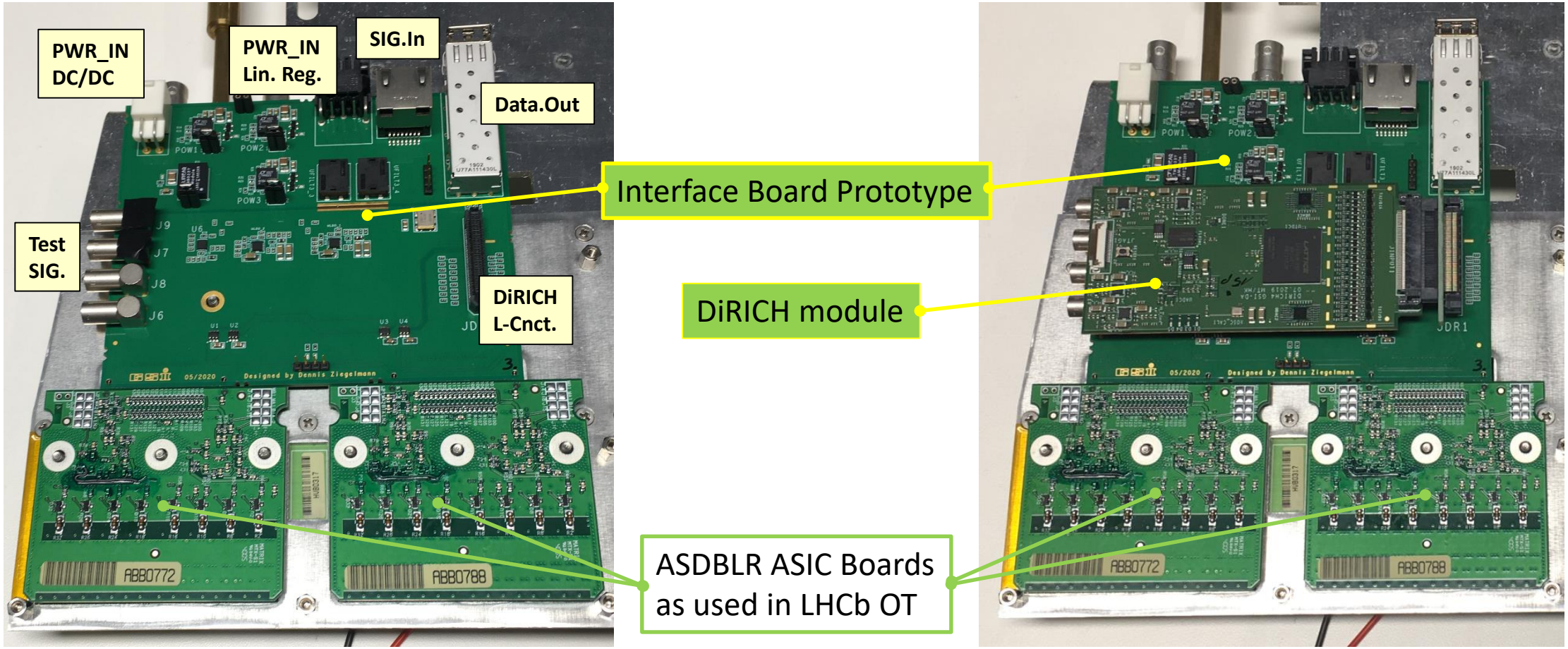
Input: 2 x64 ch.

LHCb OT – PANDA Readout

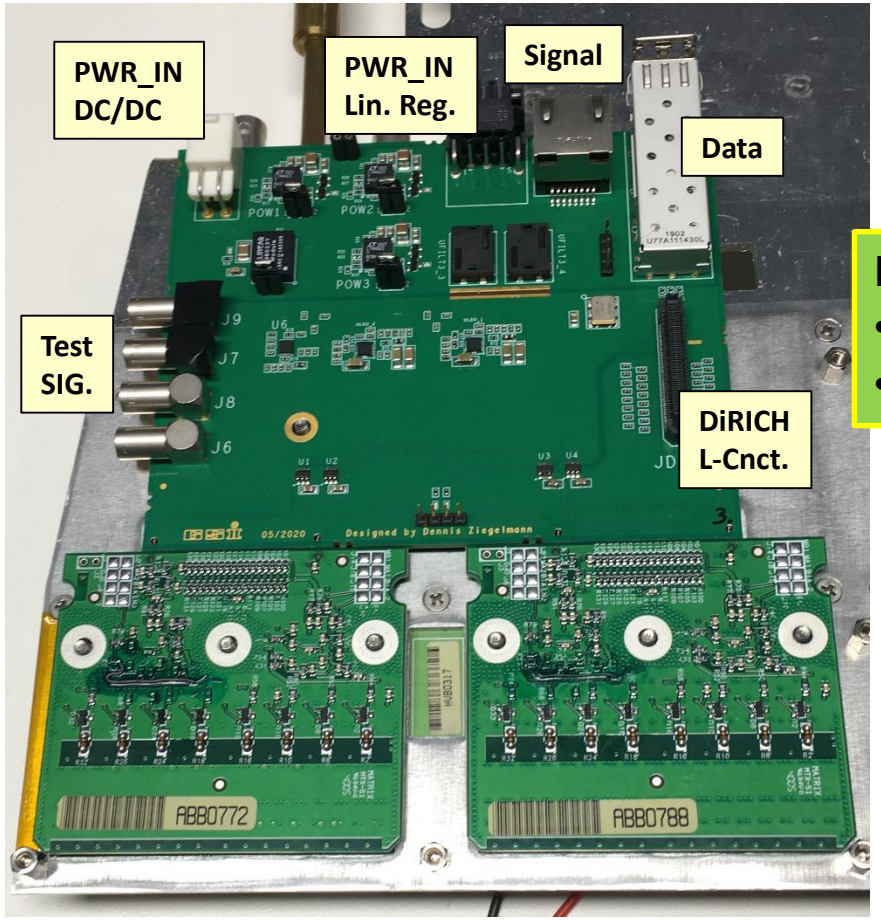




PANDA Interface to LHCb OT FEE



PANDA Interface to LHCb OT FEE



Interface Board Prototype
- Three boards produced
- Hardware checks started

ASDBLR ASIC Boards as used in LHCb OT

Interface board prototype –
Dennis Ziegelmann (MSc, Darmstadt Uni.)
with Michael Traxler (GSI)

- Power – DC/DC or Lin. Reg
  - ASDBLR ASIC boards (two, 32 ch.)
  - DiRICH module (one, 32 ch)
- Signal & Data transmission
  - ASDBLR ASICs to DiRICH
  - TRBnet signal (CTS)
  - SFP cage (2 Gbit/s SERDES link)
- Settings / Operations
  - DACs for ASDBLR ASIC thresholds
  - I/O Test pulse connections
- Size & shape constraints
  - Spacing between ASDBLR boards
  - Fit within FEE box
  - PCB, 8-layers, 120x100mm^2

LHCb OT in PANDA – Work in Progress

- Readout FEE
  - Interface board prototype produced at GSI
  - Hardware checks of interface board prototype → consolidated version
- Interface to DAQ and DCS
  - Starting with small-scale set-ups
- Mechanics
  - Dis-assemble an OT module & re-assemble for use in PANDA
  - C-frames design and production by SLRI Thailand groups
- Operations
  - Drift-gas, HV and test equipment for basic checks of OT modules

Tracking stations in addition to PANDA

– Using all large OT modules: Cosmics & more

FUTURE

- Dismantle OT and transport to GSI (~2021/22++)
- Check & Assemble OT modules in stations for installation in PANDA