



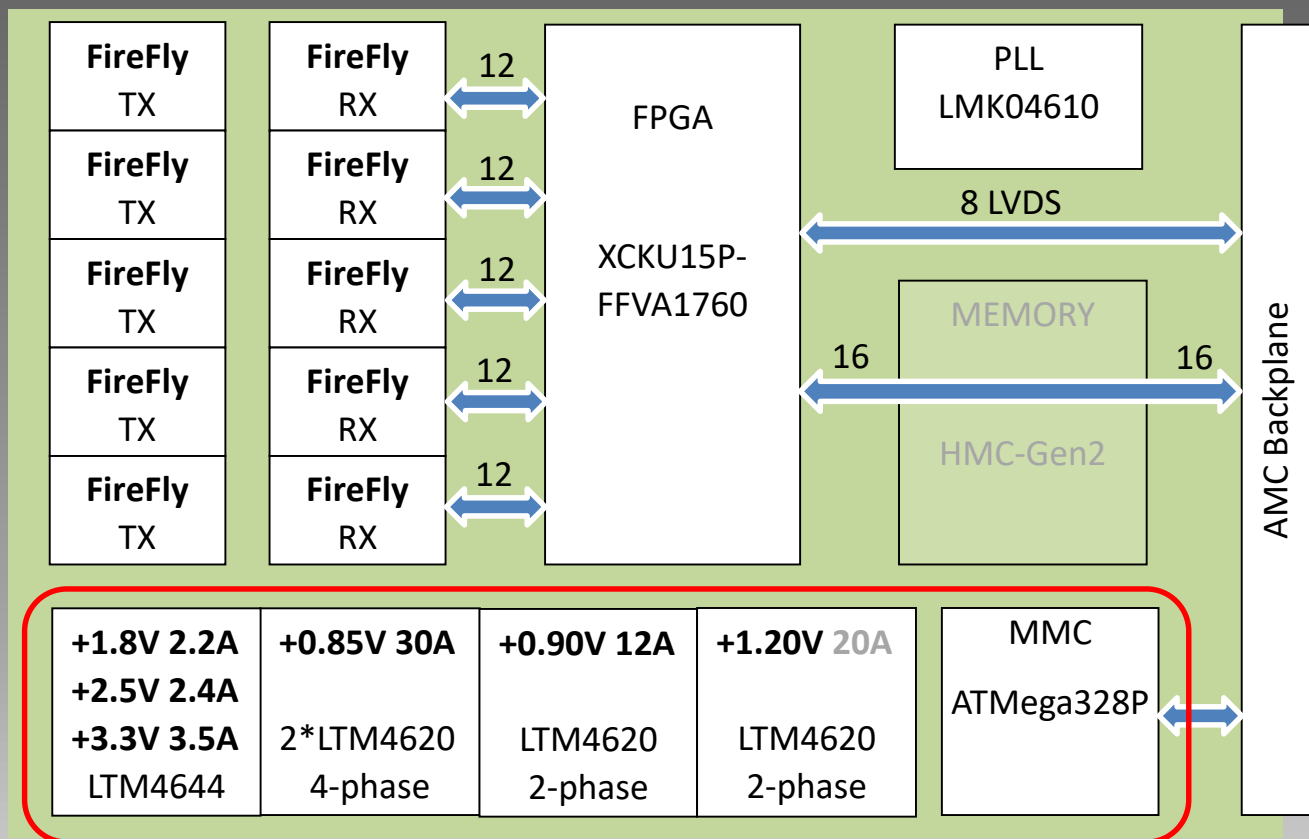
Status of the DAQ electronics for the PANDA

- From Uppsala

- PANDA DC
- LVDS ROB
- Crate Electronics
 - Backplane
 - Power Supplies
 - Crate Controller

Panda DC

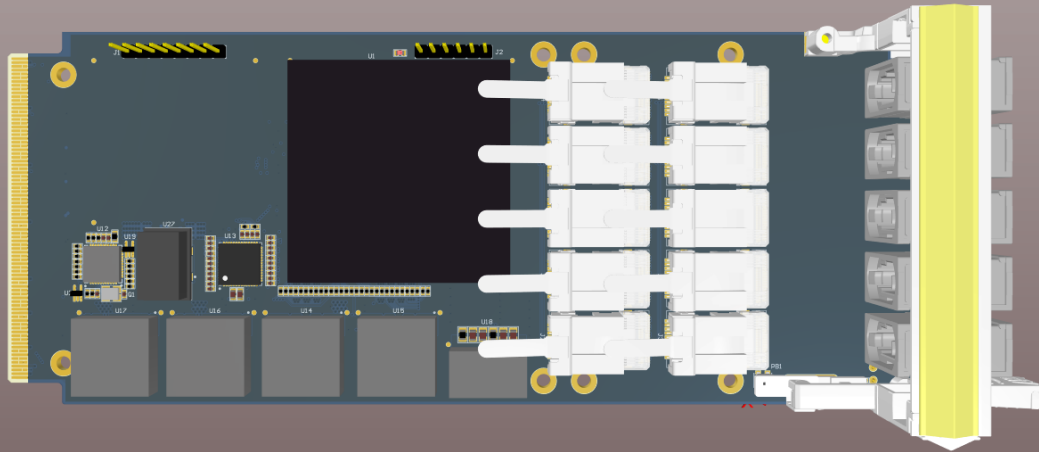
60 x 14 Gb/s



16 x 14 Gb/s

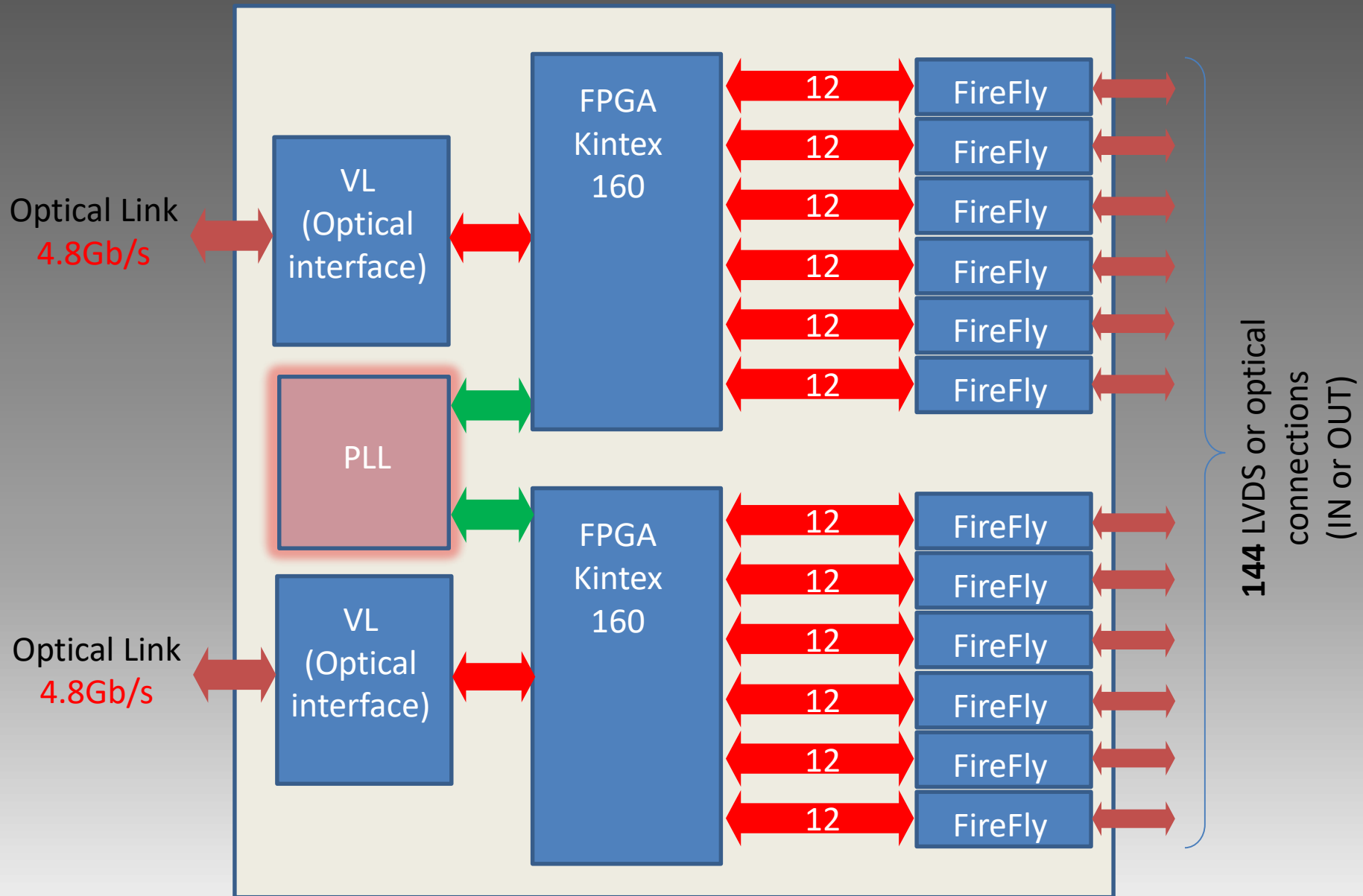
Status

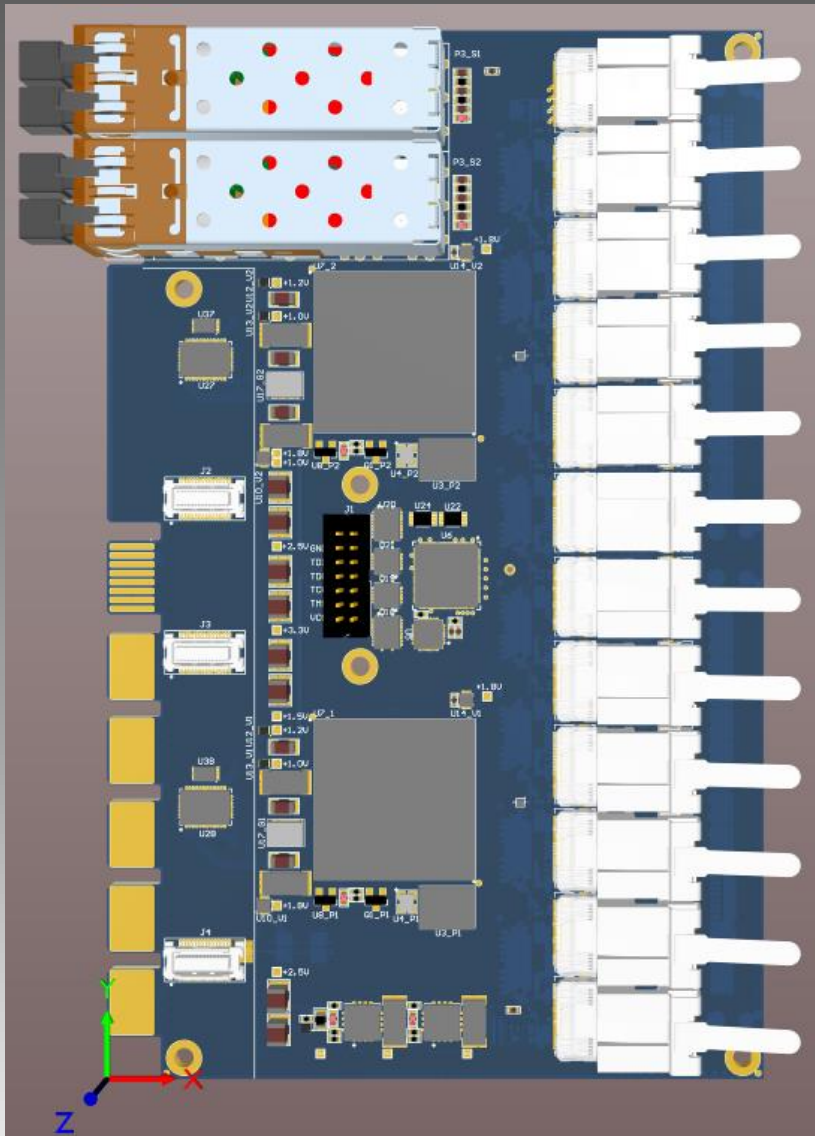
1. The device is in production. Delivery of the first assembled device is scheduled: 30.11.2020
2. The FPGAs are purchased (10 pcs)
3. The FireFly modules (non-standard pig-tail lengths) are purchased
4. Remaining is:
Testing and programming





- LVDS ROB

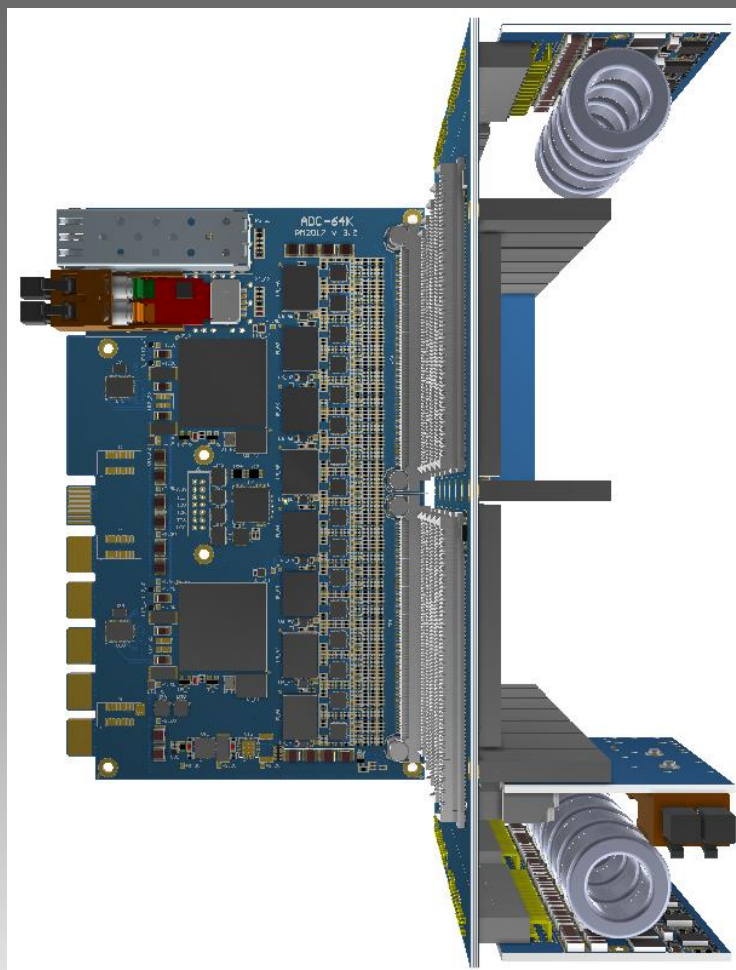




Status:

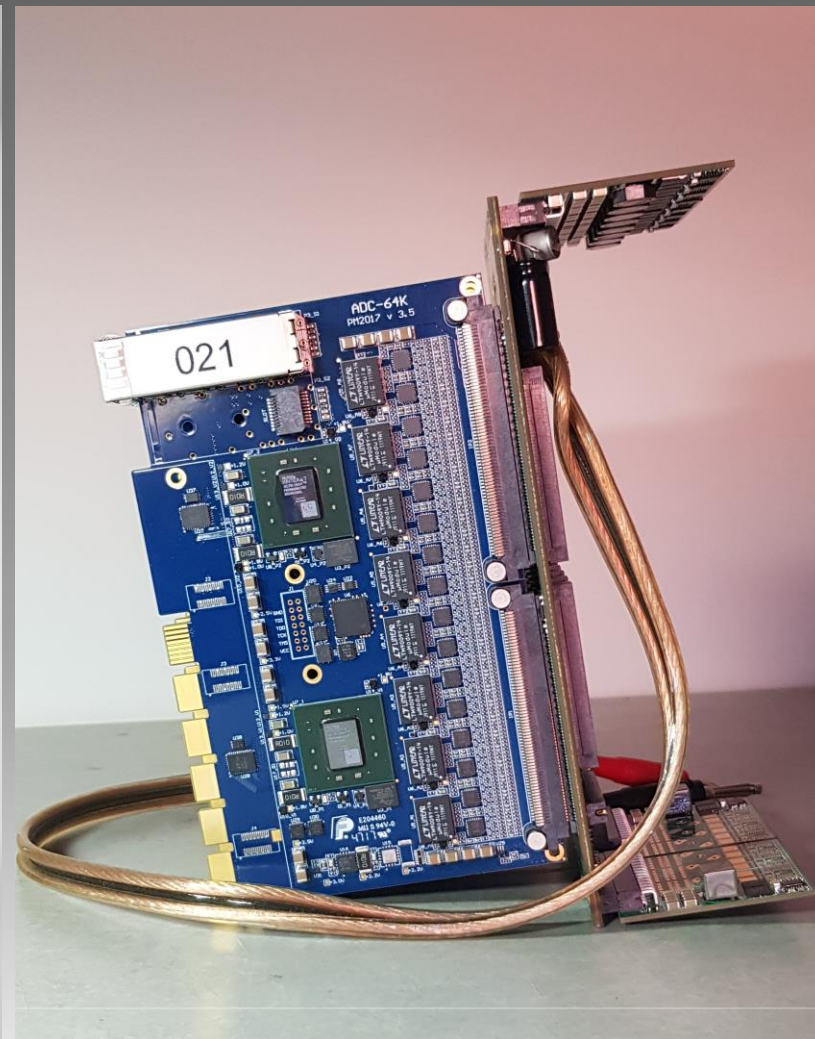
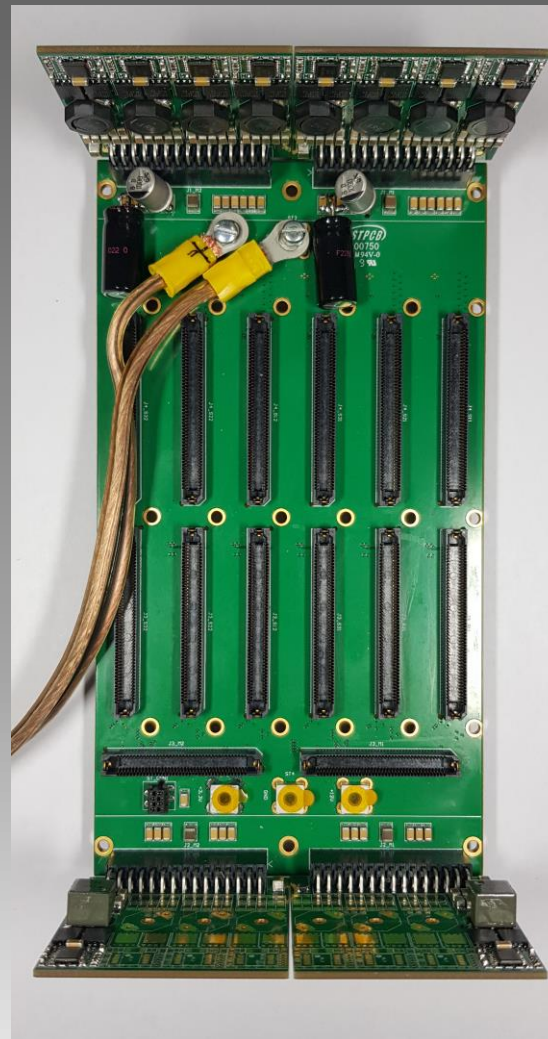
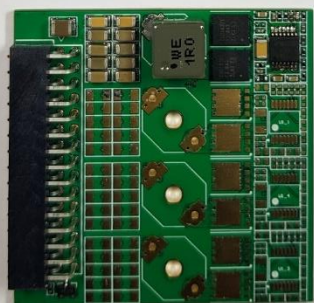
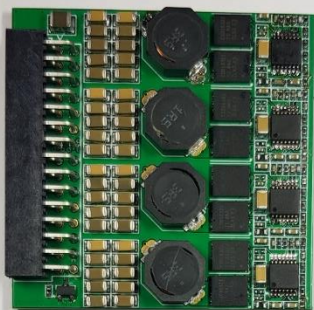
- Design obtained from the 64-channel ADC for the EMC Forward Endcap
 - 90% of necessary work done
 - To be submitted for production in the first week of November
-
- Samtec ECUE (12-channel)
 - safe transfer with buffers (400 Mb/s)
 - AC transfer up to 1.2 Gb/s up to 3 m
 - 144 I/O

ADC Crate Electronics



- Rear crate compartment electronics

Backplane and Power



Rear crate compartment electronics

Status:

Power supply

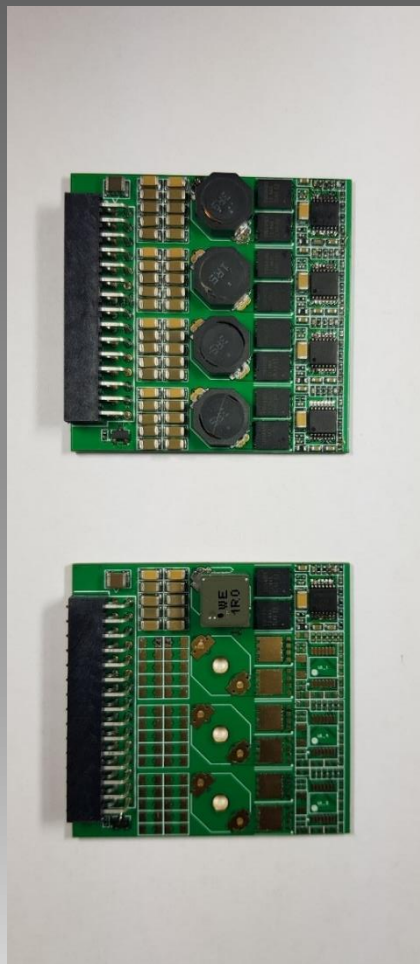
- Good efficiency (90%)
- Coils need manufacturing (winding) and testing
- Irradiation tests pending (applied for at KVI)

Backplane

- Will need some small modifications to comply to the new crate controller

Assembly

- Cooling tests pending

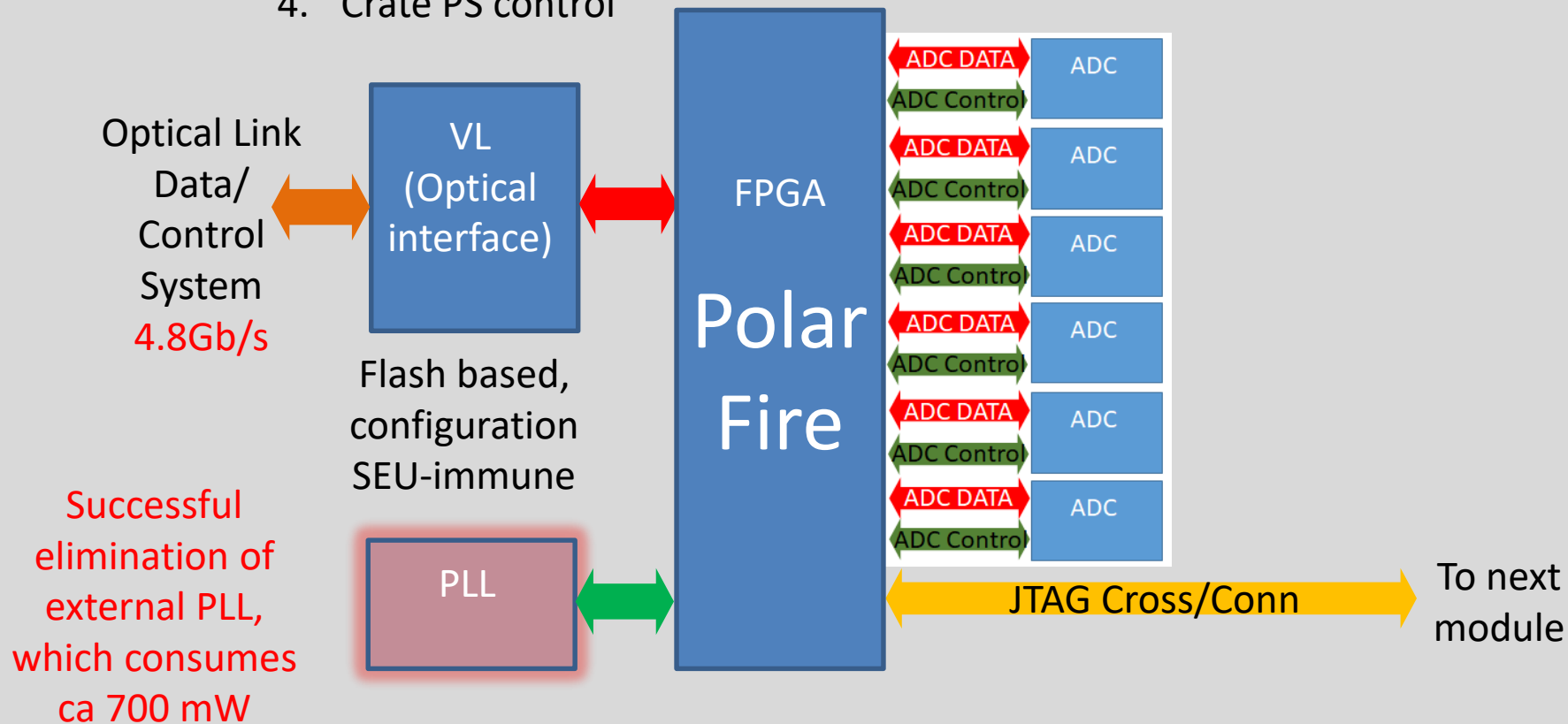




- PolarFire –based Crate Controller

Crate Controller

1. Direct JTAG configuration of individual ADCs
2. Reaction to SEU
3. Health control of ADCs (voltages, currents, temperatures)
4. Crate PS control





- Evaluation card with Libero development system

Libero - C:\Users\install\Desktop\sina\projects\Libero\Polar\XCVR - 5G-2G-PERFECT\XCVR.prjx*

Project File Edit View Design Tools Help

Design Flow

Top Module(root): TOP

Active Synthesis Implementation: CHIPSCOPE

Tool

- Create Design
 - Create SmartDesign
 - Create HDL
 - Create SmartDesign Testbench
 - Create HDL Testbench
 - Verify Pre-Synthesized Design
 - Simulate
- Constraints
 - Manage Constraints
- Implement Design
 - Open Netlist Viewer
- Synthesize
 - Verify Post-Synthesized Design
 - Generate Simulation File
 - Simulate
- Place and Route
 - Verify Post Layout Implementation
 - Verify Timing
 - Open SmartTime
 - Verify Power
 - Open SSN Analyzer
- Configure Hardware
 - Programming Connectivity and Interface
 - Configure Programmer
 - Select Programmer
- Program Design
 - Generate FPGA Array Data
 - Configure Design Initialization Data and Memories
 - Generate Design Initialization Data
 - Configure I/O States During JTAG Programming
 - Configure Programming Options
 - Configure Security
 - Generate Bitstream
 - Configure Actions and Procedures
 - Run PROGRAM Action
 - Program SPI Flash Image
 - Generate SPI Flash Image
 - Run PROGRAM_SPI_IMAGE Action
- Debian Design

Design Flow Design Hierarchy Stimulus Hierarchy Catalog Files

Message

Messages Errors Warnings Info Manage suppressed messages

Message

- Forward annotating clock ident_coreinst.comm_block_INST.dr2_tck on drive pins would add that clock to 1363 clock pins
- Forward annotating clock ident_coreinst.comm_block_INST.dr2_tck on input pins
- Found clock ident_coreinst.comm_block_INST.dr2_tck with period 1000.00ns
- Found inferred clock PF_XCVR_ERM_C1_XCVR_PF_XCVR(ILANED0_tx_rclkint_input_net_inferred_clock with period 10.00ns.

Place and Route [TOP]

Please refer to the log file for details about 7 Info(s)

Generate Bitstream [TOP]

Please refer to the log file for details

Links

- Welcome to Libero SoC
- Libero SoC Quickstart
- Libero SoC Interface Description
- Libero SoC Release Notes on the Web
- Libero Tutorials
- Product Tutorials
- Training Webcasts
- Microsemi SoC Website

Libero SoC Quickstart

What would you like to do?

- View the Libero SoC Design Flow (link opens Design Flow summary topic in Help) - Use the links below to create your design.
- Create a SmartDesign Component - Enables you to take configured cores, IP cores, macros from the Catalog, and user-created HDL source files and instantiate them into your design.
- Create HDL - Creates a new HDL file and opens it in the HDL editor; useful if you prefer to work in HDL in conjunction with SmartDesign.
- Import existing files into this project.
- View/Configure Firmware Cores - Opens the Firmware view
- Add a Core from the Catalog - Open the Catalog tab to view the list of available Cores. To open the Catalog, click View > Catalog.

Microsemi PolarFire® FPGA

EVEREST-DEV-BOARD PROTO

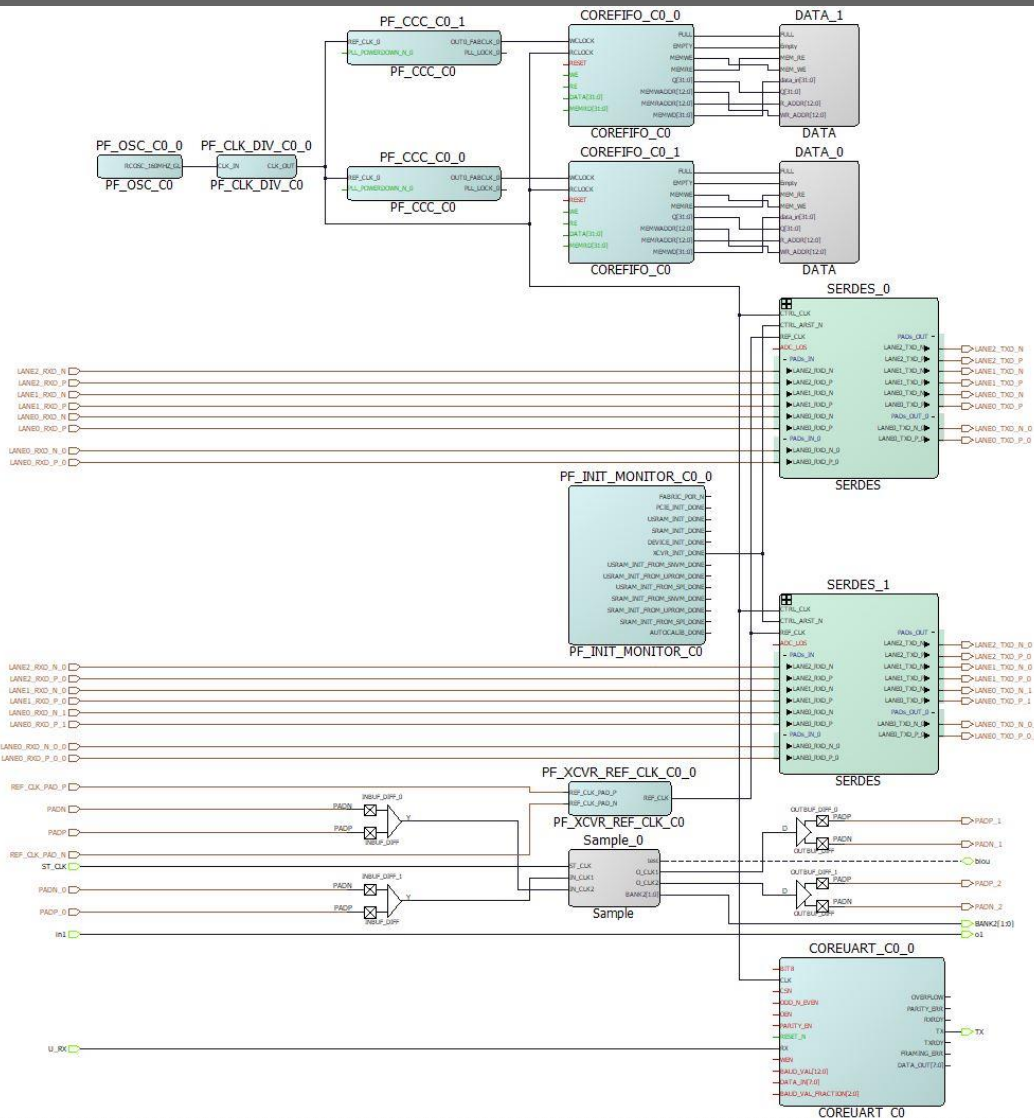
HASc IMG

Microsemi Pulse Electronics Micron ANALOG DEVICES LITEON

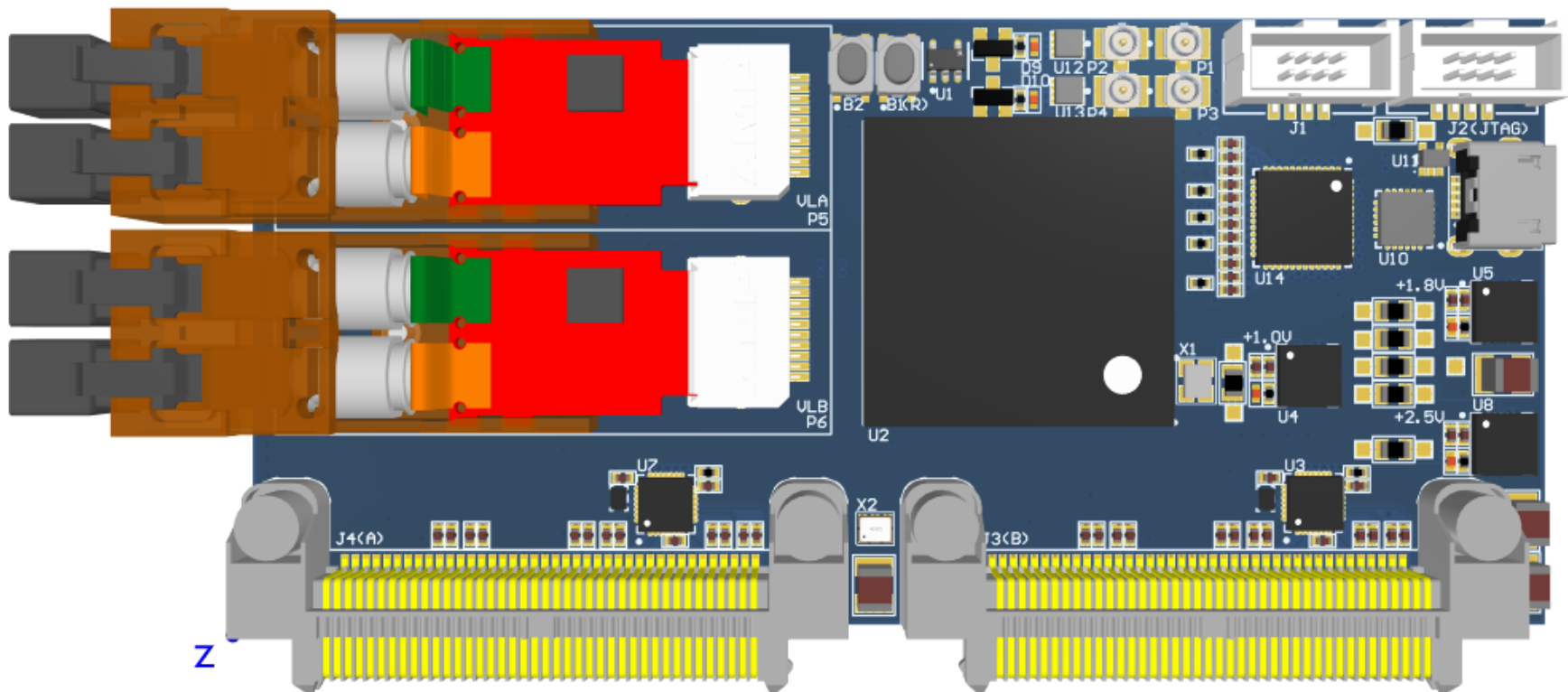
Fam: PolarFire Part: MPF300T-IFCG115ZE VHD

- Evaluation card with Libero development system

A project containing 6 channels 2Gb/s and 2 channels 6.25 Gb/s

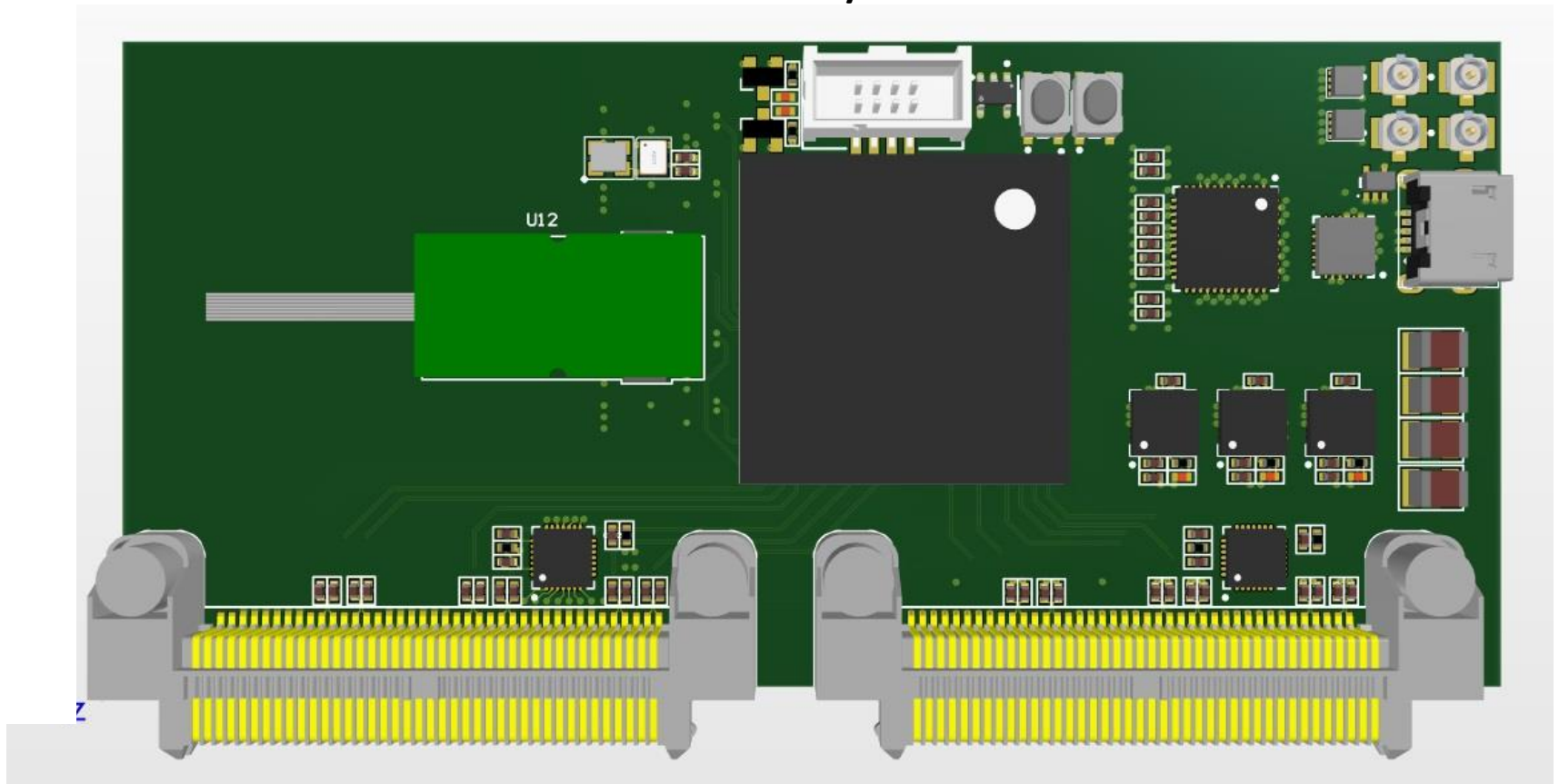


Dual channel VTRx
Test version, 2 x 4,8 Gb/s



VTRx are obsolete

**Future plans:
Dual channel VTRx+
2 x 10 Gb/s**



Old artwork of the future Crate Controller
VTRx+ will be produced 2021

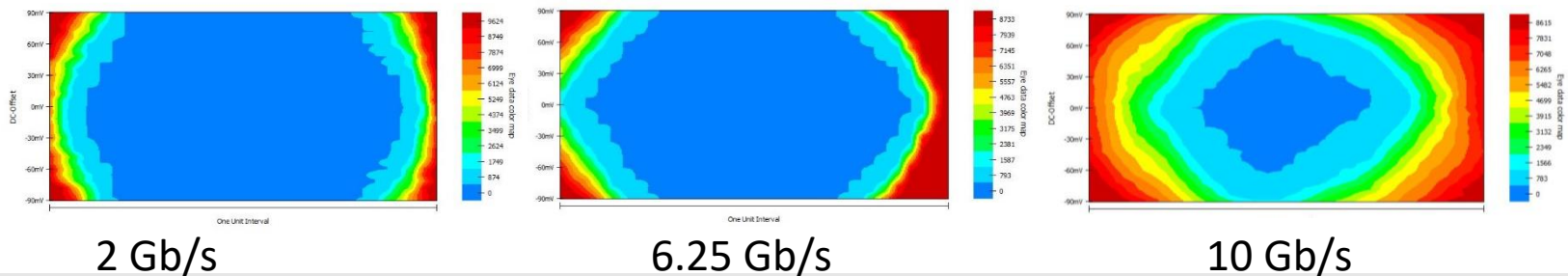
Status

Hardware:

- Hardware design completed
- Recently sent for production

Firmware:

- Canvas project in Libero is ready (mux **3 x 2 Gbit/s** → **6.25 Gbit/s**)
- Successful elimination of external PLL, which consumes ca 700 mW
- Successful time deterministic tests of bilateral communication to ADC
- New master student assigned for development of ADC control firmware





Thank You !