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# DAQ Activities in Cracow

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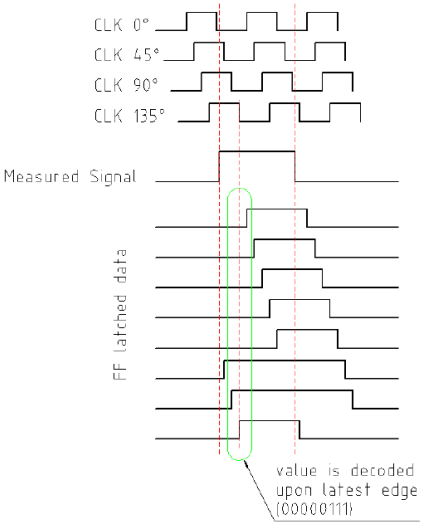
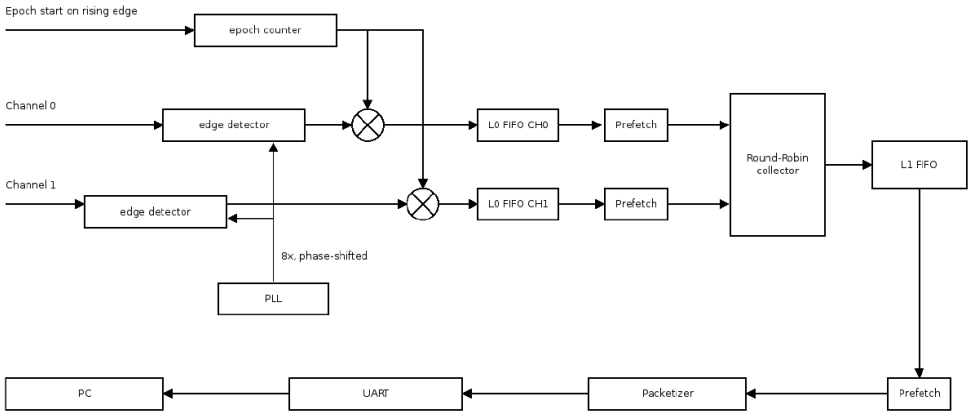
# Work packages

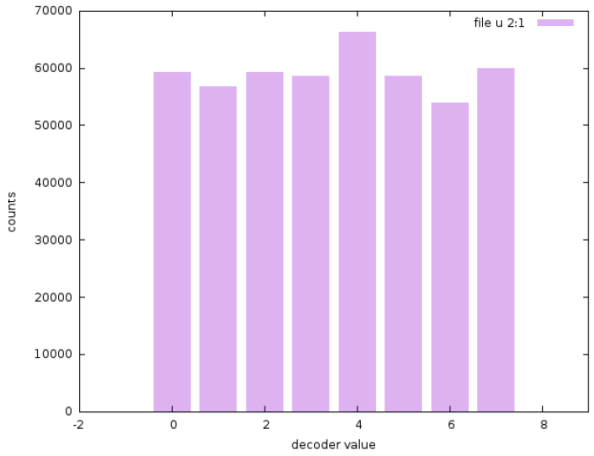
1. TRB5 readout board
   - Firmware:
     - New TDC implementation
     - PASTTREC controller
     - Communication infrastructure
2. Intermediate board for FT
   - Firmware:
     - Online tracking pipeline
3. New DAQ Concept
   - Evaluation of HPC systems
   - Evaluation of programming models
4. Support and maintenance

# 1. TRB5 Readout Board (M. Michalek)

- Low-resolution TDC on Lattice ECP5
  - Input signal oversampling with phase-shifted clocks
- Base design developed and under evaluation
  - Running on Lattice ECP5 Versa evaluation board
  - 250MHz master clock – 500 ps TDC bin
  - Many compiler related problems overpassed

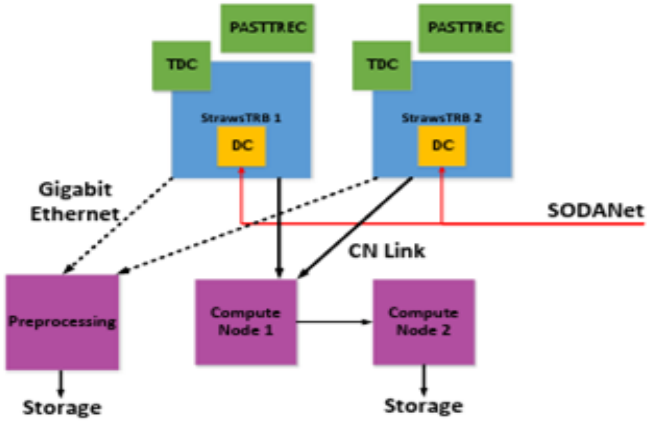


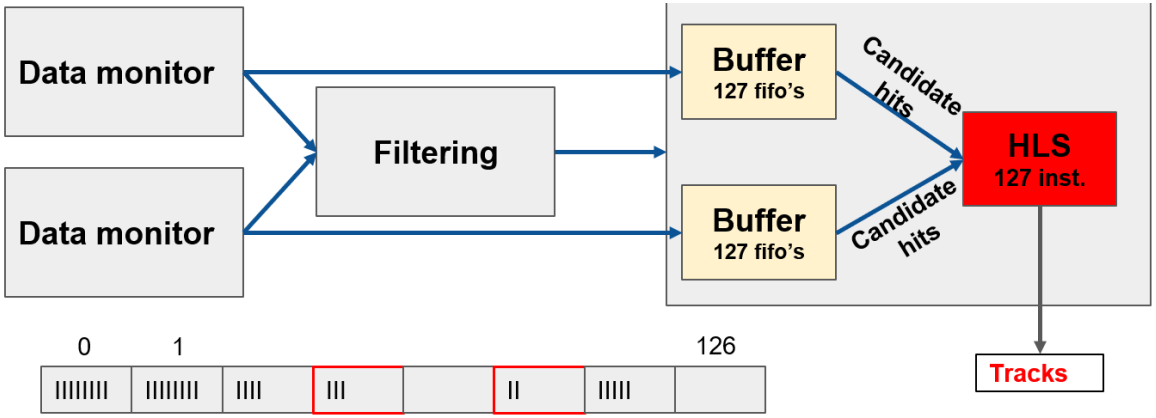



# 2. Intermediate FT processing (A. Malige)

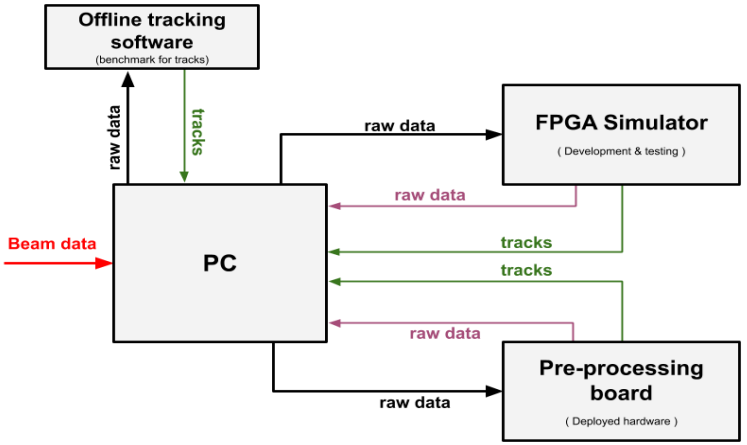
- Development of an FPGA-based event selection
- Data from beamtime in Juelich 2019
- Superburst data sporting into timebins
- Parallel timebin tracking
  - Data filtration and sorting in HDL
  - Tracking in High Level Synthesis



# 2. Intermediate FT processing (A. Malige)

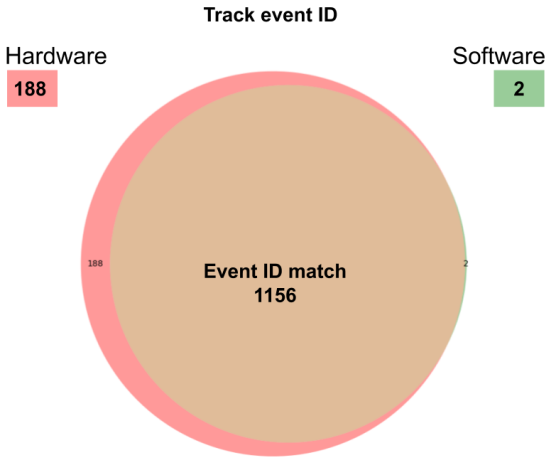
- Development of a complete evaluation environment
  - Algorithm verification at multiple stages
- 2019 beamtime data analyzed
  - Preliminary insight into implementation
  - 90% match with software analysis
  - Limited FPGA resources
- Focus on event selection and data reduction
- Evaluate tracking on Neural Nets (W. Esmail)




**Utilization Estimates**

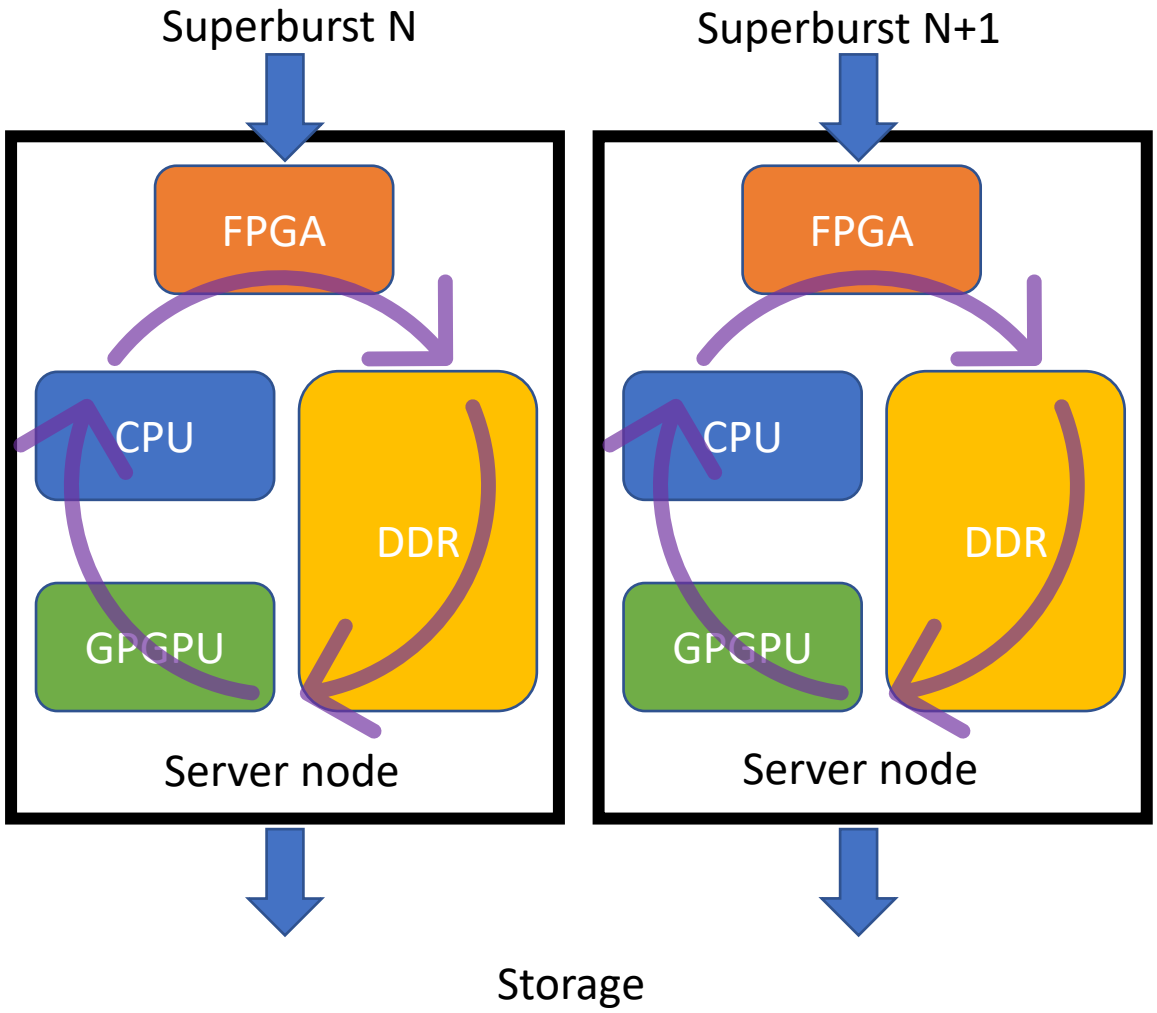
**Summary**

| Name | BRAM_18K | DSP48E | FF | LUT | URAM |
|---|---|---|---|---|---|
| DSP | - | - | - | - | - |
| Expression | - | - | 0 | 1501 | - |
| FIFO | - | - | - | - | - |
| Instance | 20 | 32 | 13069 | 14392 | 0 |
| Memory | 6 | - | 0 | 0 | 0 |
| Multiplexer | - | - | - | 597 | - |
| Register | - | - | 2383 | - | - |
| Total | 26 | 32 | 15452 | 16490 | 0 |
| Available | 1824 | 2520 | 548160 | 274080 | 0 |
| Utilization (%) | 1 | 1 | 2 | 6 | 0 |



# 3. New DAQ concept

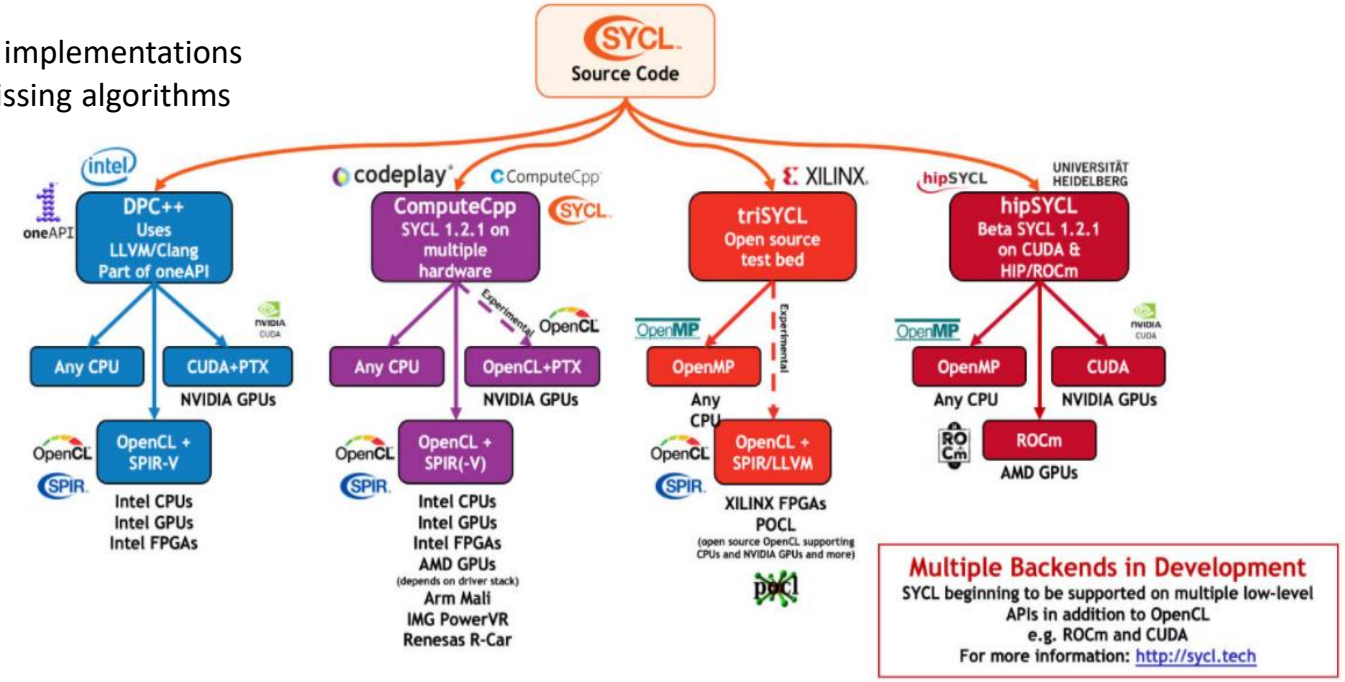
- Take advantage of each device
  - FPGA: direct and low latency network interface, data preprocessing, accelerated kernels, custom data-types
  - GPGPU: highly paralel processing, FLOPS/W ratio
  - CPU: processing pipeline managment, data shuffeling, kernels invocation



# 3. New DAQ concept

- Development of software environment with the use of hardware accelerated kernels
- Use of high-level programming models
  - Single source – any platform SYCL
  - Based on C++11 standard
  - Host – Kernels architecture

- Analysis software
  - Migrate existing implementations
  - Develop new/missing algorithms




Khronos group

# 3. New DAQ concept

- Foundation of a research group
  - Hardware Acceleration Lab – Jagiellonian University
    - Gathering of experts from various HPC related fields
    - Exchange of know-how
    - Access to supercomputing center at Cyfronet AGH Kraków
    - Significant investment into computing infrastructure at UJ
    - Coordinated application for project funding
  - SYCL subgroup
    - Migration of FT tracking algorithm (TDR) to SYCL
    - Optimization and evaluation on CPU/GPGPU/FPGA
    - Next step: investigation on Neural Net-based tracking (W. Esmail)
  - Looking forward estalishing the Big Bicture of online algorithmic pipeline