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Online data processing system on heterogenous architectures

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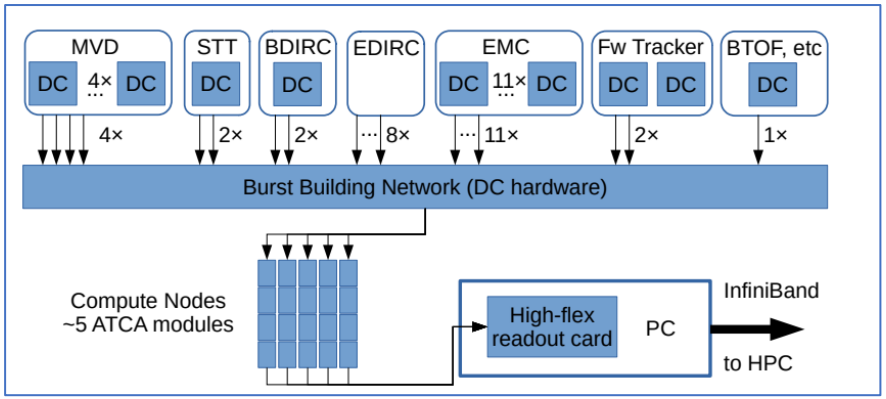
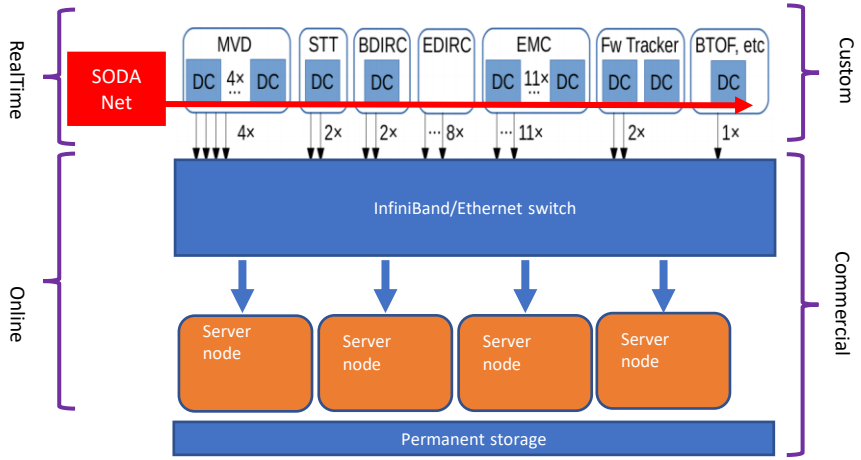
25 October 2020, Kraków

PANDA DAQ Concept

- Proposed solution (DAQ-TDR)
  - Escape to commercial hardware at the earliest stage
    - Long-term manufacturer support
    - Support from experts/community
    - Easily upgradable with new HW/SW releases
  - Select technologies with high-level development environments
    - Avoid reinventing the wheel (protocols, data handling, etc.)
    - Focus on algorithmics
    - Merge offline and online analysis procedures
    - Accelerate development and debugging cycles
    - Involve non-hardware experts into the developers group
  - Current trend in major experiments

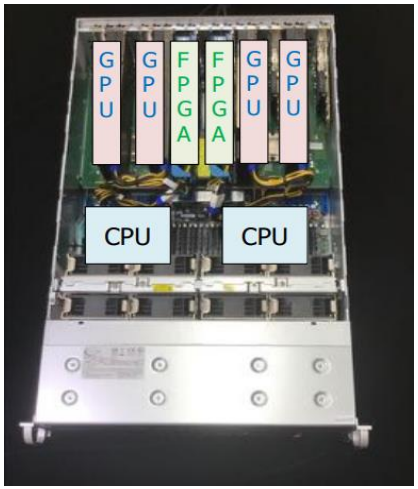




M. Kavatsyuk

Server configurations

- Heterogenous HPC systems
  - Mix of CPU, GPGPU, FPGA, …
  - Each architecture has its pros/cons
    - CPU
      + General purpose, easy to use
      - Low FLOP/W ratio, low level of parallelism
    - GPGPU
      + High FLOP/W ratio, high level parallelism (SIMT)
      - Low performance at non-regular computations, data organization
    - FPGA
      + High FLOP/W, high level of parallelism, real-time, direct data access
      - Difficult to program and use efficiently



T. Boku, Cygnus, Albireo node

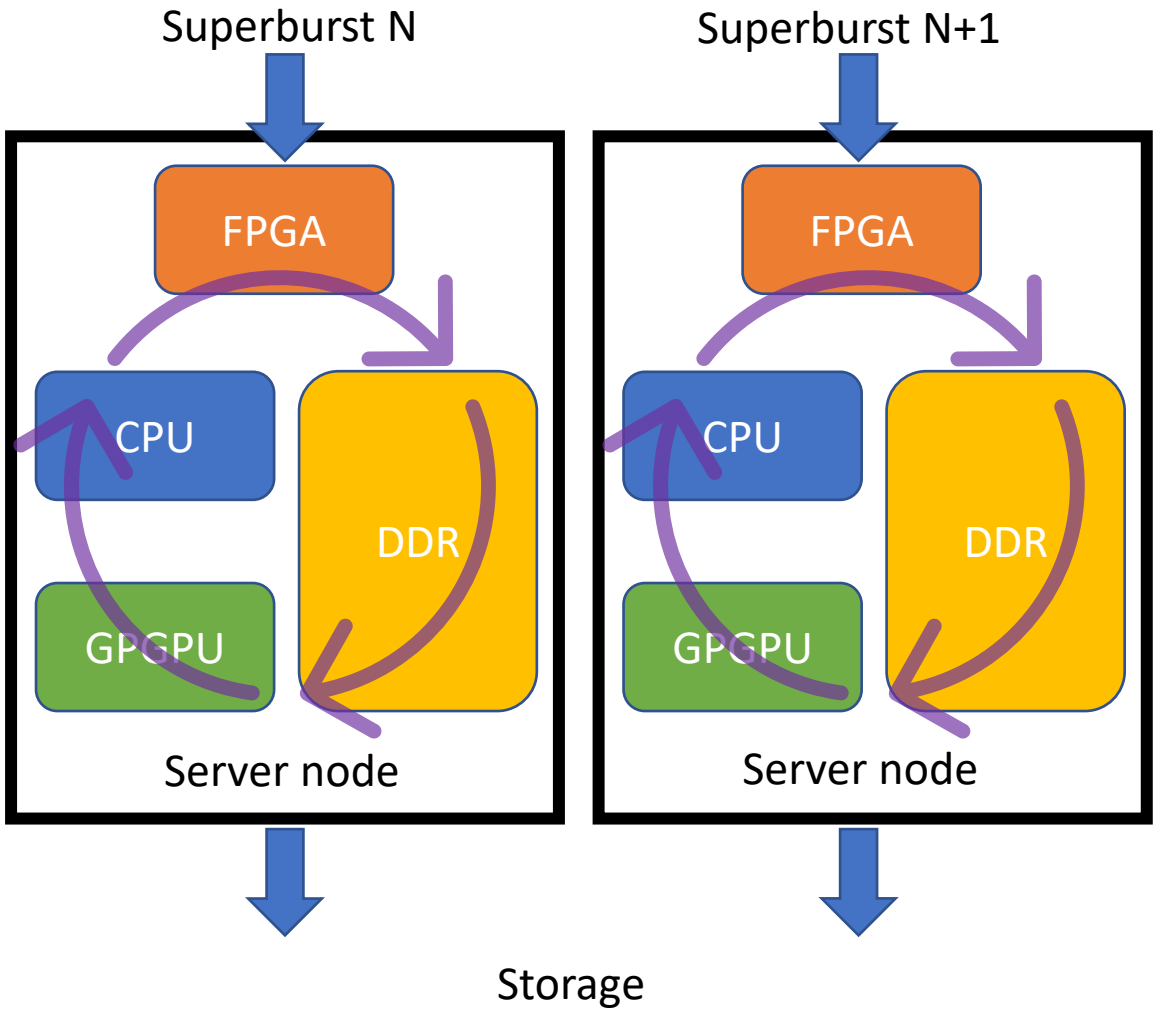
- Major HPC systems have diversified architecture
  - Amazon AWS
  - Microsoft Azure
  - Huawei
  - Cygnus at Tsukuba Japan

Xilinx.com

- Variety of ready-to-use hardware available

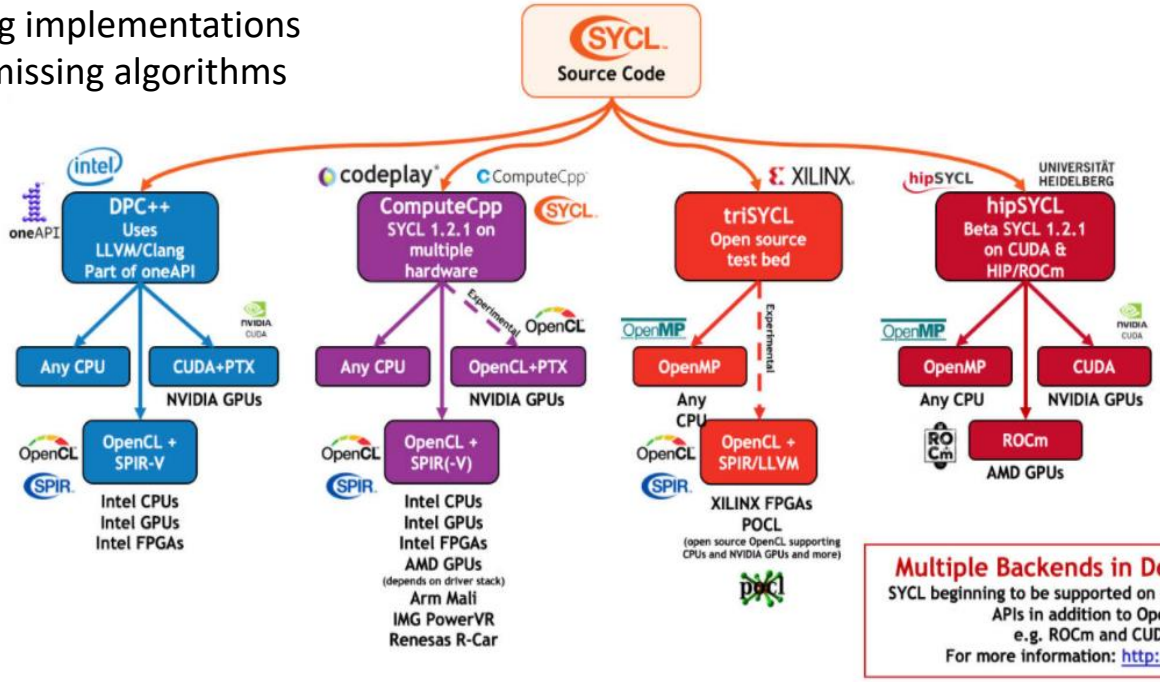
Server configurations

- Take advantage of each device
  - FPGA: direct and low latency network interface, data preprocessing, accelerated kernels, custom data-types
  - GPGPU: highly paralel processing, FLOPS/W ratio
  - CPU: processing pipeline managment, data shuffeling, kernels invocation



Programming model

- Development of software environment with the use of hardware accelerated kernels
- Use of high-level programming models
  - Single source – any platform: SYCL
  - Based on C++11 standard
  - Host – Kernels architecture
- Analysis software
  - Migrate existing implementations
  - Develop new/missing algorithms



Khronos group

Online software analysis

- Foundation of a research group
  - Hardware Acceleration Lab – Jagiellonian University
    - Gathering of experts from various HPC related fields
    - Exchange of know-how
    - Access to supercomputing center at Cyfronet AGH Kraków
    - Significant investment into computing infrastructure at UJ
    - Coordinated application for project funding
  - SYCL subgroup (B. Soból, W. Gawłowski UJ)
    - Migration of FT tracking algorithm (FT-TDR) to SYCL
    - Optimization and evaluation on CPU/GPGPU/FPGA
    - Next step: investigation on Neural Net-based tracking (W. Esmail)

Hardware acceleration group

- We are looking for:
  - Algorithms and implementations to be accelerated
  - People willing to get involved into development on accelerated platforms
  - Experts from subsystems for interfacing with specific readout data
- All efforts in this field will be beneficial for all computing related activities in PANDA