PANDA MVD Optimisation

Lars Schmitt, GSI

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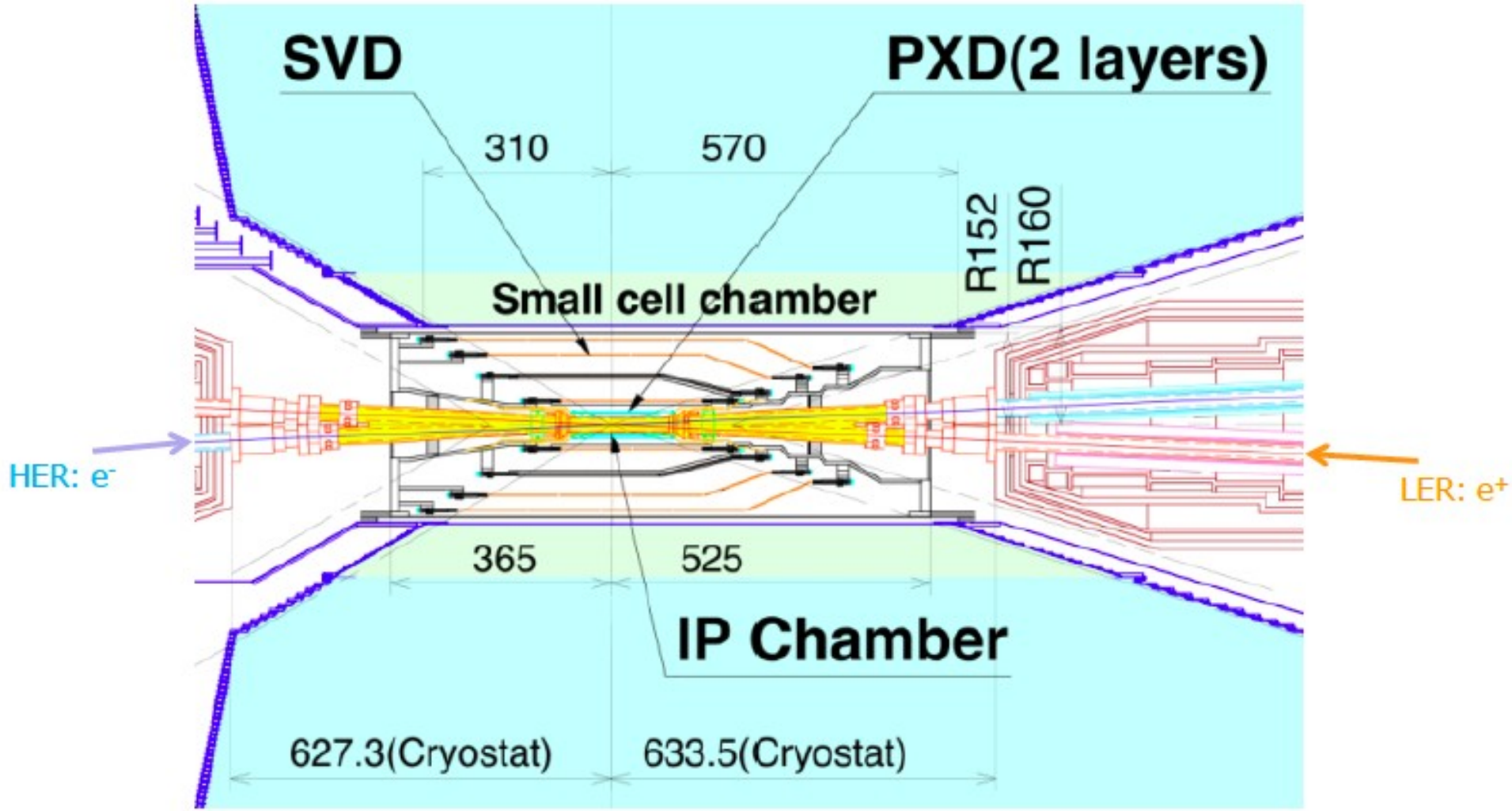
- A Look at Belle-II
- MVD Material Budget
- Possible Optimisations
- Conclusions

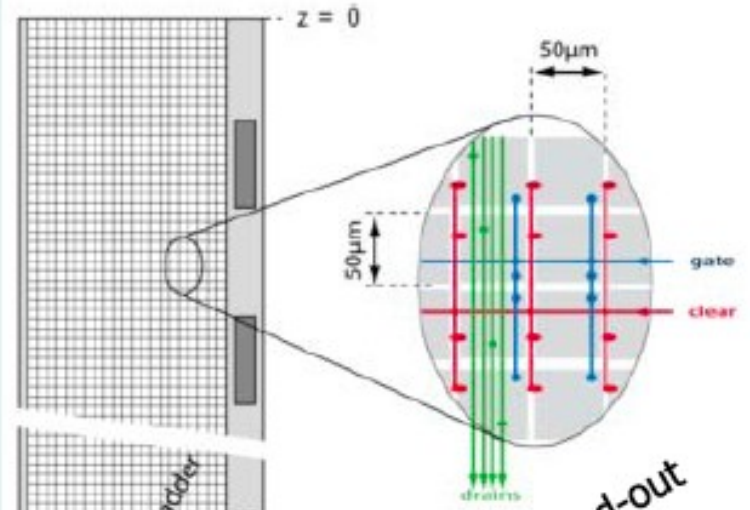
Belle to Belle-II

Belle Silicon Vertex Detector (SVD): 4 layers DSSD → Belle II: 4 DSSD (SVD)+ **2 pixel layers (PXD)**

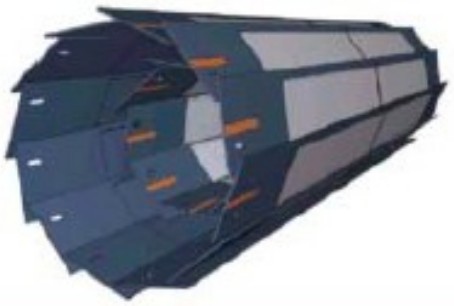


-: also Central Driftchamber (CDC), Calorimeters, Particle ID, Muon ....

The DEPFET Belle-II ladder

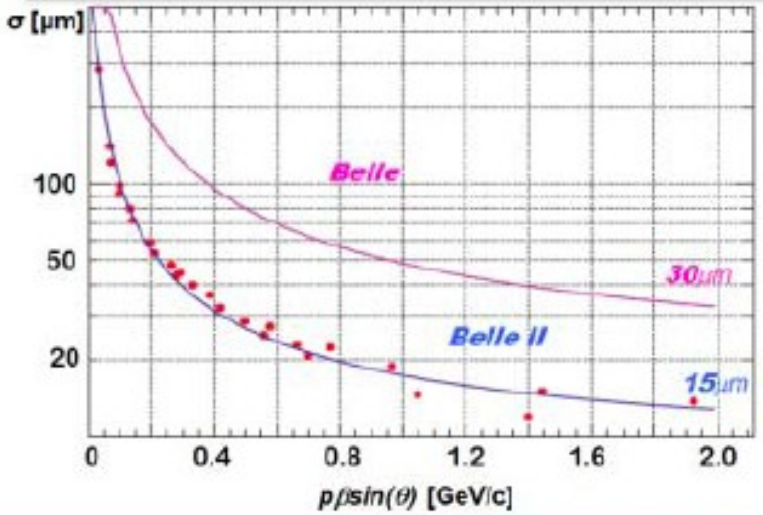


	Inner layer	Outer layer
# ladders	8	12
Sens. length	90 mm	123 mm
Radius	1.4 cm	2.2 cm
Pixel size	50x50 µm²	50x75 µm²
# pixels	1600(z)x250(R-ϕ)	1600(z)x250(R-ϕ)
Thickness	75 µm	75 µm
Frame/row rate	50 kHz/10 MHz	50 kHz/10 MHZ

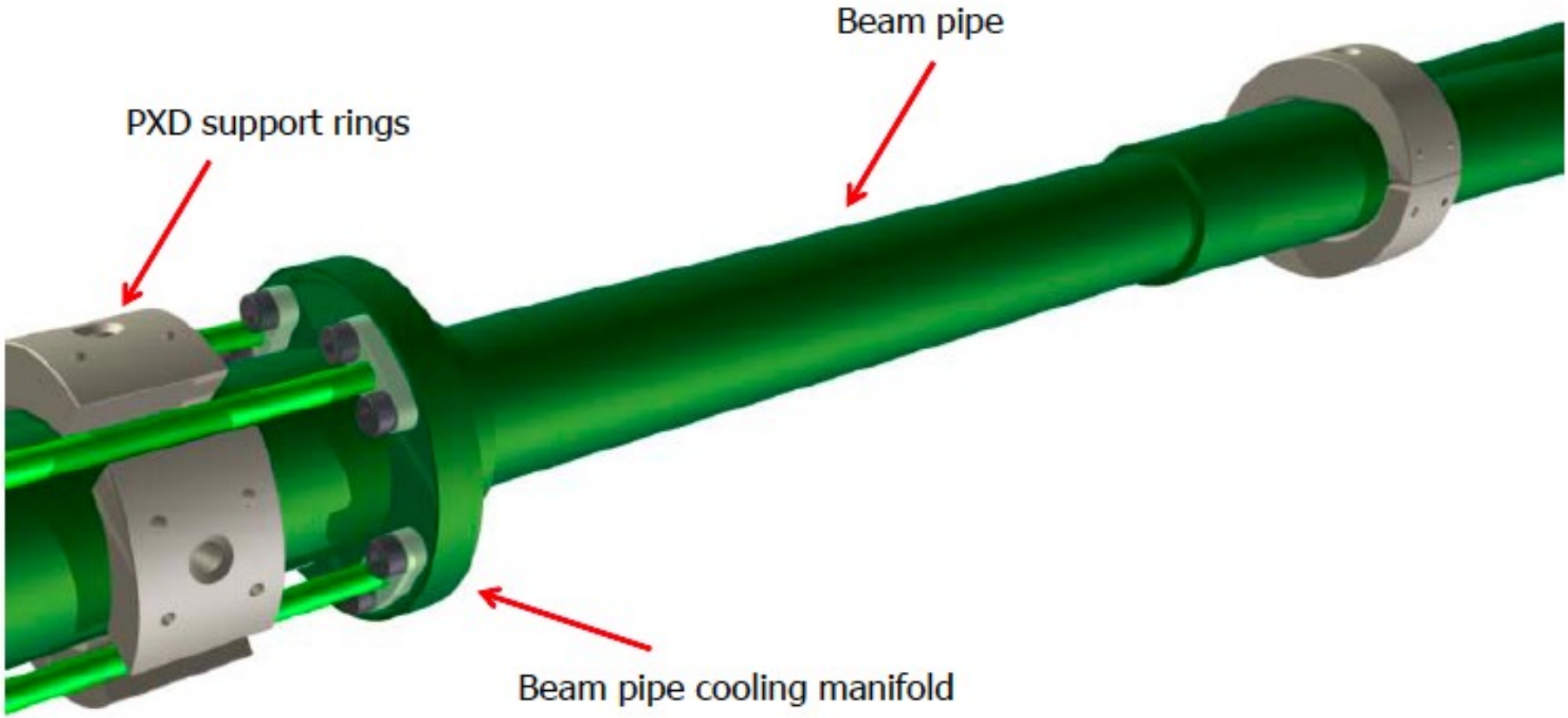


Angular coverage 17°<θ < 155°

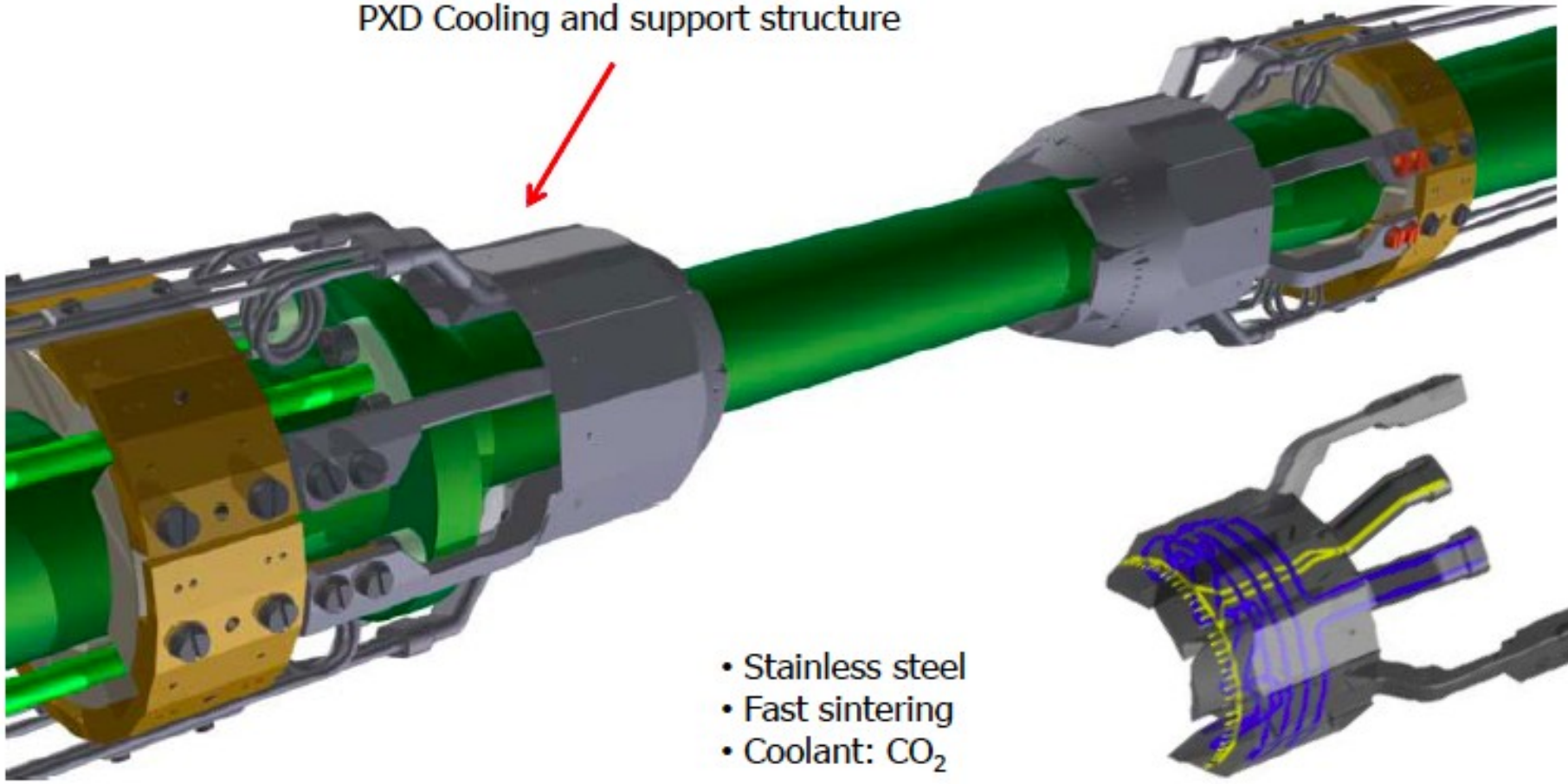
z vertex resolution significantly improved



Mechanical design



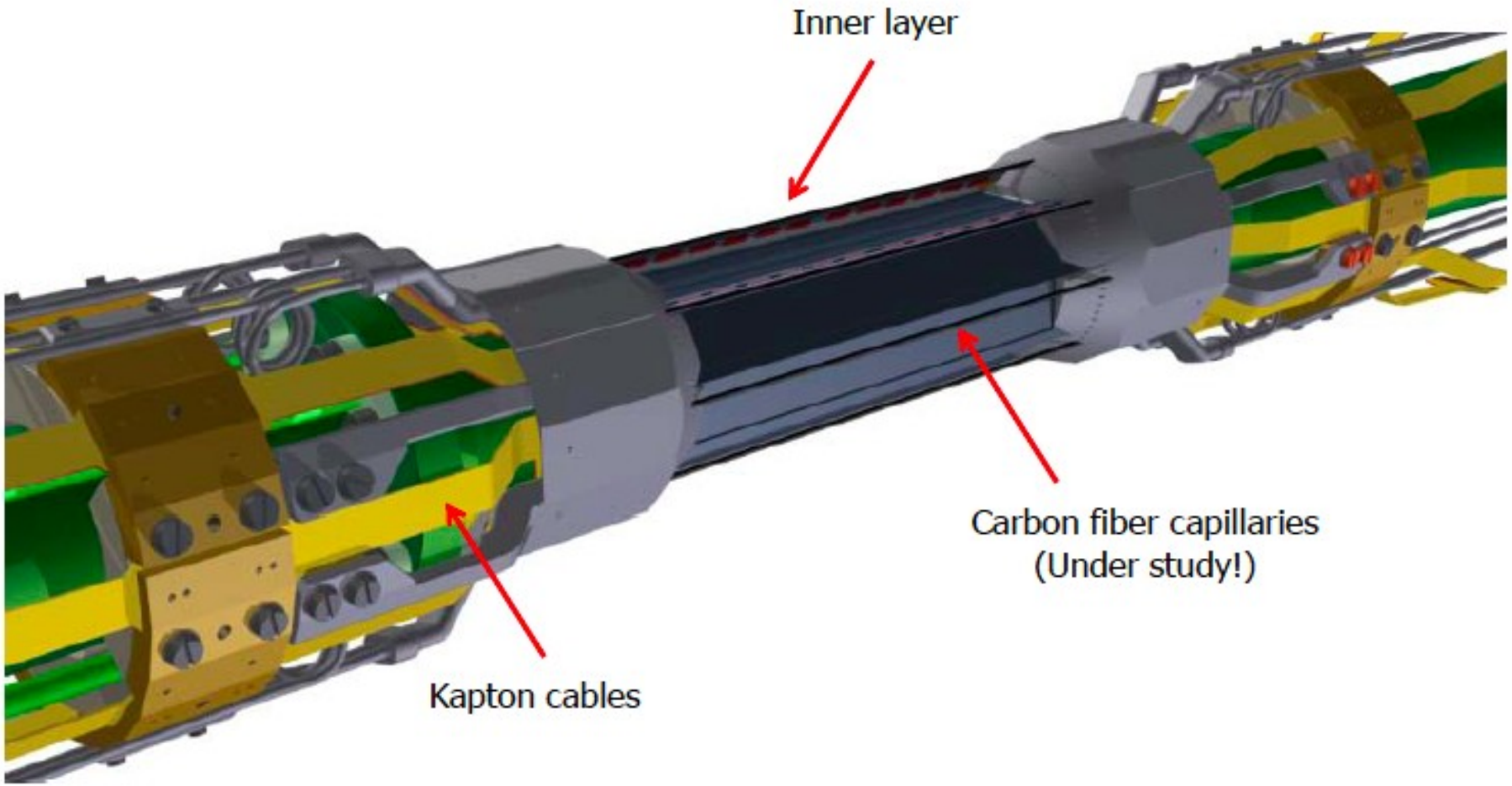
Mechanical design



- Stainless steel
- Fast sintering
- Coolant: CO_2

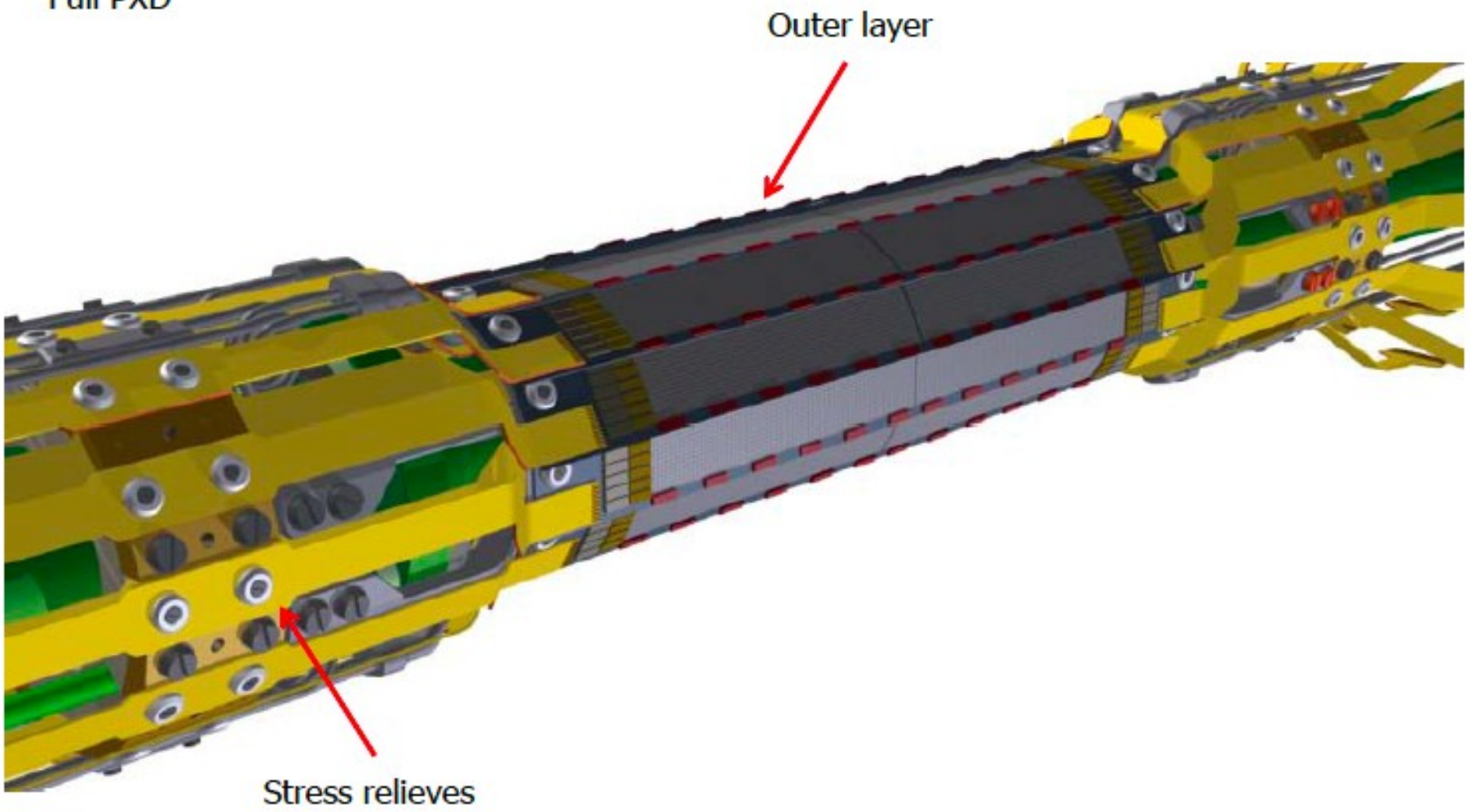
Blue: CO_2 capillaries
Yellow: Air channels

Mechanical design



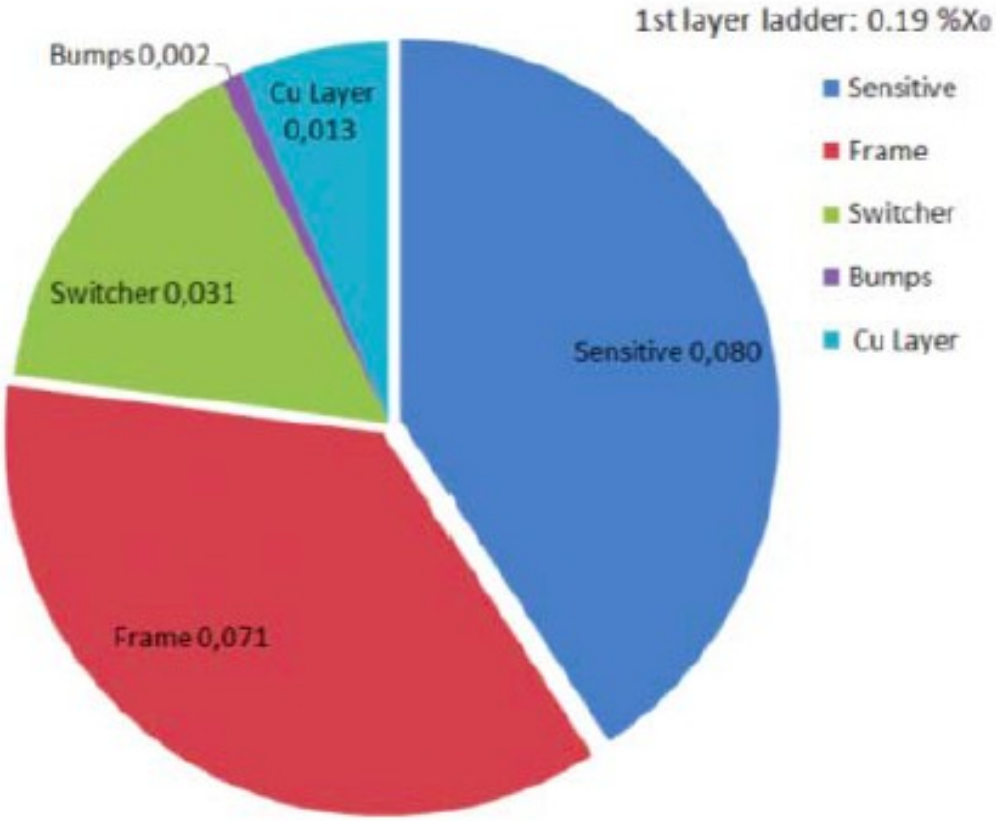
Mechanical design

Full PXD



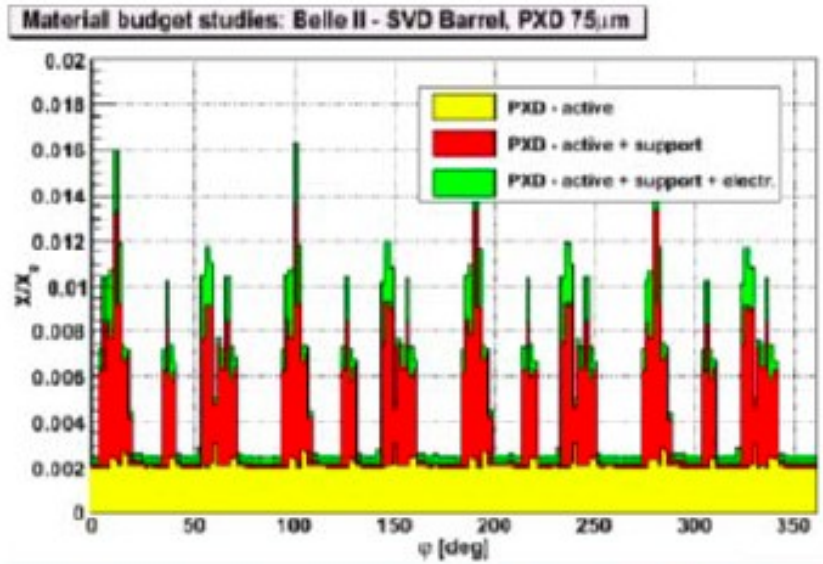
Total Material Budget within the Sensitive Volume

- sensitive area of the first layer ladder: 1.25x9.0 cm² (1.5x9.0 incl. frame), 75 µm thin
- support frame: 0.1+0.2 cm, 420 µm
- Switcher-Sensor Interconnect: Gold stud bumps, one bump/connection, Φ=48 µm
- Cu Layer t=3 µm, 50% coverage in acceptance
- Switcher dimensions: 0.15x0.36 cm²
- Number of Switchers: 12 (32x2 channels per chip – gate and clear)
- Material reduction by frame perforation: 1/3

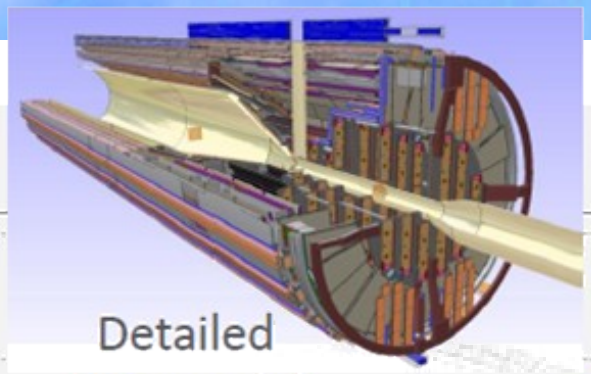


→ 0.19 %X_0 in total

Silicon contribution (0.15%) experimentally confirmed



PANDA MVD Material Budget



Comparison of Material Budget

Belle-II Vertex Detector

- 2 pixel and 4 strip layers
- Pixel layer: 0.19 % X/X_0
- Strip layer: 0.57 % X/X_0
- Total: 2.66 X/X_0
- In a PANDA-like configuration: 1.52 % X/X_0

PANDA MVD

- Barrel: 2 pixel + 2 strip layers
- Pixel layer: 1.19 % X/X_0
- Strip layer: 0.96 % X/X_0
- Total: 4.3 X/X_0

  But from the previous picture more like >6 X/X_0

ALICE Vertex Detector

Detector	Pixel		Drift		Strip	
	Inner	Outer	Inner	Outer	Inner	Outer
Layer	1.14	1.14	1.13	1.26	0.83	0.86
Thermal shield/Support		0.52	0.25		0.53	
Total	7.18 (7.26 including Air)					

Possible Optimisation

Two roads for a lower material budget

- Take a completely different approach, e.g. DEPFET
- Modernize presently chosen approach

Items for optimisation ***(these are just examples)***

- Keeping the ToPiX design try to go for 3D integration:
  - Further thinning of sensor
  - Wafer-to-wafer bonding with ToPiX
  - Possibly introduce a further transfer layer
- Different cooling strategies:
  - CO_2 cooling (liquid or 2-phase)
  - Silicon oxide support providing heat transfer
- Optimise cable routing
  - Avoid double layering
  - Consider forward routing for disks

Conclusions

- Comparison to competitors which are even ready before us:
  - Resolution and material budget are *the* critical figures of merit
  - Referees of our TDR may judge our design baseline as too conservative
- Which impact would a factor 2 less material have?
  - Electromagnetic calorimetry
  - Vertex and track resolution
- We should re-evaluate some of our assumptions
  - Cable routing
  - Beam pipe design
  - Cooling and support

Final Questions

Questions we have to ask ourselves before further steps:

- How much time would we need for further optimisations?
- Would we need additional collaborators?
- Whom should we approach, from whom can we learn?
- Can we afford not to do any further optimisation?