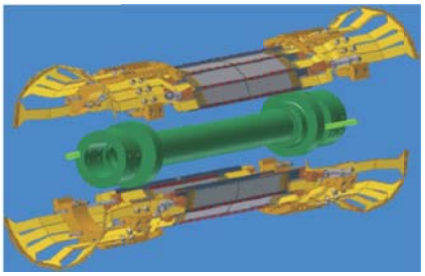
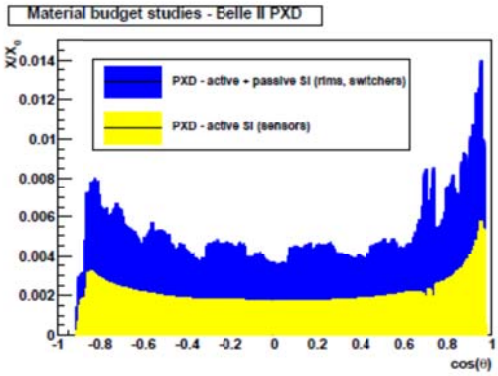
- Interaction region design much more evolved than in PANDA => detectors much easier to construct!
- In particular: Details of what is needed as injection etc.!
- Beam position monitors!
- Beam-induced background estimations provided to the detector groups!
- Much of it admittedly based on extrapolations from KEKB to SuperKEKB
- COSY extrapolations to HESR?

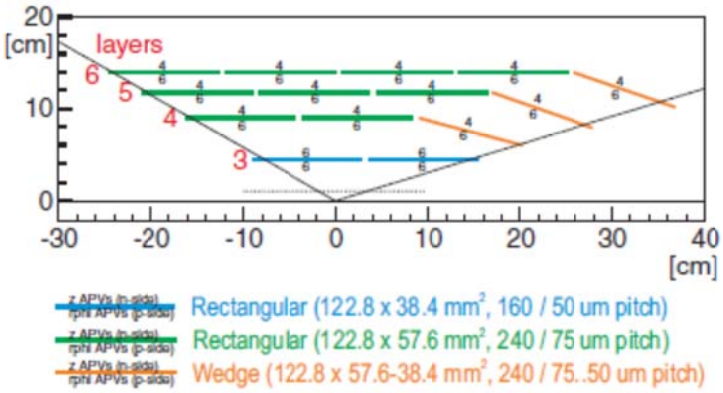
- Belle II PXD using DEPFETs
- Only two layers, 17.4 mm long, large dead area in front and back needed for readout electronics
- Sensitive layers 14 mm radius / 90 mm length, 8 sensors of 15 mm width along circumference
-



- All pixels read out, zero suppression externally in ASICs at frontend level.
- 20µs readout time for full frame, external readout trigger on frames, individual pixel dead time 100 ns per frame
- Surrounded by strip detector
- "world's most complex technology on high ohmic wafers"
- Thinning not yet achieved
- Rad hardness not yet achieved
- Pixel size not much different from ToPiX (50x50 and 75x75)
- Row processing time 100 ns
- Drift times below 60 ns
- ASIC developments? (Switcher, Drain Current Digitizer, Data Handling Processor)
- Switcher timing by EXTERNAL Strobe!
- ADC sampling time 10 MHz
- Detector will integrate over 20 µs!
- .18% of X_0
- No simulations of radiation level, at least 10 MRad (1-2 per year)
- Particle flux 10 MHz/cm^2 … 10^{13} n_{eq}/cm^2 NIEL
- Estimates based on a trigger rate of 30 kHz
- Average occupancy about 1%, 80000 fired pixels per frame
- Hardware platform (PANDA) compute nodes



- Outside by SVD II, covering 17° to 150°, 38 mm to 140 mm radius
- Using the front end ASICs we employ in current tests



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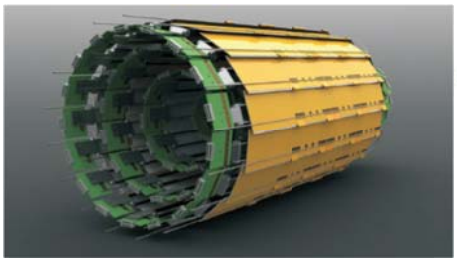
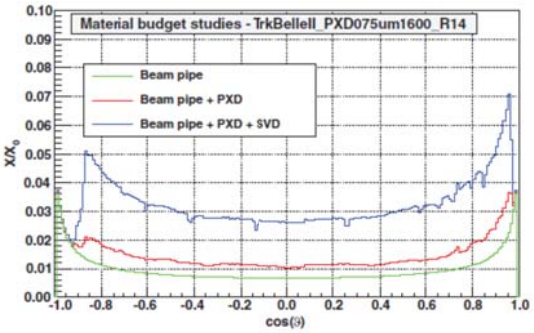
- 300 µm thick sensors





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- 700 W thermal power