The sensor study for the pixel detector: report on the thinning process

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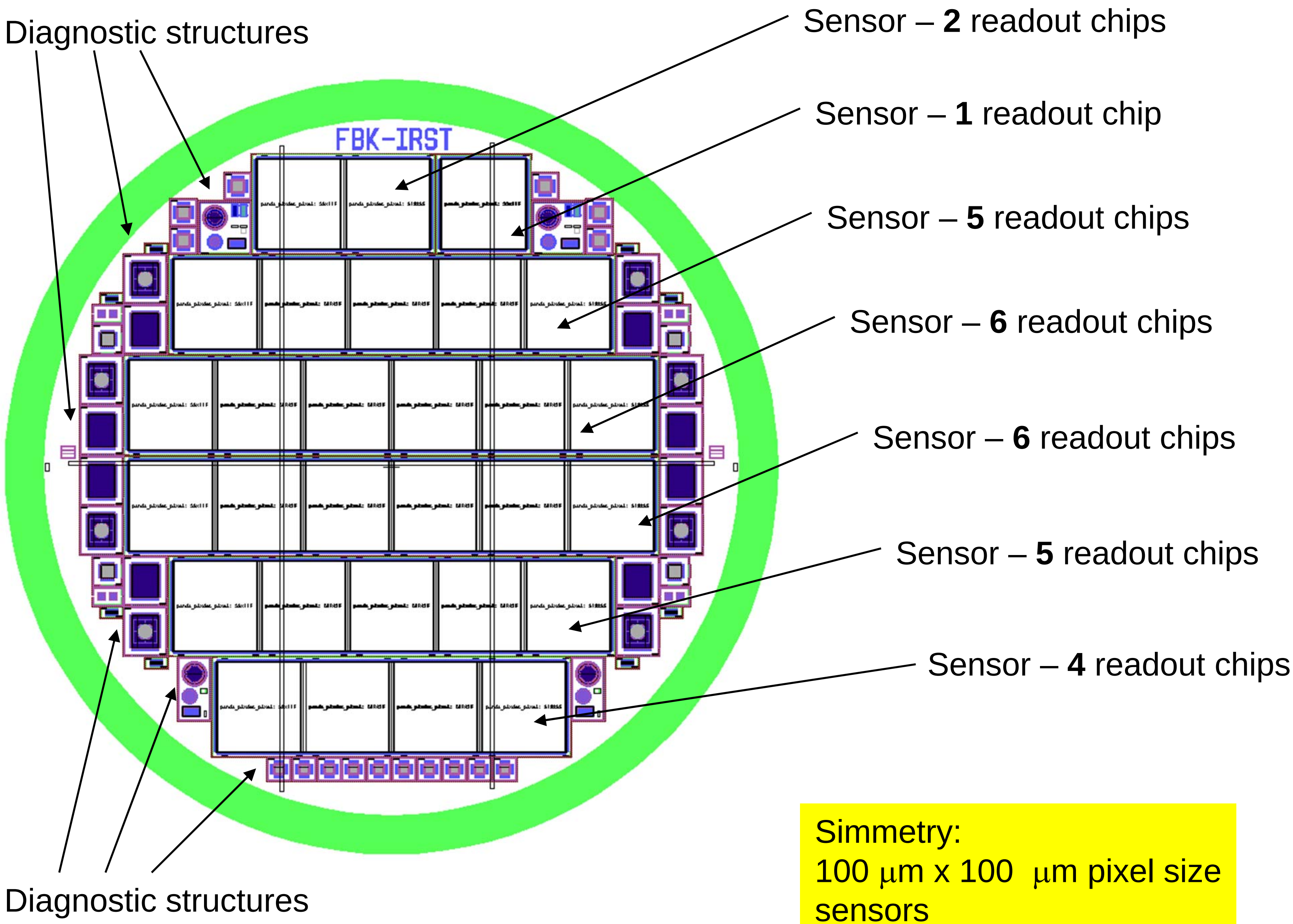
in collaboration with FBK - Trento

Thinning process on the PANDA pixel wafers

PANDA pixel wafer: first sensor prototype



Simmetry:
100 μm x 100 μm pixel size sensors

Some calculations

	Barrel 1	Barrel 2	Disk 1	Disk 2	Disk 3	Disk 4	Disk 5	Disk 6	Total
Module 2	6		6	6					18
Module 4			2	2	6	6	6	6	28
Module 5	8				12	12	12	12	56
Module 6		50			4	4	4	4	66
Total number	14	50	8	8	22	22	22	22	168

	1 wafer	33 wafers
Single chip	1	33
Module 2	1	33
Module 4	1	33
Module 5	2	66
Module 6	2	66

Wafer features

Wafer parameter	Epi-75, low resistivity	Epi-50	Epi-75	Epi-100
substrate				
Diameter [mm]	100 ± 0.05	100 ± 0.05	100 ± 0.05	100 ± 0.05
Orientation	<100>	<100>	<100>	<100>
Conductivity type/dopant	n^+/Sb	n^+/Sb	n^+/Sb	n^+/Sb
Thickness [µm]	525 ± 25	525 ± 25	525 ± 25	525 ± 25
Resistivity [ohm·cm]	0.008 ÷ 0.02	0.008 ÷ 0.02	0.008 ÷ 0.02	0.008 ÷ 0.02
Epitaxial layer				
Conductivity type/dopant	n/P	n/P	n/P	n/P
Epitaxial layer thickness [µm]	73.67 ÷ 75.90	49.35 ÷ 50.39	73.83 ÷ 75.42	99.34 ÷ 100.38
Radial thickness variation	< ± 8%	< ± 5%	< ± 8%	< ± 8%
Resisitvity [ohm·cm]	435 ÷ 460	3100	3200	3610
Radial resistivity variation	< ±10%	< ±10%	< ±10%	< ±10%

Thickness measured by IR reflectance method and resistivity measured by spreading resistance method at ITME

Measured parameters on the patterned wafers

wafer #	Type	Epi thick (µm)	resistivity [ohmcm]	J (nA)/cm2	Ox thickness (nm)	Qox (cm-2)	N epi (cm-3)
1	Subs:n+/SB epi:n/P	75	~ 460	3.75	760	6.2E+10	5.7E+12
2	Subs:n+/SB epi:n/P	75	~ 460	5	779	6.4E+10	3.9E+12
3	Subs:n+/SB epi:n/P	100	3610	7.5	760	6.9E+10	7.8E+11
4	Subs:n+/SB epi:n/P	50	3100	2.25	781	6.5E+10	3.5E+11
5	Subs:n+/SB epi:n/P	75	3200	2.5	760	6.6E+10	7.6E+11
6	Subs:n+/SB epi:n/P	50	3100	2.25	783	7.0E+10	3.6E+11
7	Subs:n+/SB epi:n/P	75	3200	2.75	766	6.3E+10	7.1E+11
8	FZ	FZ		1.5	-		
9	FZ	FZ		1.75	-		
10	Subs:n+/SB epi:n/P	75	3200	2.75	784	6.9E+10	3.3E+11
11	FZ	FZ		2	-		
12	Subs:n+/SB epi:n/P	100	3610	3.5	777	7.1E+10	2.8E+11
13	Subs:n+/SB epi:n/P	50	3100	2.5	760	6.4E+10	7.7E+11
14	Subs:n+/SB epi:n/P	75	3200	2.5	781	1.0E+11	3.2E+11
15	Subs:n+/SB epi:n/P	75	~ 460	3.5	760	6.3E+10	6.3E+12
16	Subs:n+/SB epi:n/P	50	3100	3.25	779	6.7E+10	3.1E+11
17	FZ	FZ		1.25	-		

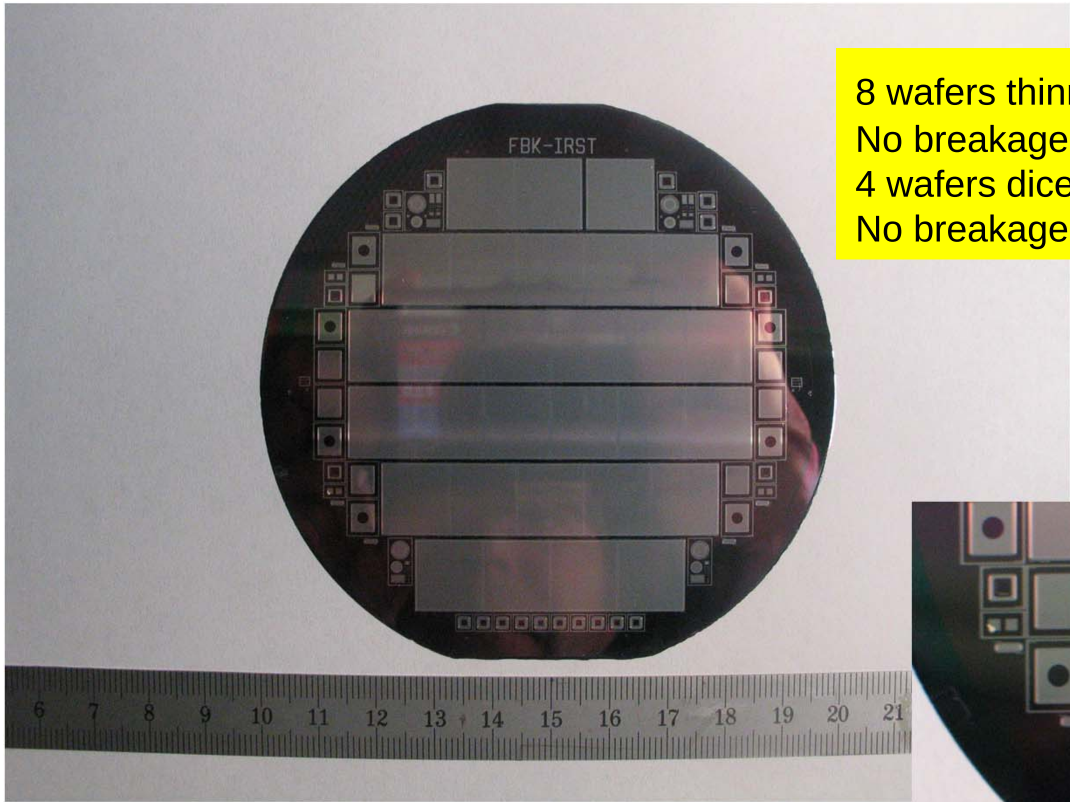
Measurements performed at FBK by Giacomini and Tengattini before thinning process

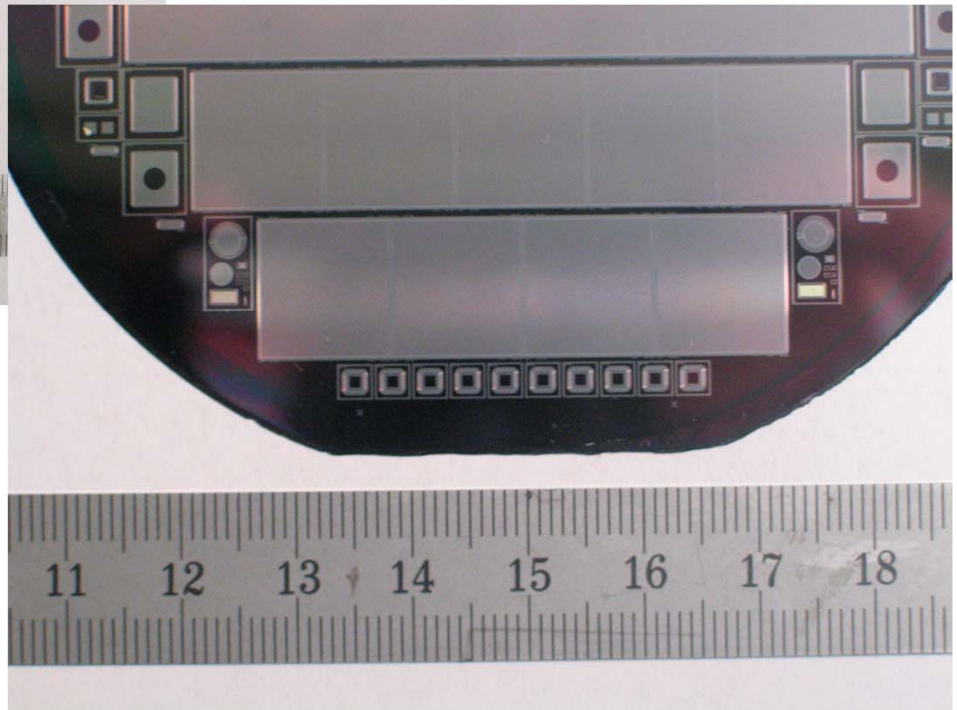
Thinning and dicing processes plan

Wafer number	Type	Target thickness [μm]	Sensor + diagnostic structures dicing
1	Epi-75,LR	100	
3	Epi_100	120	
4	Epi-50	100	
7	Epi-75	100	
10	Epi-75	100	Y
12	Epi-100	120	Y
13	Epi-50	100	Y
15	Epi-75,LR	100	Y

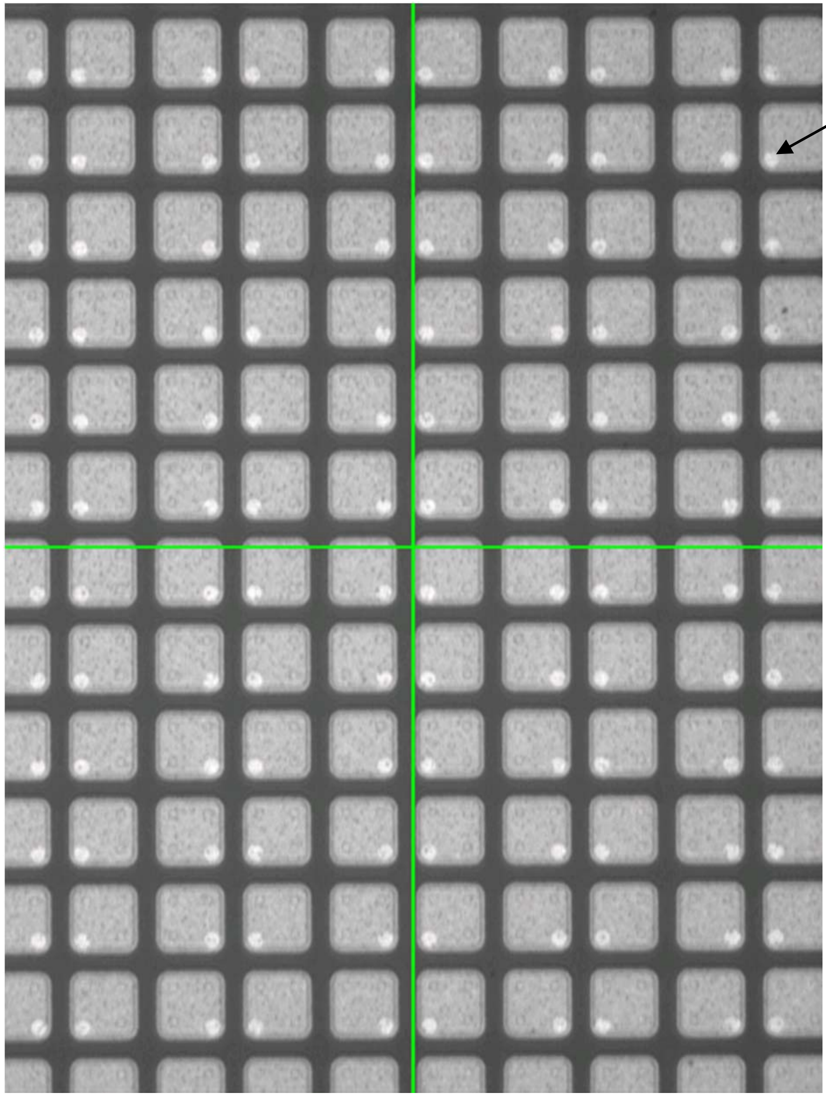
First PANDA pixel wafer (June 2010)

8 wafers thinned to 100-120 μm from WAFER Solution
No breakage problem (de-stressing + polishing processes)
4 wafers diced to obtain sensors and test structures
No breakage problem





Sensor partial view



Pad x bump bonding process

The sensor study for the pixel detector: report on the displacement damage tests

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High resistivity epitaxial silicon devices

Diodes HR, with different Cz substrate

			Group HR (High Resistivity) thin CZ			Group HR (High Resisitivity) thick CZ		
Epi layer name	Epitaxial thickness [μm]	Resistivity [Ω· cm]	Target thickness [μm]	Full depletion voltage [v]	Current density [10-8 A/cm^3]	Target thickness [μm]	Full depletion voltage [v]	Current density [10-8 A/cm^3]
Epi - 50	49.0 ± 0.5	4060	100	4.9	6	200	4.4	6
Epi - 75	73.5 ± 1.0	4570	120	4.9	30	200	5.6	22
Epi -100	98 ± 2	4900	150	5.7	13	200	5.9	42

Test structures obtained from epitaxial patterned wafers using the ALICE pixel mask

Diodes HR, with different Cz substrate

Comparison after a neutron irradiation equivalent to 3 year PANDA lifetime

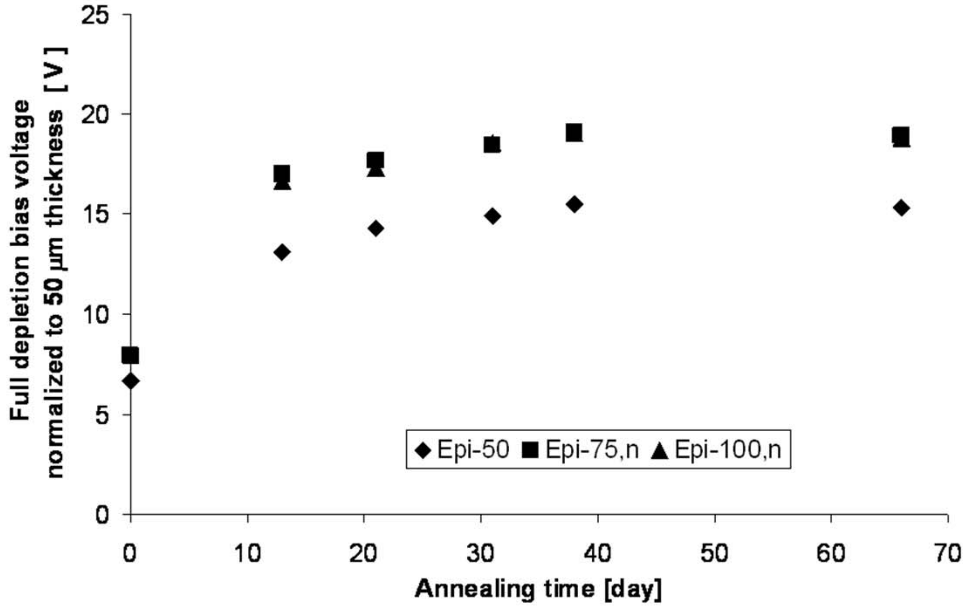
	Group HR (High Resistivity) thin CZ		Group HR (High Resisitivity) thick CZ	
Epi layer name	Full depletion voltage [v]	Current density [10^{-3} A/cm^3]	Full depletion voltage [v]	Current density [10^{-3} A/cm^3]
Epi - 50	6.7	11.5	6.7	13.2
Epi - 75	17.8	12.0	15.5	12.5
Epi -100	29.3	11.6	29.3	12.8

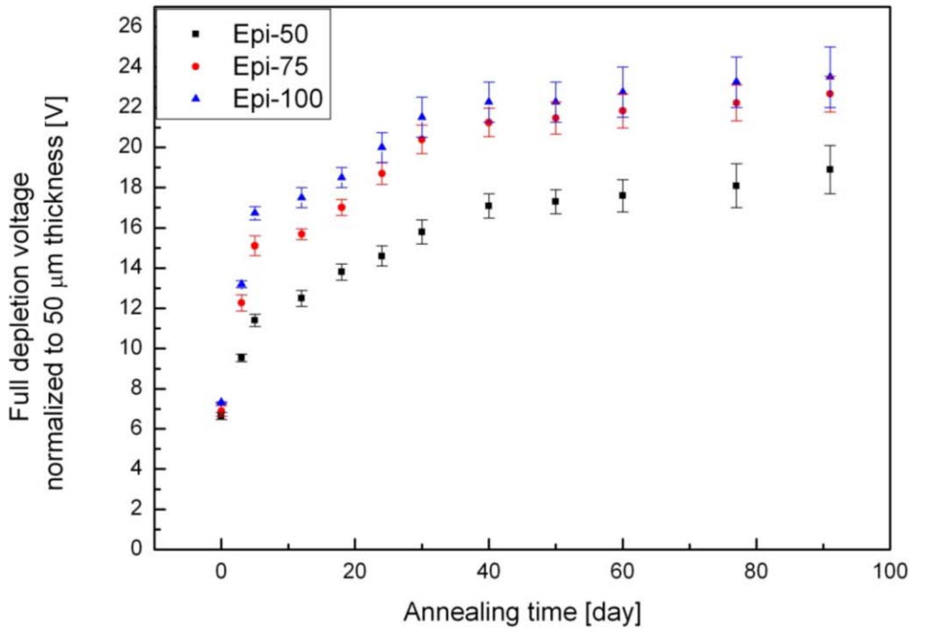
$$\alpha = (7.6 \pm 0.3) * 10^{-17} \frac{A}{cm} \qquad \alpha = (8.14 \pm 0.21) * 10^{-17} \frac{A}{cm}$$

Different CZ layers don't contribute
to the variation of the full depeltion voltage and current density
measured after the neutron irradiation

Diodes HR, with different Cz substrate

Comparison during an annealing phase at 60°C





Middle and lower resistivity epitaxial silicon devices

Diodes MR and LR before neutron irradiation

			Group MR (Middle Resistivity)			Group LR (Low Resisitivity)		
Epi layer name	Epitaxial thickness [μm]	Resistivity [Ω· cm]	Target thickness [μm]	Full depletion voltage [v]	Current density [10^{-8} A/cm^3]	Target thickness [μm]	Full depletion voltage [v]	Current density [10^{-8} A/cm^3]
Epi - 50	49.8 ± 0.6	3100	100	4.9	56			
Epi - 75	74.6 ± 0.9	3200	100	8.2	32			
Epi -100	99.8 ± 0.5	3610	120	10.4	35			
Epi -75	74.7 ± 1.2	460				100	42.6	46

Test structures from PANDA pixel wafers

Diodes MR and LR after neutron irradiation

Comparison after a neutron irradiation equivalent to 3 year PANDA lifetime

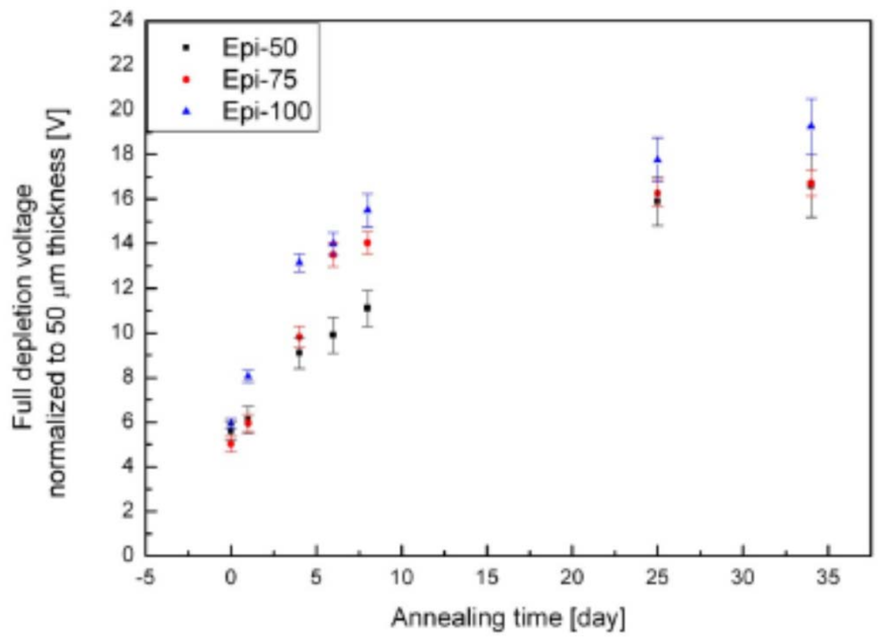
	Group MR (Middle Resistivity)		Group LR (Low Resisitivity)	
Epi layer name	Full depletion voltage [v]	Current density [10^{-3} A/cm^3]	Full depletion voltage [v]	Current density [10^{-3} A/cm^3]
Epi - 50	5.6	7.9		
Epi - 75	11.3	8.5		
Epi -100	23.7	6.4		
Epi -75			9.1	9.3

$$\alpha = (4.9 \pm 0.7) * 10^{-17} \frac{A}{cm}$$

$$\alpha = (6.2 \pm 0.8) * 10^{-17} \frac{A}{cm}$$

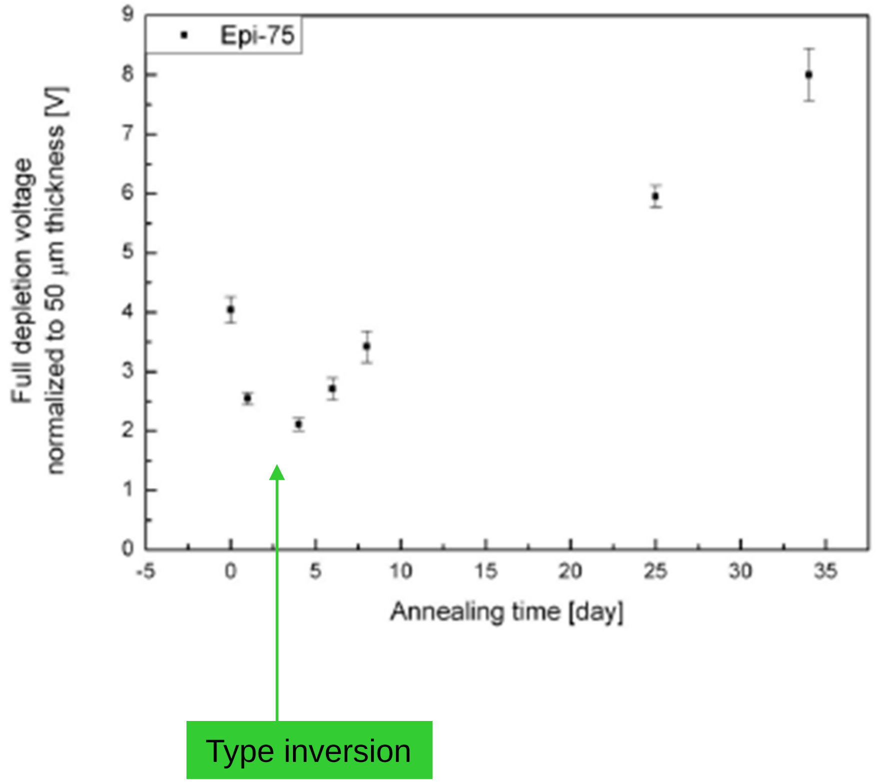
Annealing phase at 60°C - MR

Annealing time [days]	Full depletion Voltage [V]		
	Epi - 50	Epi - 75	Epi -100
0	5.6	11.3	23.7
1	6.1	13.4	32.2
4	9.1	22.1	52.6
6	9.9	30.4	56
8	11.1	31.6	62
25	15.9	36.6	71
34	16.6	37.6	77

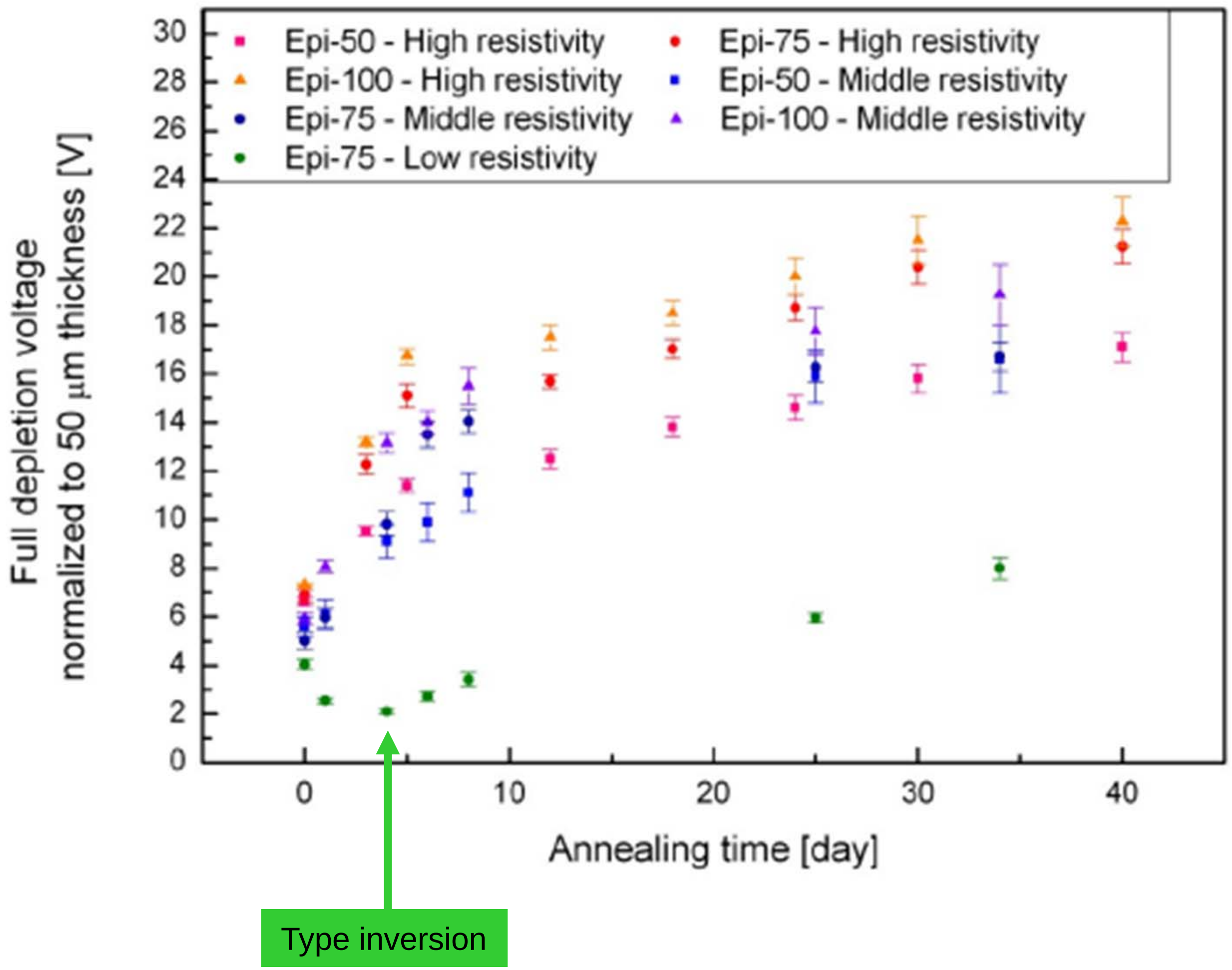


Annealing phase at 60°C - LR

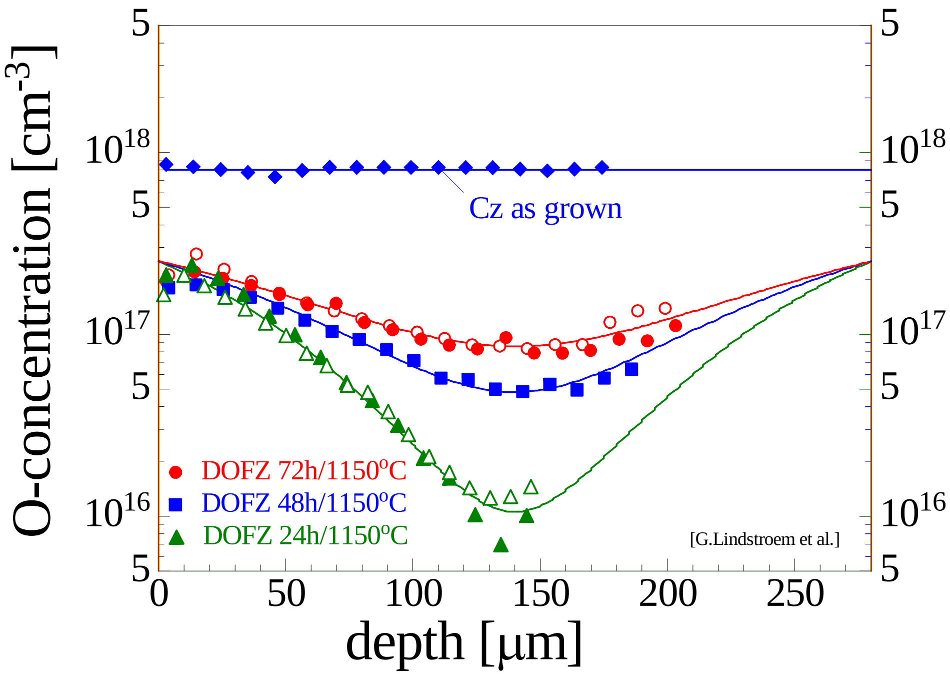
Annealing time [days]	Full depletion Voltage [V]
	Epi - 75
0	9.1
1	5.7
4	4.8
6	6.1
8	7.7
25	13.4
34	18



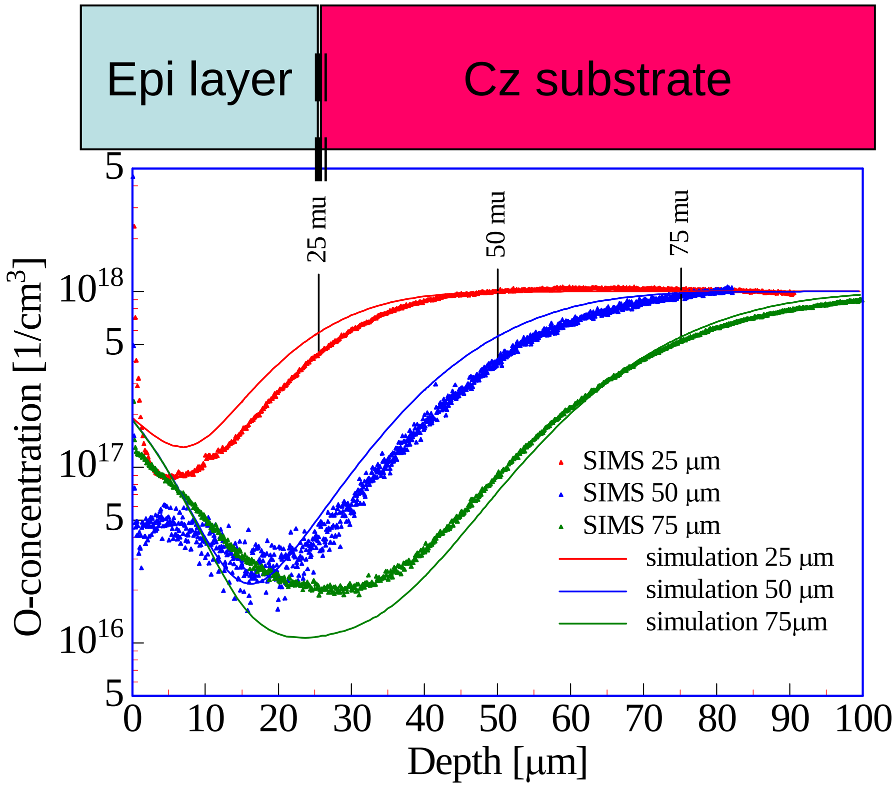
Annealing phase at 60°C - All



More oxygen for the epi wafers, 100 μm thick



Tests to increase the oxygen concentration
have to be performed (FBK)



[G.Lindström et al.,10th European Symposium on Semiconductor Detectors, 12-16 June 2005]

Aluminum strips: report on tests and simulations

Daniela Calvo[1], P. De Remigis[1], M. Mignone[1], T. Quagli [1,2] (degree thesis), Richard Wheadon[1]

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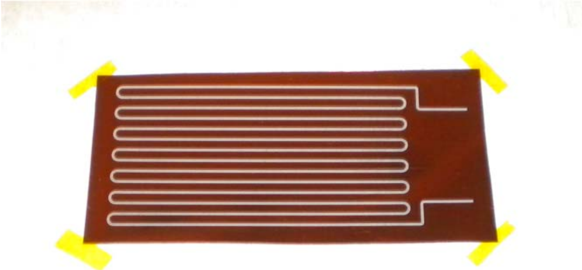
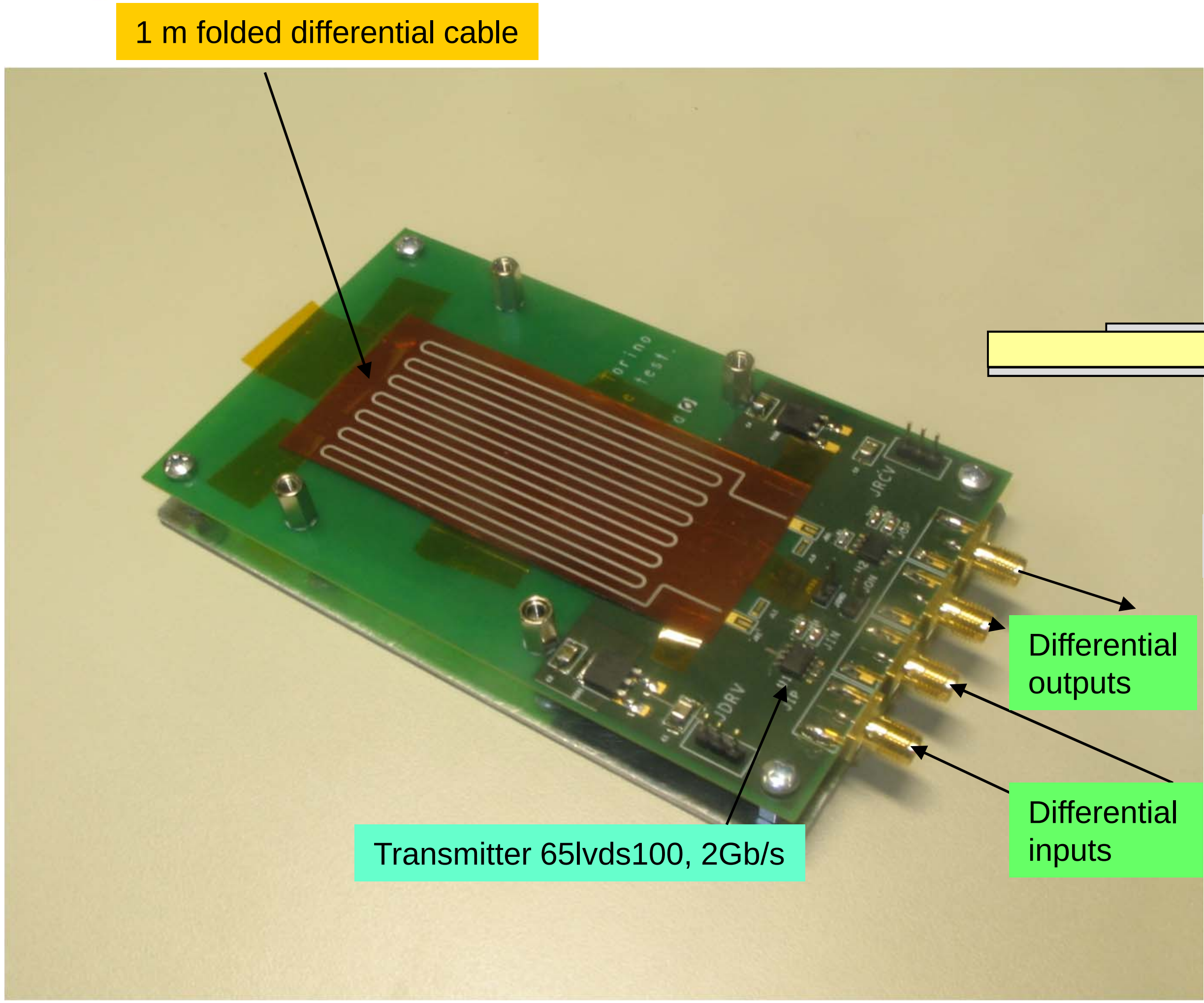
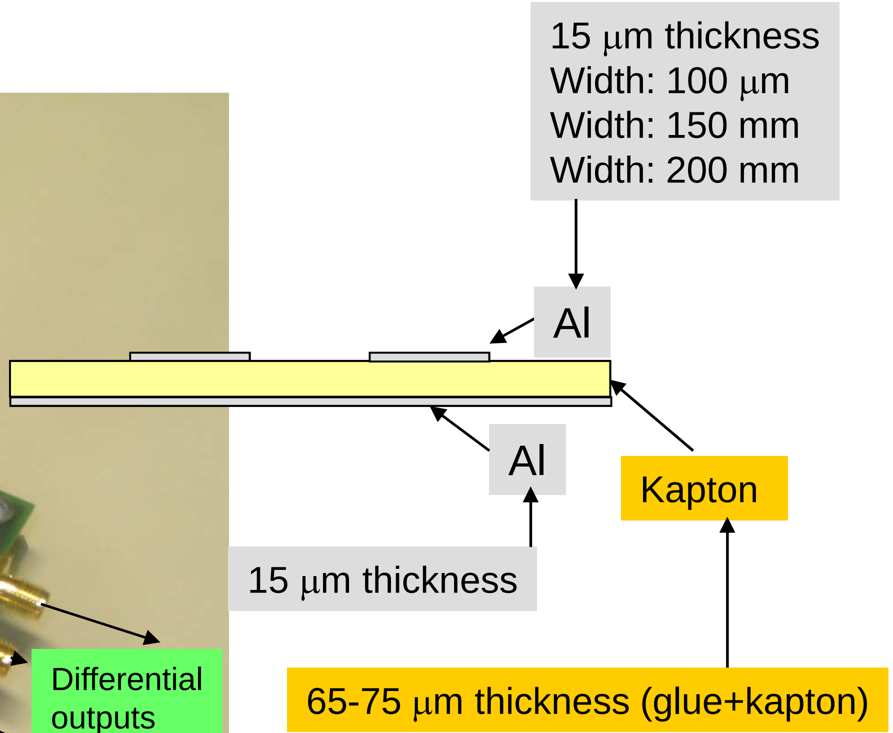
Aluminum folded strips

Aluminum folded strips

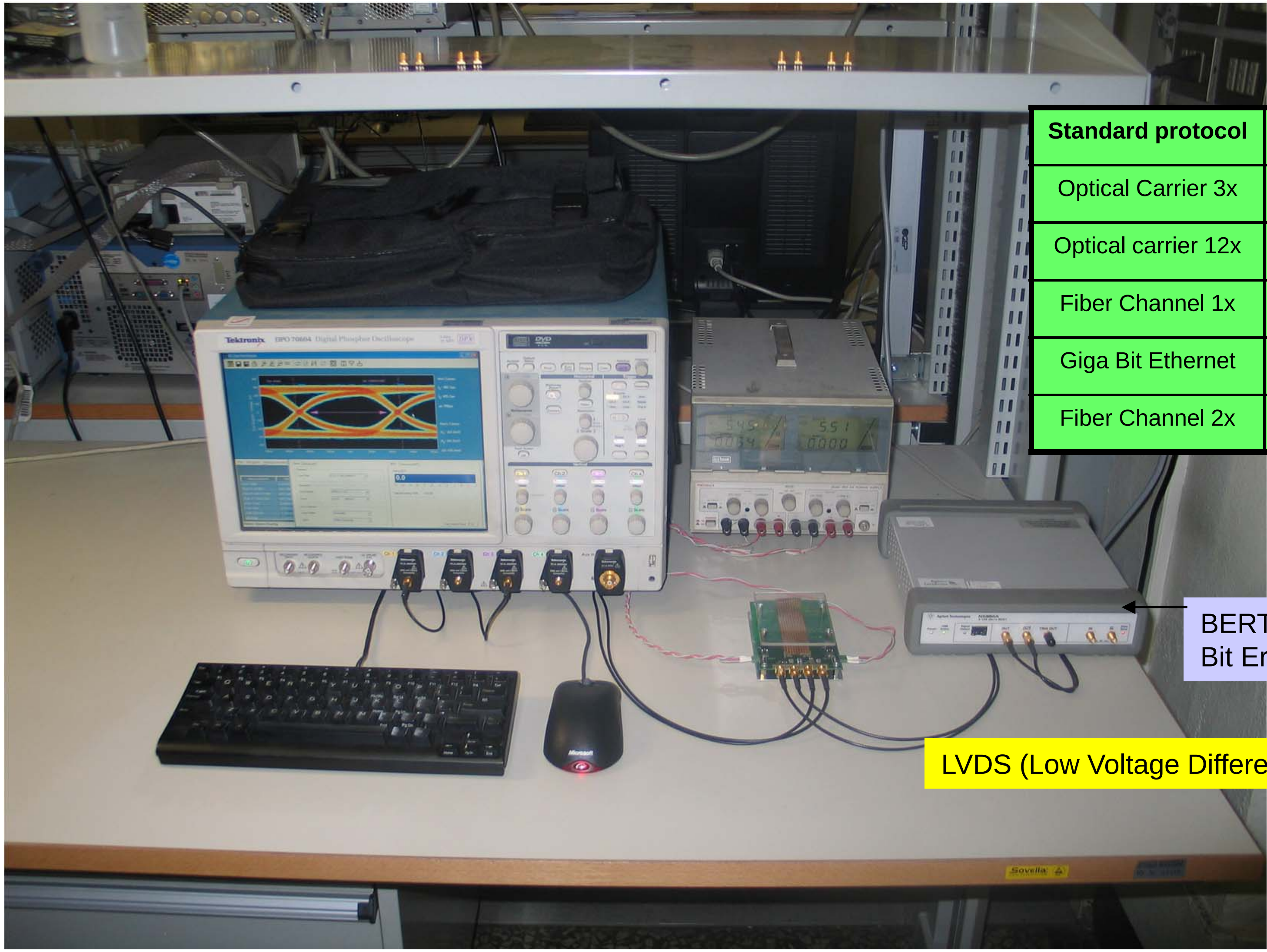


CERN
Technology with laminated aluminum on kapton, reliable for bonding





Aluminum folded strips

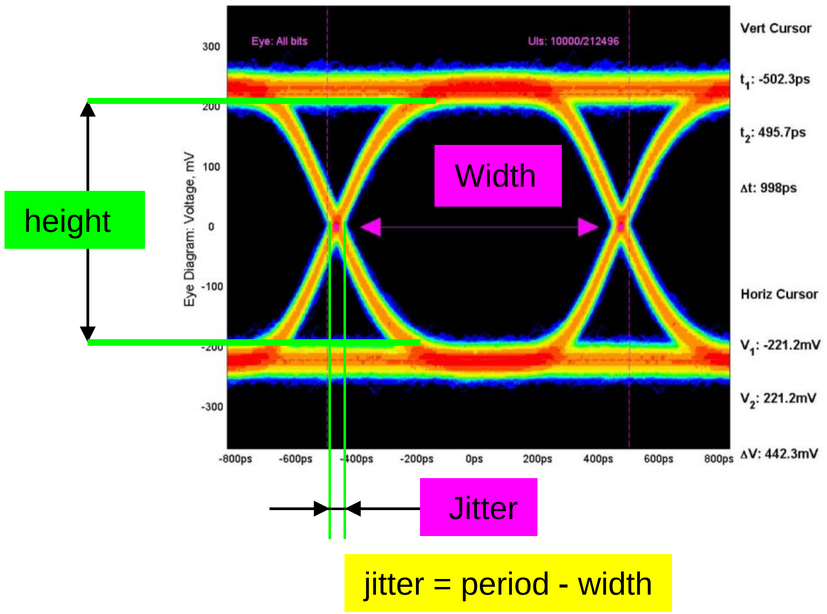


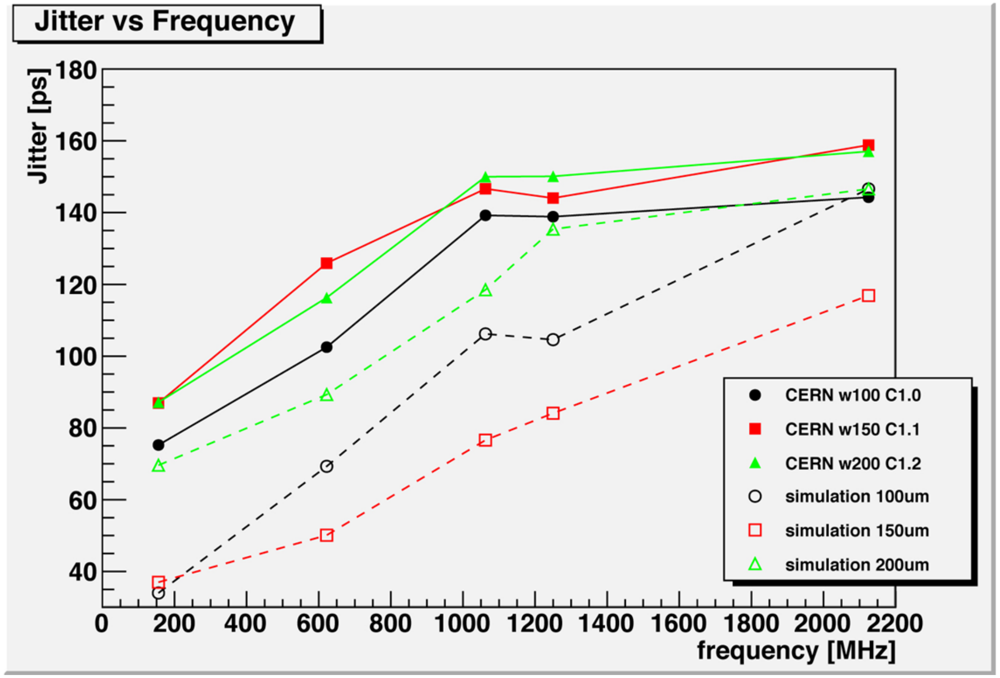
Standard protocol	Data rate [Gb/s]
Optical Carrier 3x	0.156
Optical carrier 12x	0.622
Fiber Channel 1x	1.060
Giga Bit Ethernet	1.250
Fiber Channel 2x	2.130

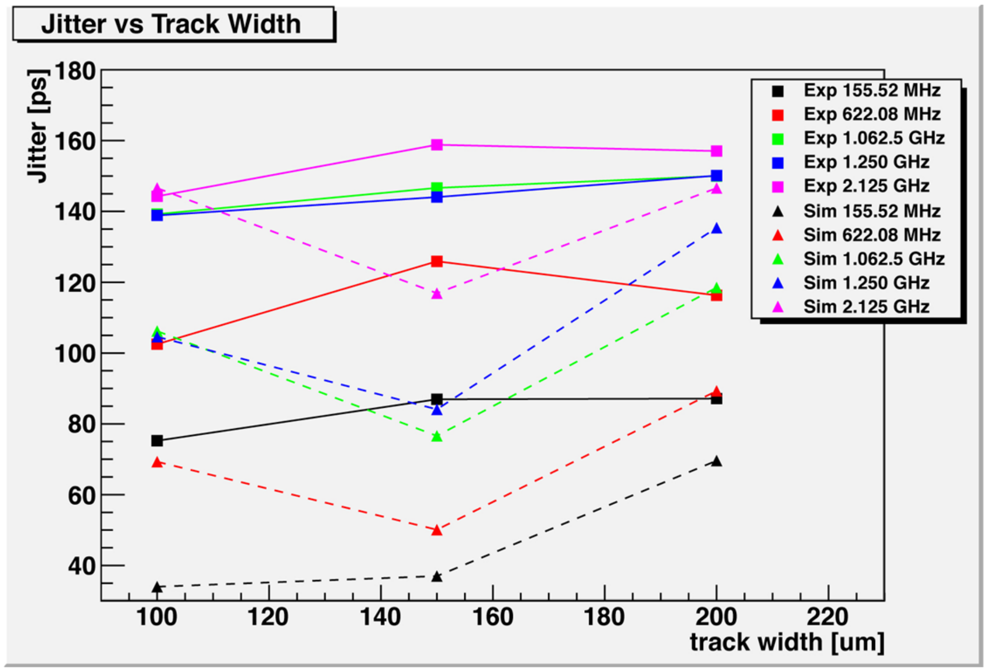
BERT
Bit Error Rate Tester

LVDS (Low Voltage Differential Signal)

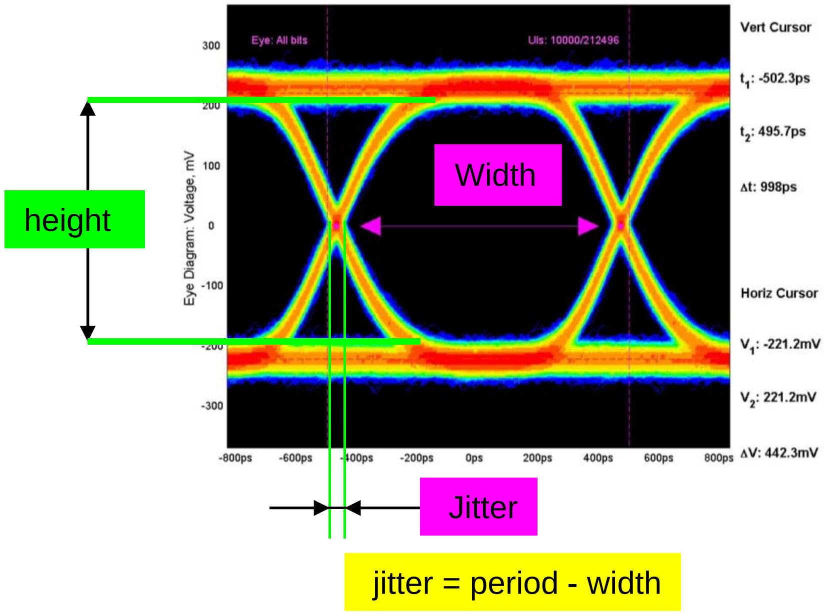
Measurement and simulation - Jitter

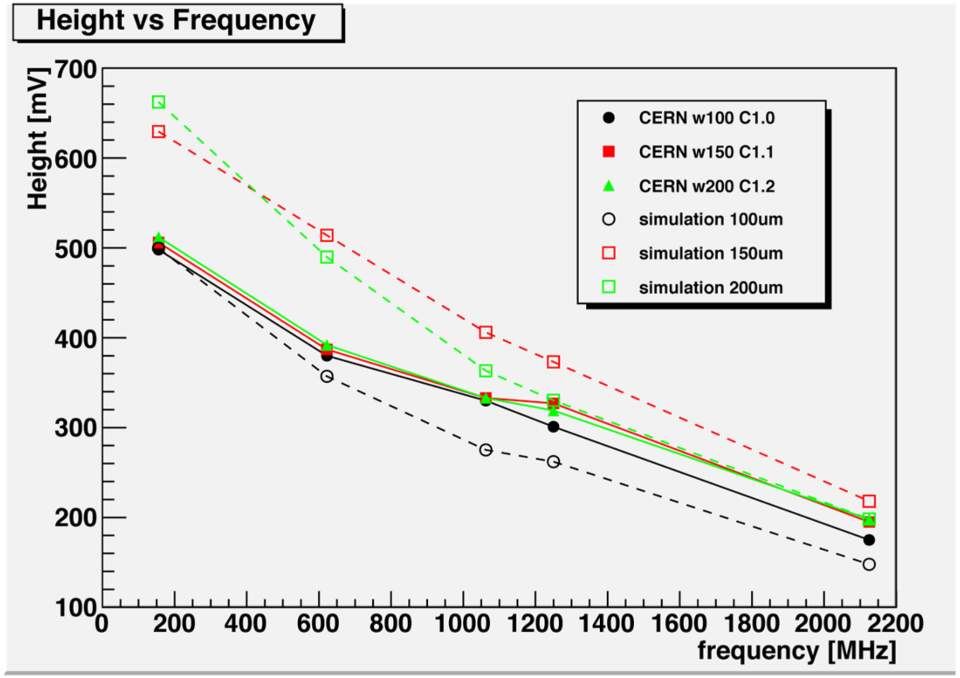


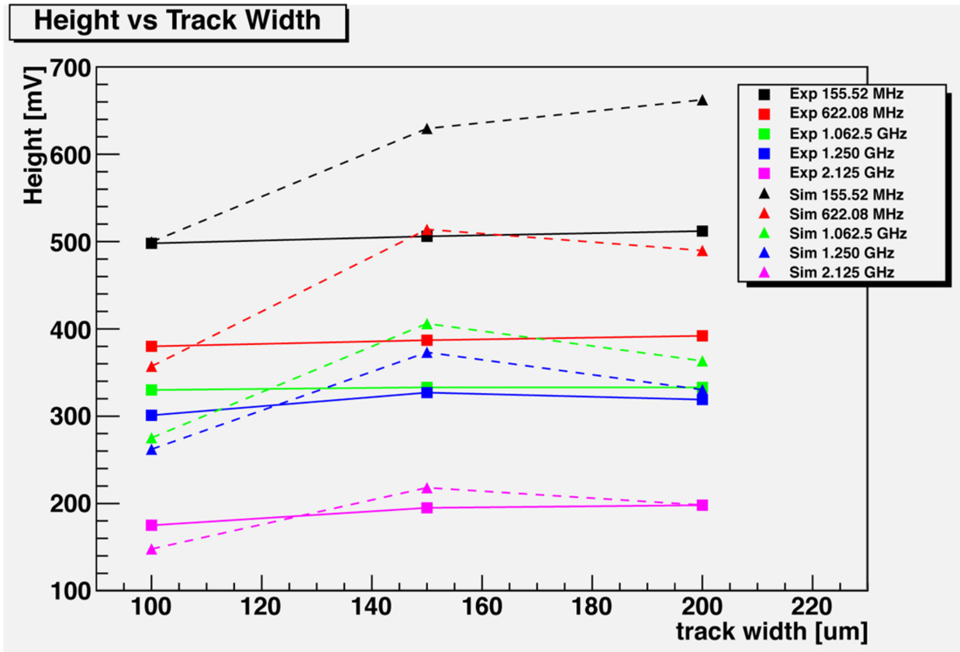




Measurement and simulation - Height







From LVDS to SLVS standard protocol

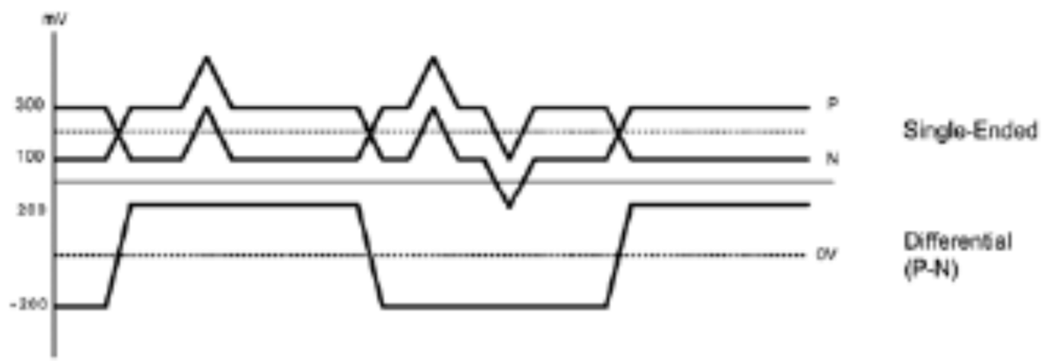
LVDS – Low Voltage Differential Signaling
(used in the 250 nm CMOS technology
@ 2.5 V)

Voltage swing: 400mV on 100 Ω load
Common mode: 1250 mV
Differential voltage: 800 mV

SLVS – Scalable Low Voltage Signaling
(used in the 130 nm CMOS technology
@ 1.2 V)

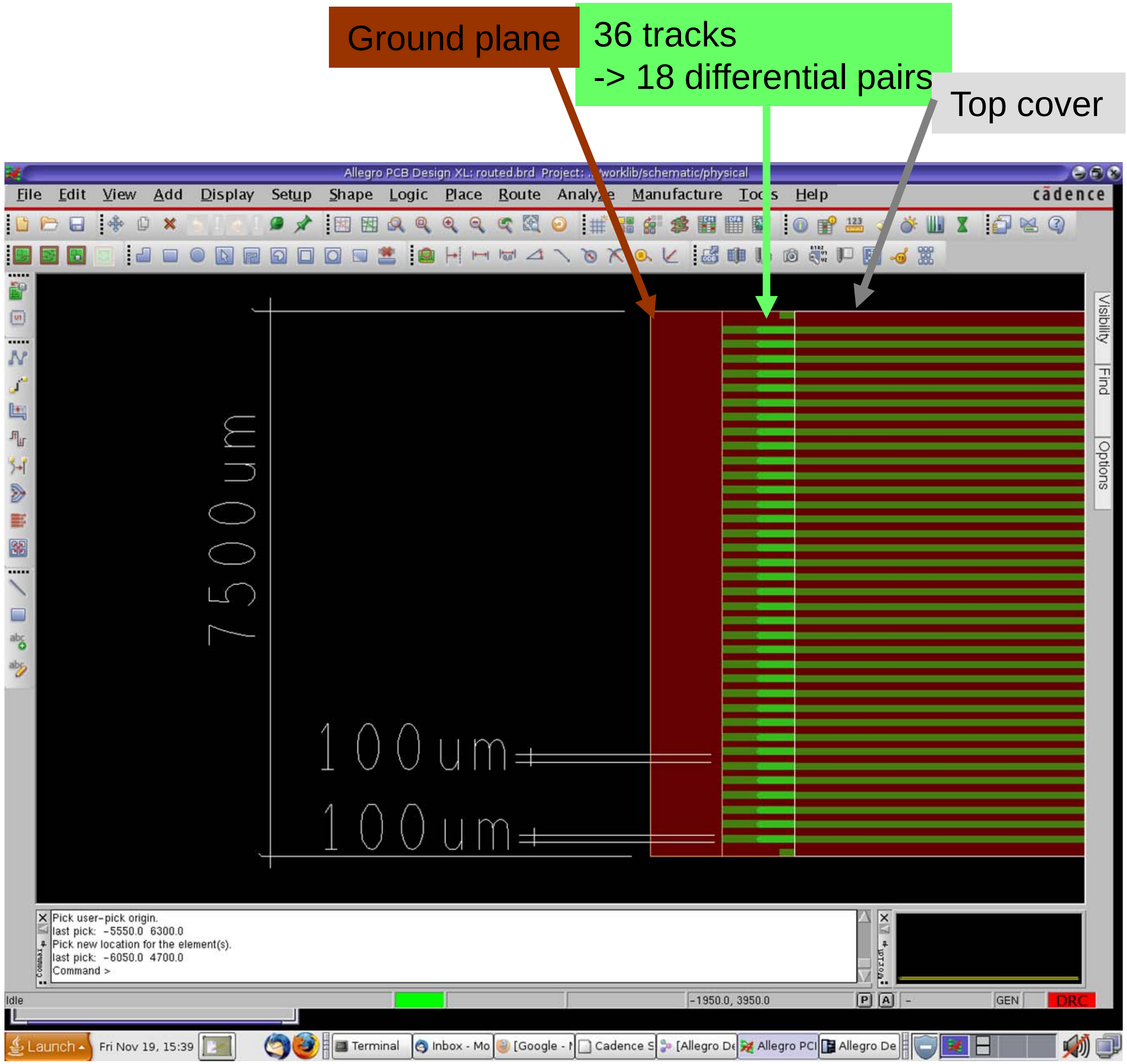
Voltage swing: 200mV on 100 Ω load
Common mode: 200 mV
Differential voltage: 400 mV

New tests are planned using the e-link ASIC
developed at CERN
4 chips are already in Turin
The bording test is under design
1 m long and straight aluminum stips

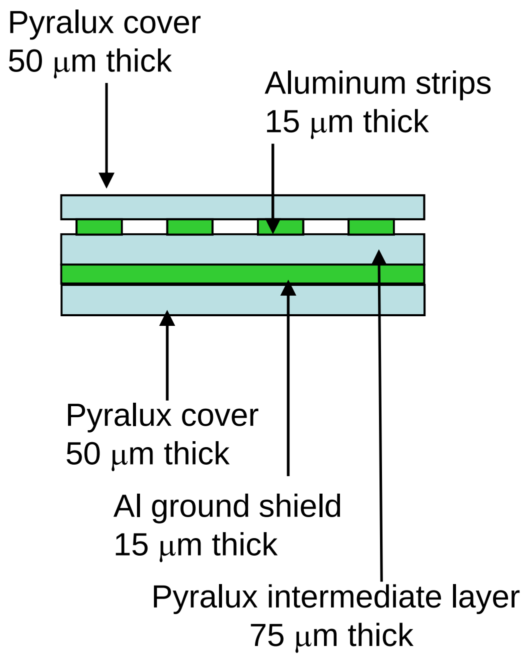


1 meter long aluminum strip prototype

One end of the strip-cable



Laminated aluminum technology

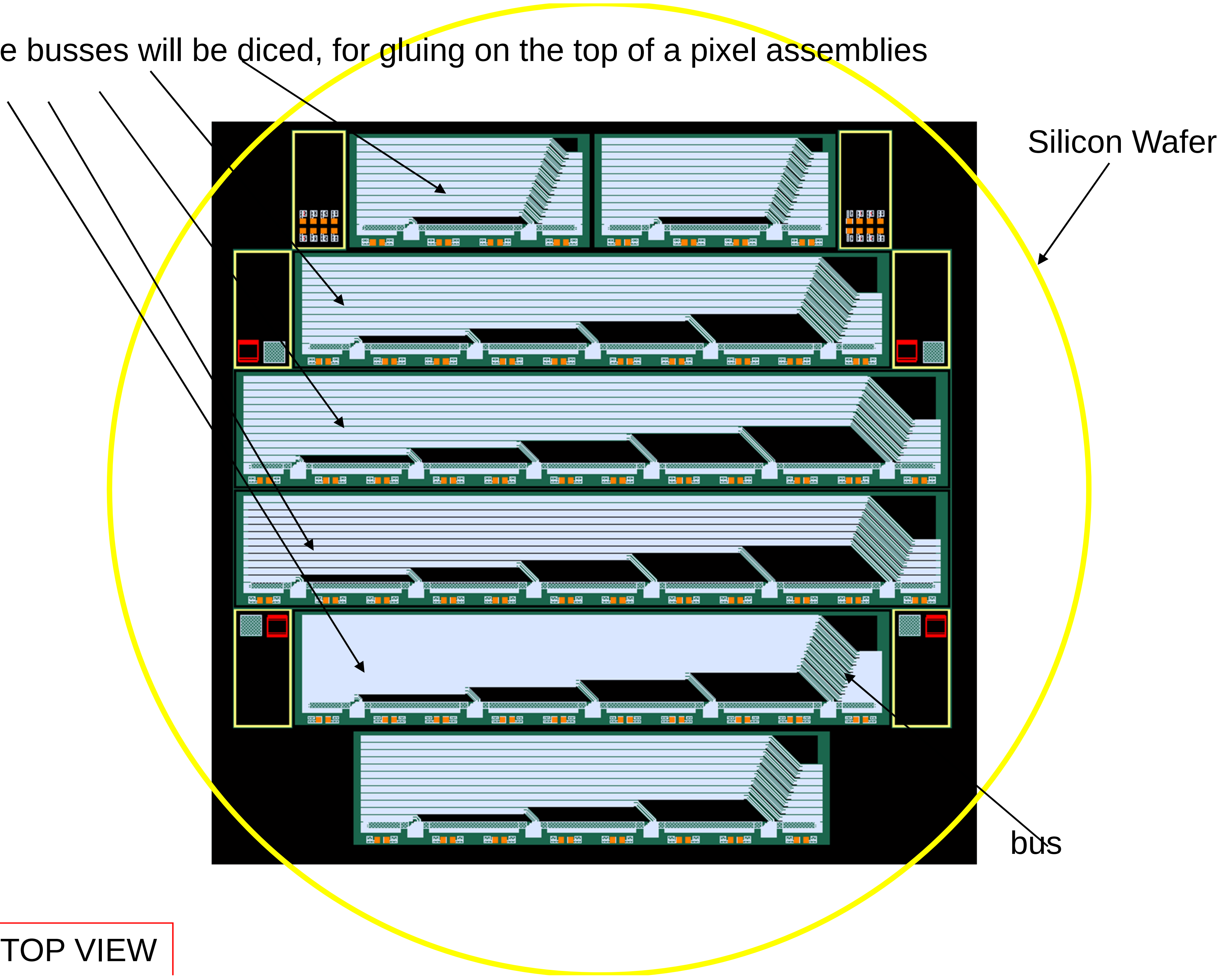


Bus prototypes:
first ideas

Daniela Calvo[1] on behalf of Richard Wheadon[1]

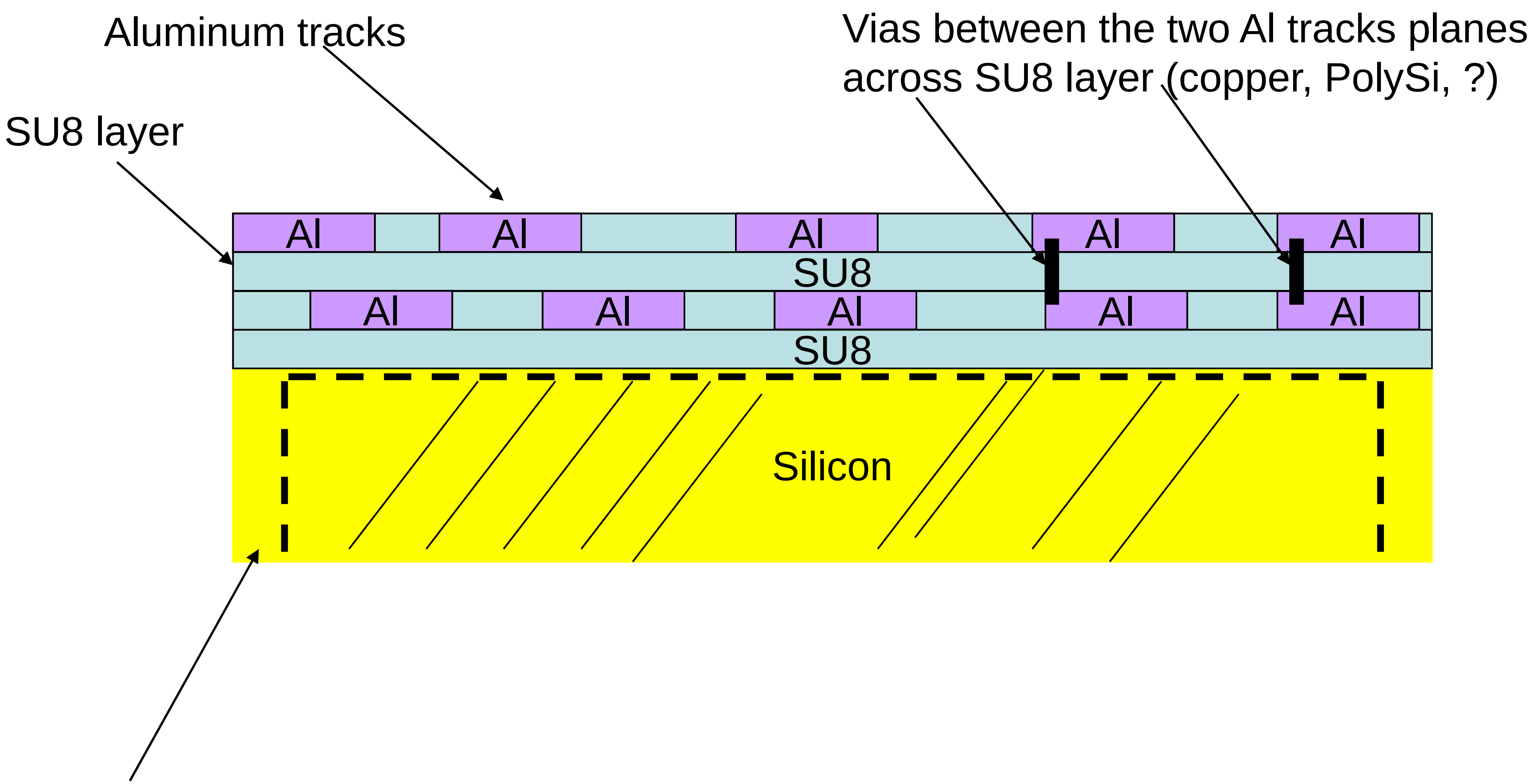
1- INFN - Torino

The busses will be diced, for gluing on the top of a pixel assemblies



TOP VIEW

Schematic lateral view (not in scale)



Silicon wafer, the most of Silicon has to be removed after SU8 and Al depositions, except for a perimeter frame for supporting

The Al tracks are about 100 μm width
and the thickness is supposed to be 5-10 μm,
The SU8 layer (or equivalent material, for dielectric constant)
has about the same thickness range