Pixel Detector

Sezione di Torino

Status report of the MVD pixel detector electronic readout system

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MVD

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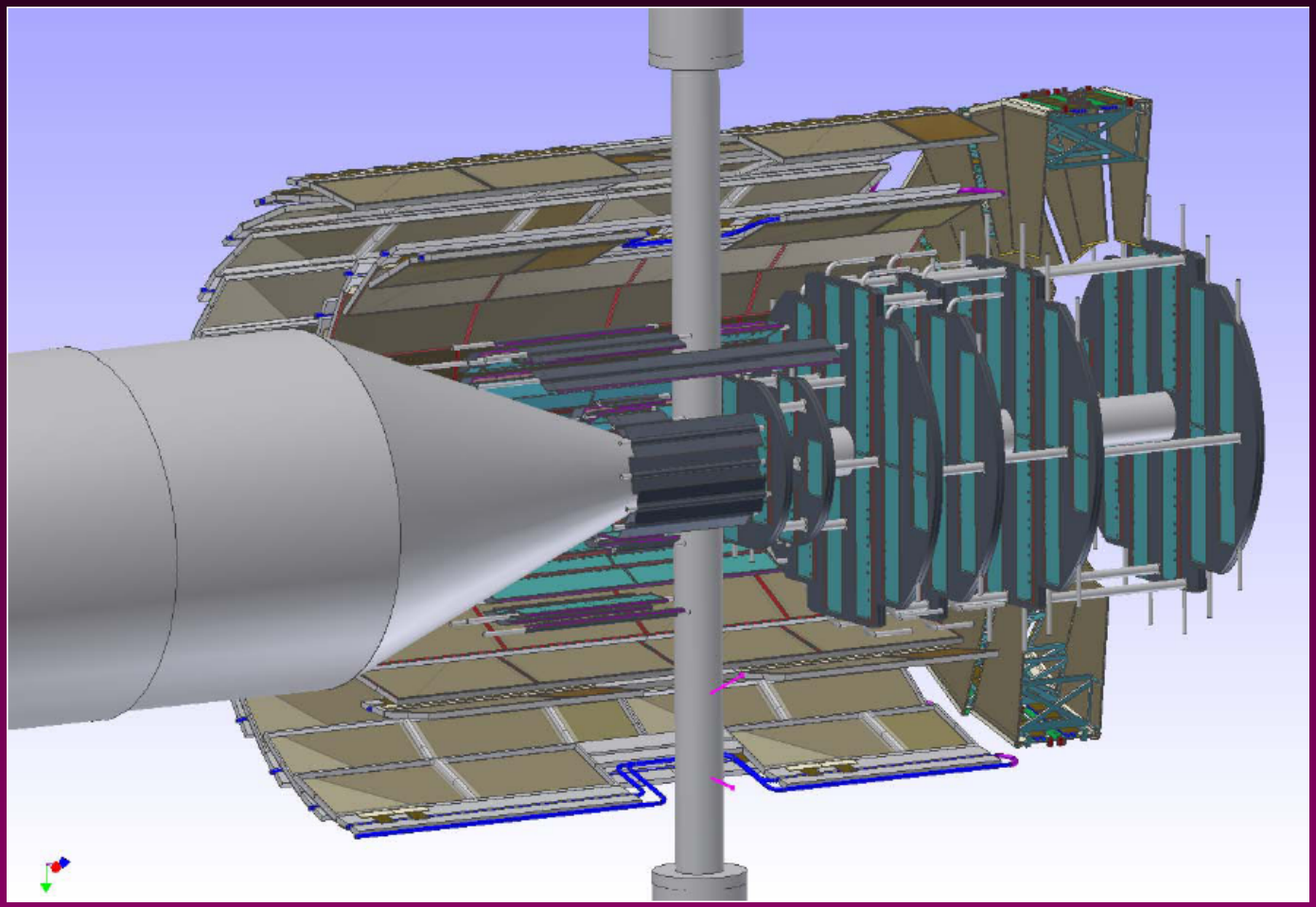

- Barrel :

  Layer 1 : radius 28 mm, SPDs

  Layer 2 : radius 53 mm, SPDs

  Layer 3 : radius 92 mm, SSDs

  Layer 4 : radius 120 mm, SSDs

- Forward :

  Disks 1-2 : radius 37.5 mm, SPDs

  Disks 3-4 : radius 75 mm, SPDs

  Disks 5-6 : radius 130 mm, SPDs + SSDs

Module concept

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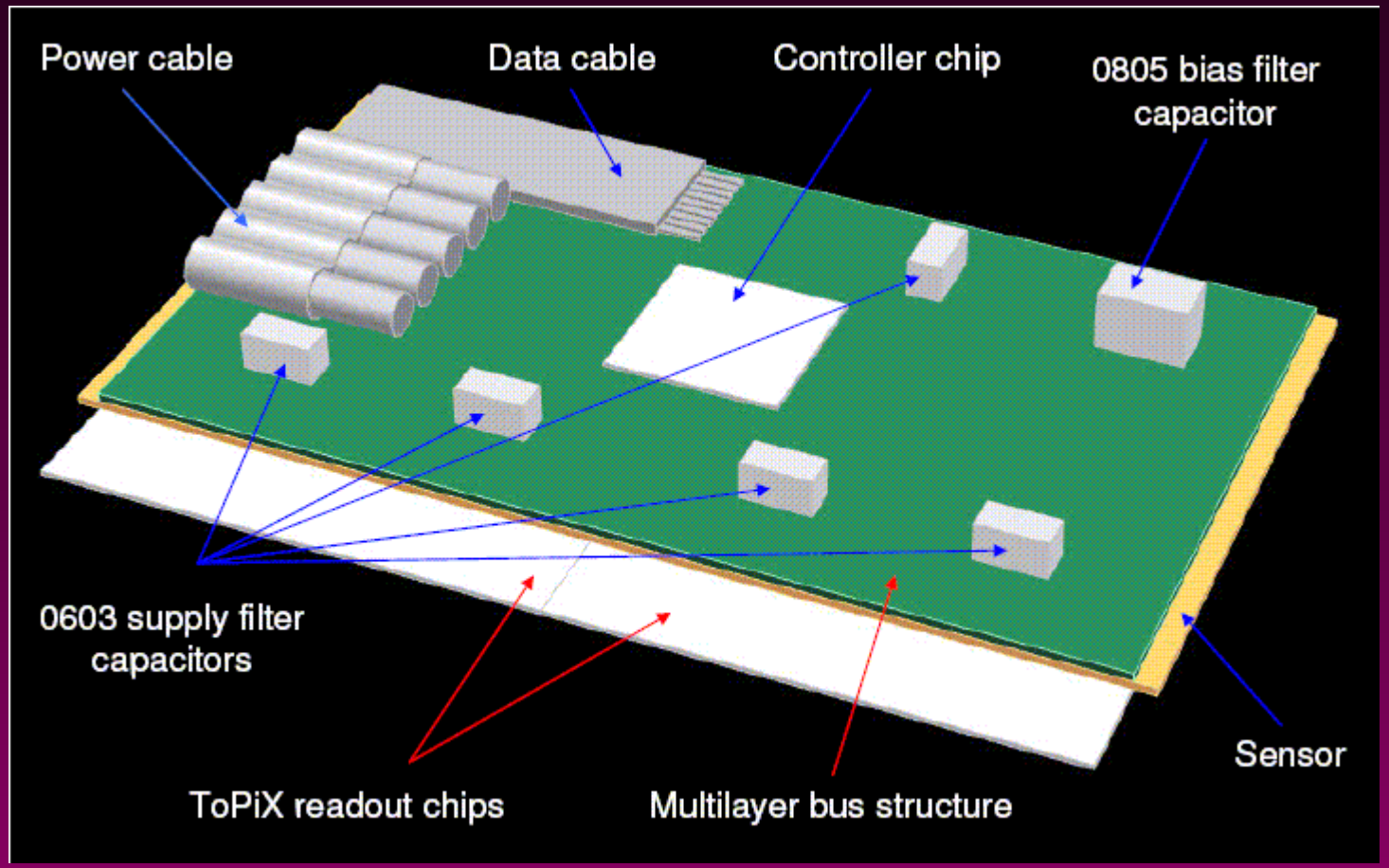

Module options

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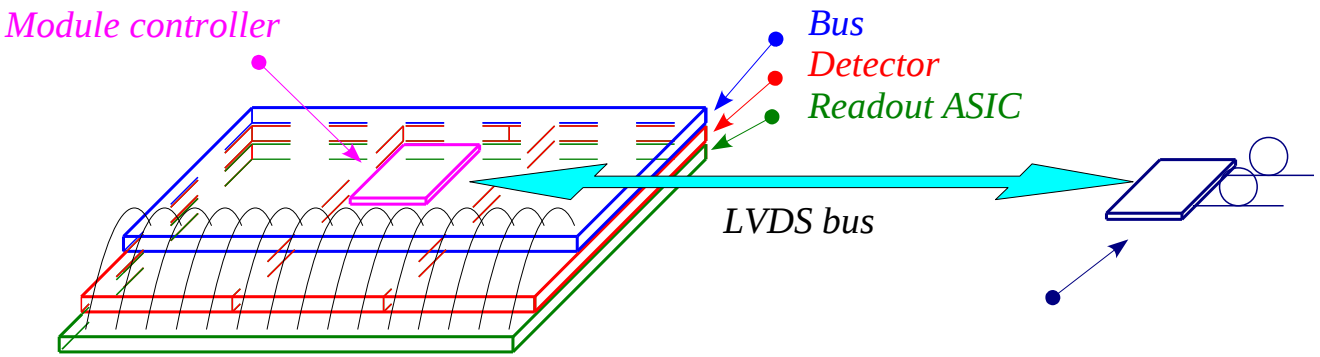
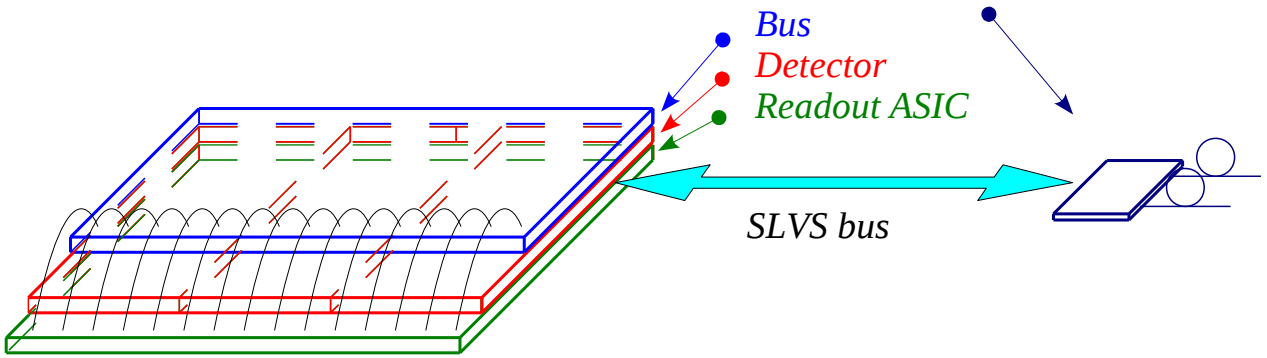


Option 1



Option 2

ToPiX ASIC

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- Provides spatial and time coordinates plus energy resolution measurement (via ToT)
- Compatible either with p-type or n-type detectors
- Self-reset circuitry for long signals
- Self triggered architecture
- Each event has a 12 bits time reference
- Data corresponding to a 12 bits counter cycle (26.21 μs) are packed in a frame, with an 8 bits frame counter (6.71 ms cycle)
- *Possible modification : counter cycle stopped at 3000 (19.2 μs, i.e. 8 bursts) - 8 bits frame counter cycle ~4.9 ms (8 super-bursts)*

ToPiX block diagram

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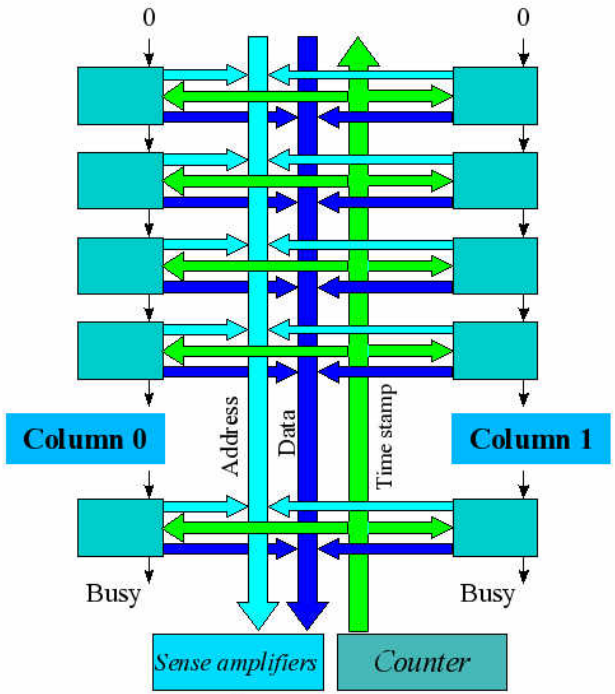

116 pixels/column
110 columns
50 bits/event
8.1 MHits/s
~400 Mb/s max output rate

Control logic

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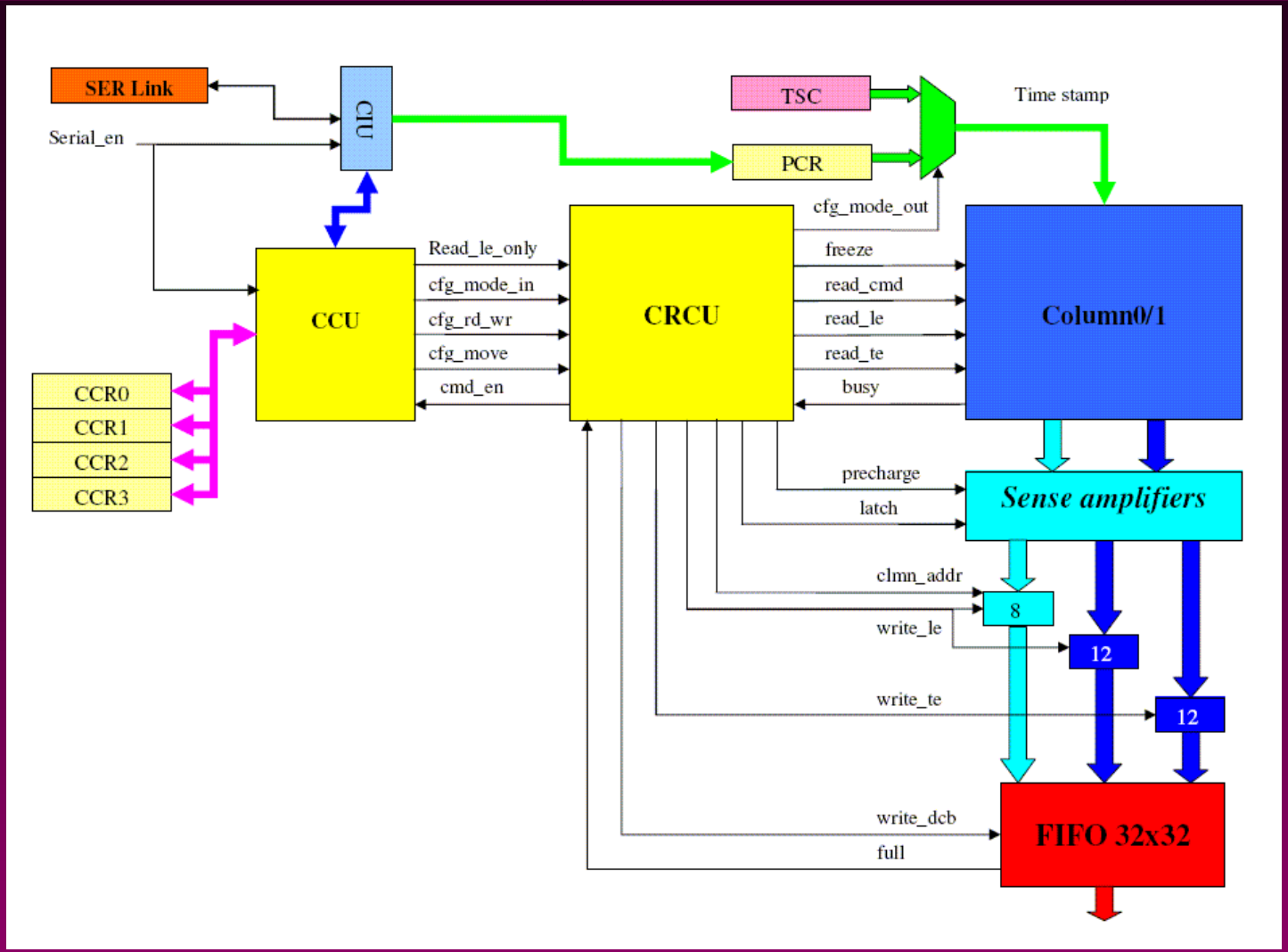

SLVS rx/tx

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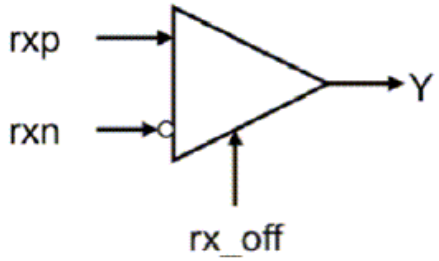
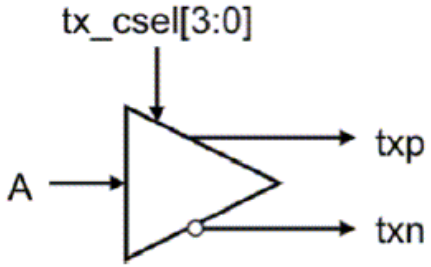
- Receiver
  - *Power Supply: 1.2V to 1.5V*
  - *Power Dissipation:*
    - *150uW @ 320Mbs, 1.2V supply*
    - *<1uW @ power down*



- Driver
  - *Power Supply: 1.2V to 1.5 V*
  - *Power Dissipation:*
    - *3.1mW @ 320Mbs, 1.2 V supply*
    - *<10uW @ power down*



- Engineer
  - Sandro Bonacini – CERN, Switzerland

Electrical Specifications

Symbol	Parameter	Notes	Min	Typ	Max	Units
V_{OD}	Differential output voltage		110	200	320	mV
ΔV_{OD}	Differential output voltage change	(fig.1)	0	14	20	mV
V_{OS}	Driver offset voltage		100	200	350	mV
I_{SCO}	Output short-circuit current	V_{OS}=0, V_{OD}=0		-25	-60	mA
I_{SCOD}	Differential output short-circuit current	V_{OD}=0		-3	-5	mA
I_{DD}	Supply current			2.5	4.0	mA

Programmable Output Current

csel[3:0]	Output current [mA]	Driver power dissipation [mW]
8	2.0	3.0
4	1.3	2.1
2	0.8	1.4
1	0.5	1.0
(sleep) 0	0	<.01

Note: All values are given at 1.2V power supply voltage, typical conditions.

SLVS Driver test with Al cables ongoing

Two pixel cells

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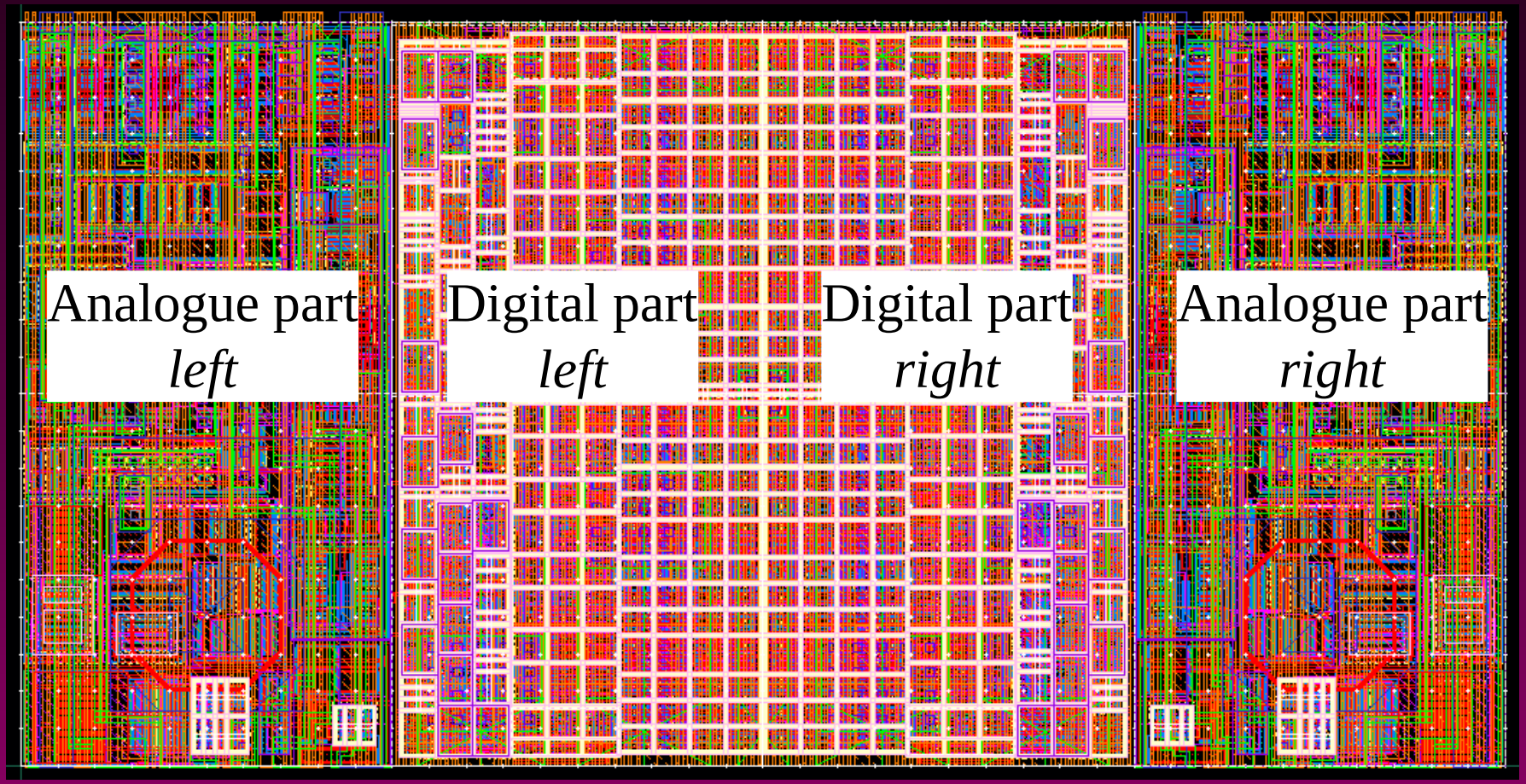

Common bus

ToPiX v3 layout

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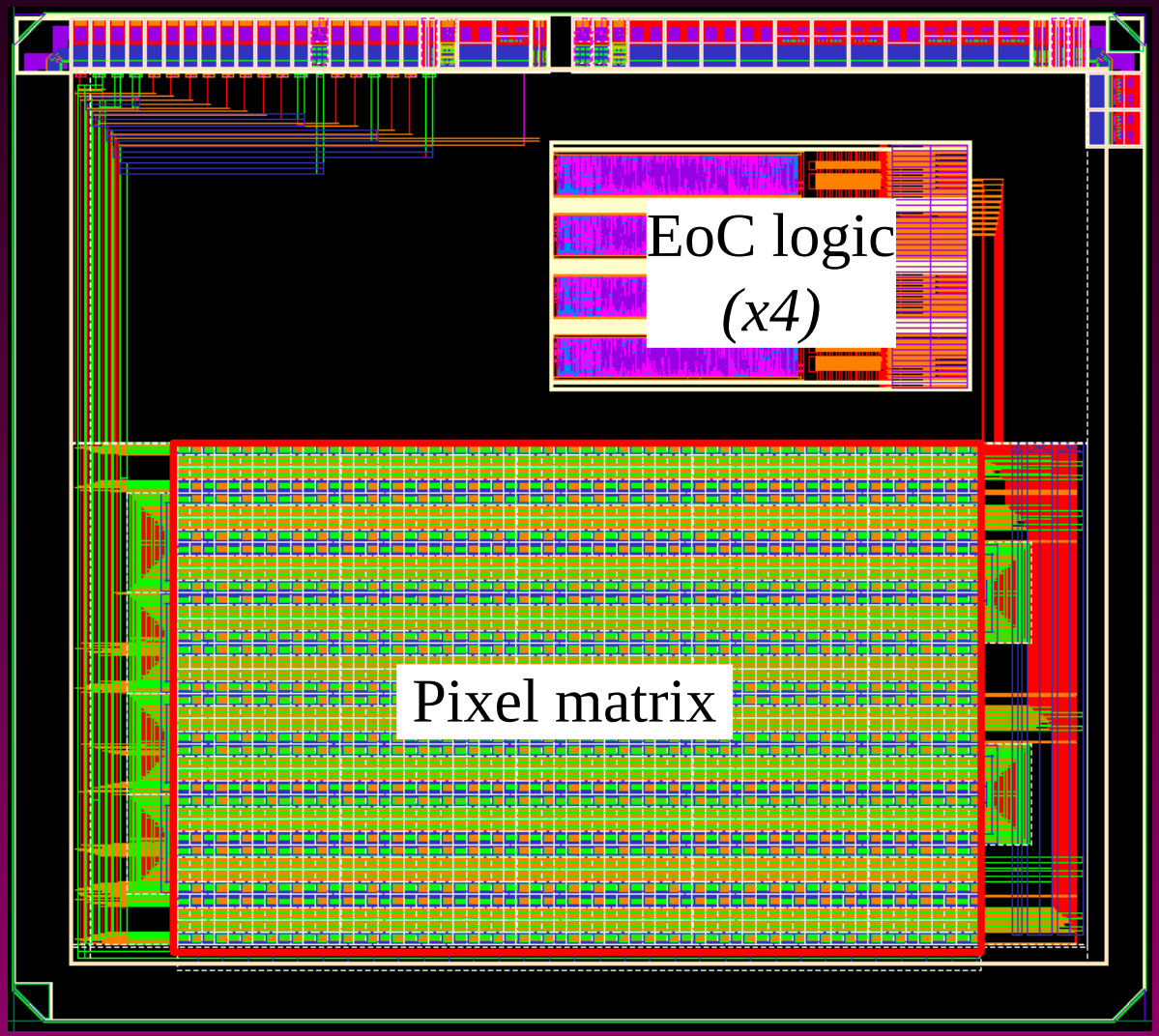

Chip area : 4.5 × 4 mm^2
4 × 128 cells columns
4 × 32 cells columns
Cell size : 100 × 100 μm^2
EoC logic size : 0.2 × 1.7 mm^2
SLVS differential I/O

Column delay

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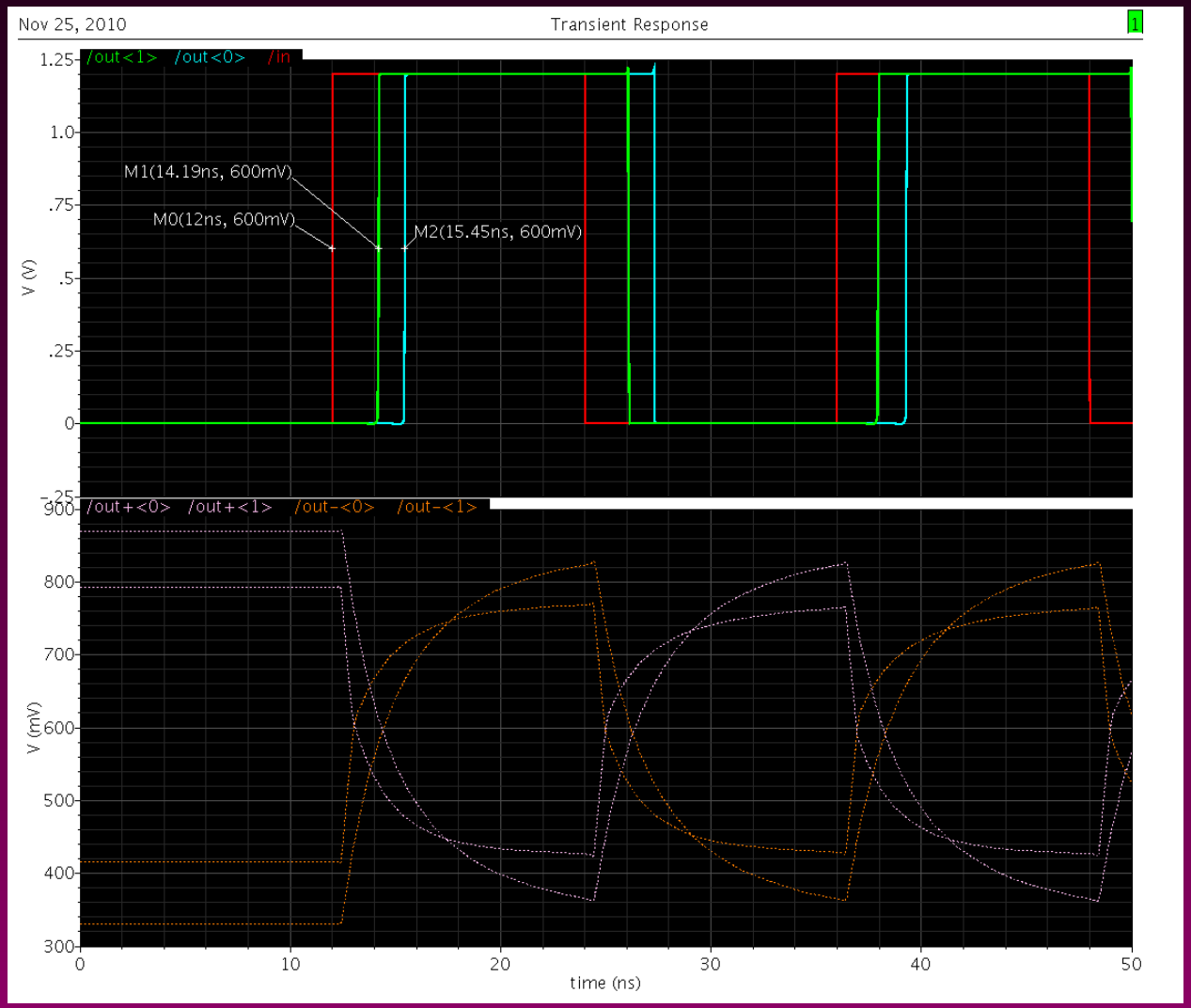

Max delay :

3.3 ÷ 3.5 ns (no PE)

1.4 ÷ 1.8 ns (PE)

Receiver schematic

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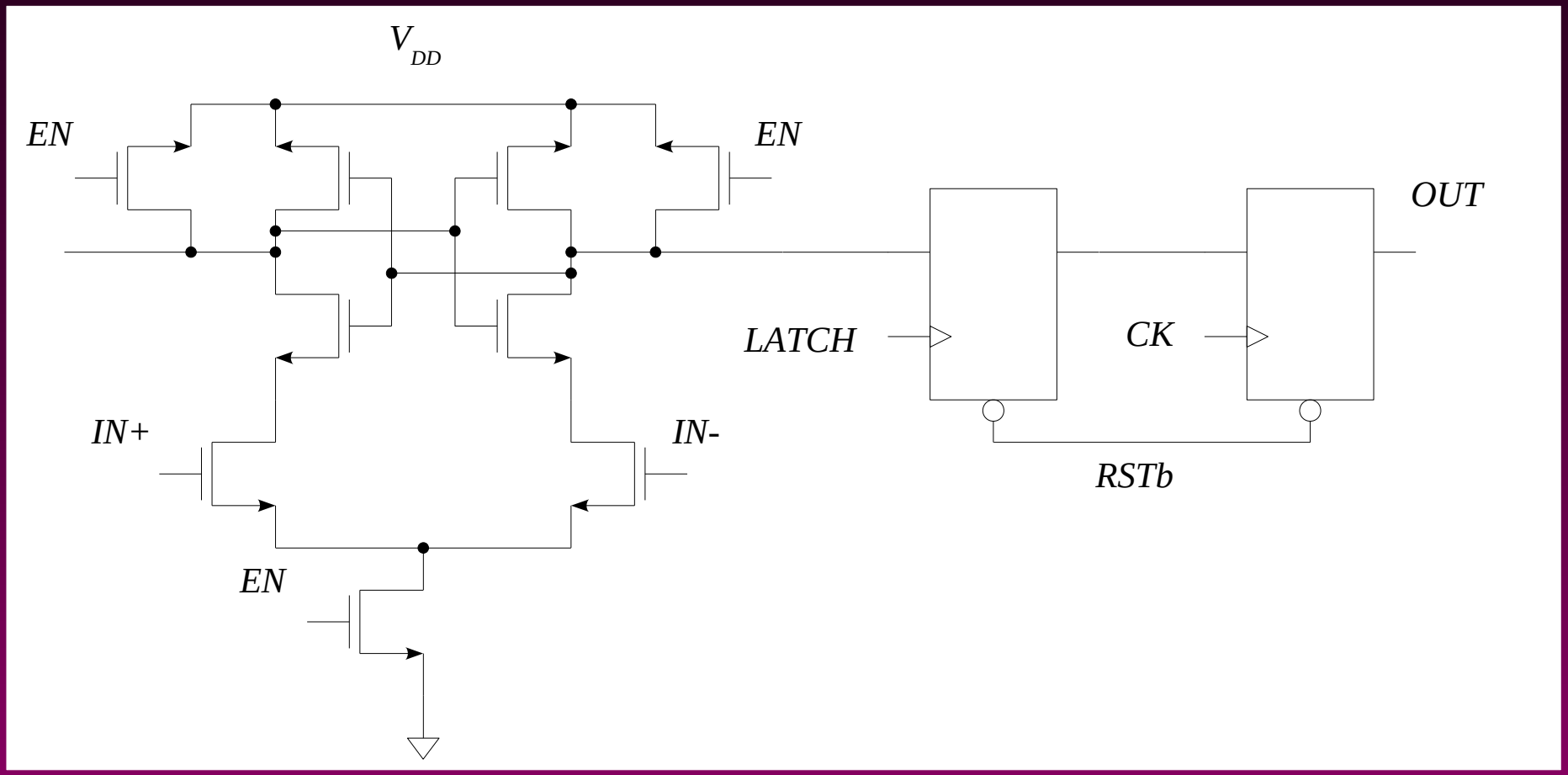
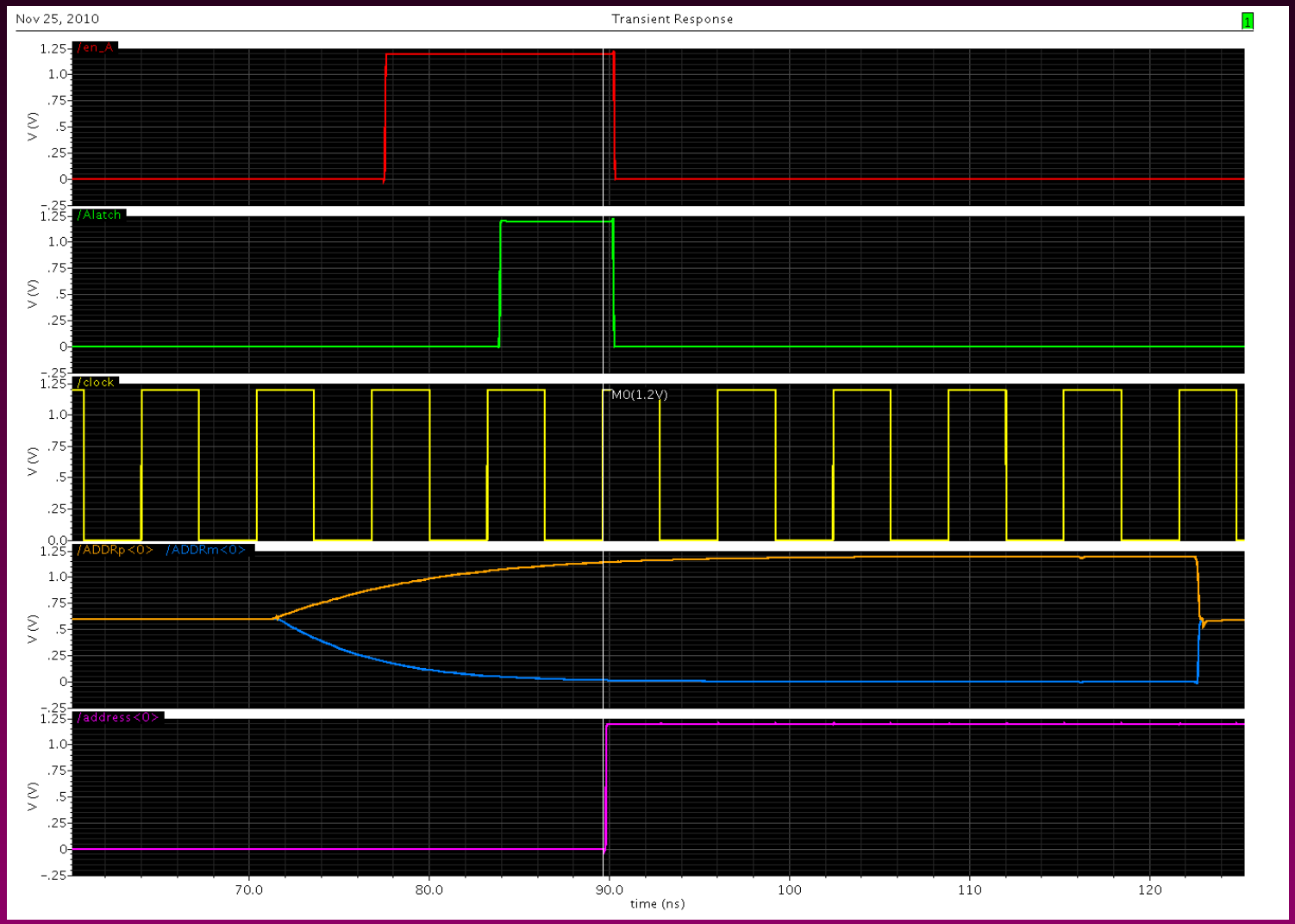


Column receiver

Sezione di Torino



Hiccup...

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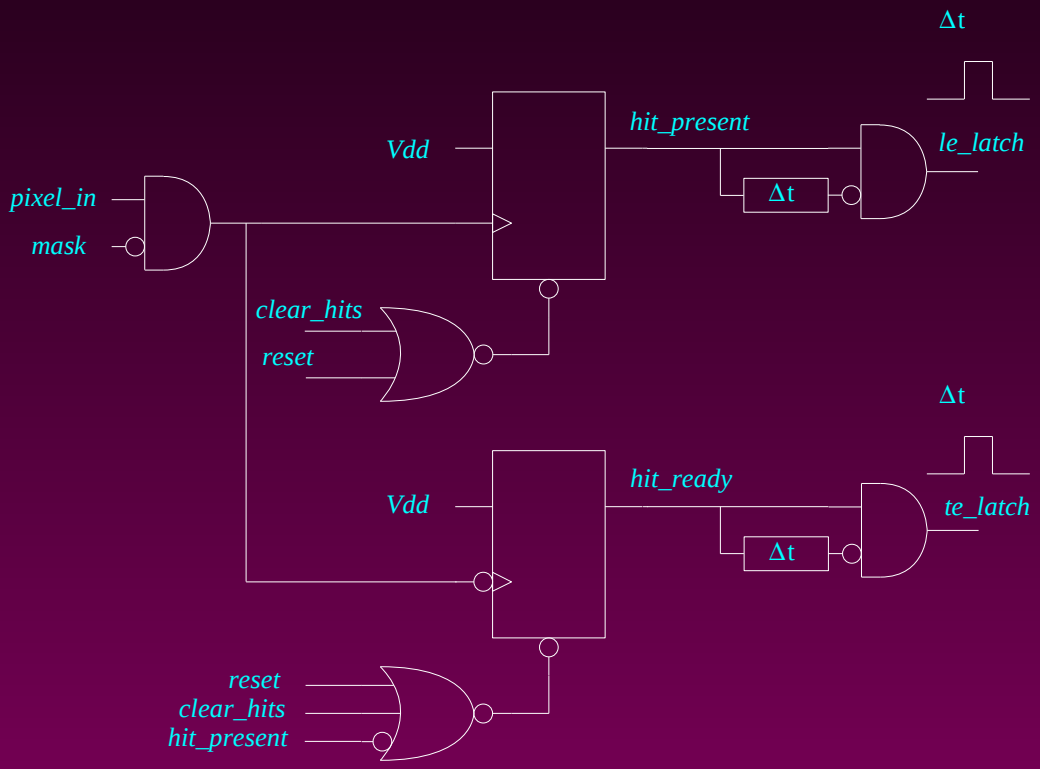

Standard cell based delay line fails to generate a signal in post-layout simulations for all process corner.

Problem discovered too late to meet submission deadline → *rescheduled to February 7th* .

New hand-made delay cell designed.

Process corner	tt	ff	ss	fs	sf
Pulse width	1.75 ns	1.1 ns	2.7 ns	2.32 ns	1.32 ns

Conclusions

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- ToPiX :
  - Pixel cell and column design completed
  - End of column logic design completed
  - Data transmission logic design ongoing
    - ➔ *Submission postponed to February 7th 2011* ☹
- Data transmission :
  - E-link interface for the current prototype
  - GBT tests ongoing at CERN
- Future steps :
  - ToPiX version 3 submission and tests
  - Irradiation tests (TID and SEU)
  - ToPiX v3 – detector and ToPiX v3 – GBT tests
  - GBT-FPGA customization for PANDA (interface with SODA and DAQ)