XXXV PANDA Collaboration Meeting
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ToPix3 Analog Cell Design & Simulation

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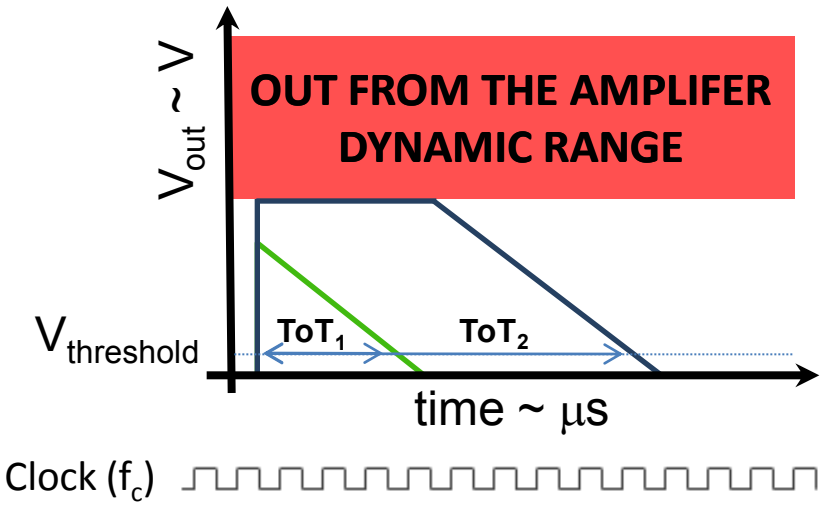
Pixel Readout Cell Specification

Pixel Size	100µm x 100µm
Input charge range	≈ 1fC to 50fC
Noise (ENC)	< 200 e^-
Power consumption	15µW
Input polarity	Selectable
Leakage compensation	Up to 50 nA
Average Hit Rate	≈ 10^3 hits/s
Trigger	Self triggering
Radiation tolerance	10 Mrad

Simultaneous time stamping (12bit) and charge measurement
Good time resolution ≈2 ns rms (at 155 MHz clock) with $2 \cdot 10^7$ ann/s

Technology CMOS 8RF 130nm

Time Over Threshold



Constant Current Feedback

$$V_{out}(t) = \frac{Q_{in} - I_{dis}t}{C_f}$$

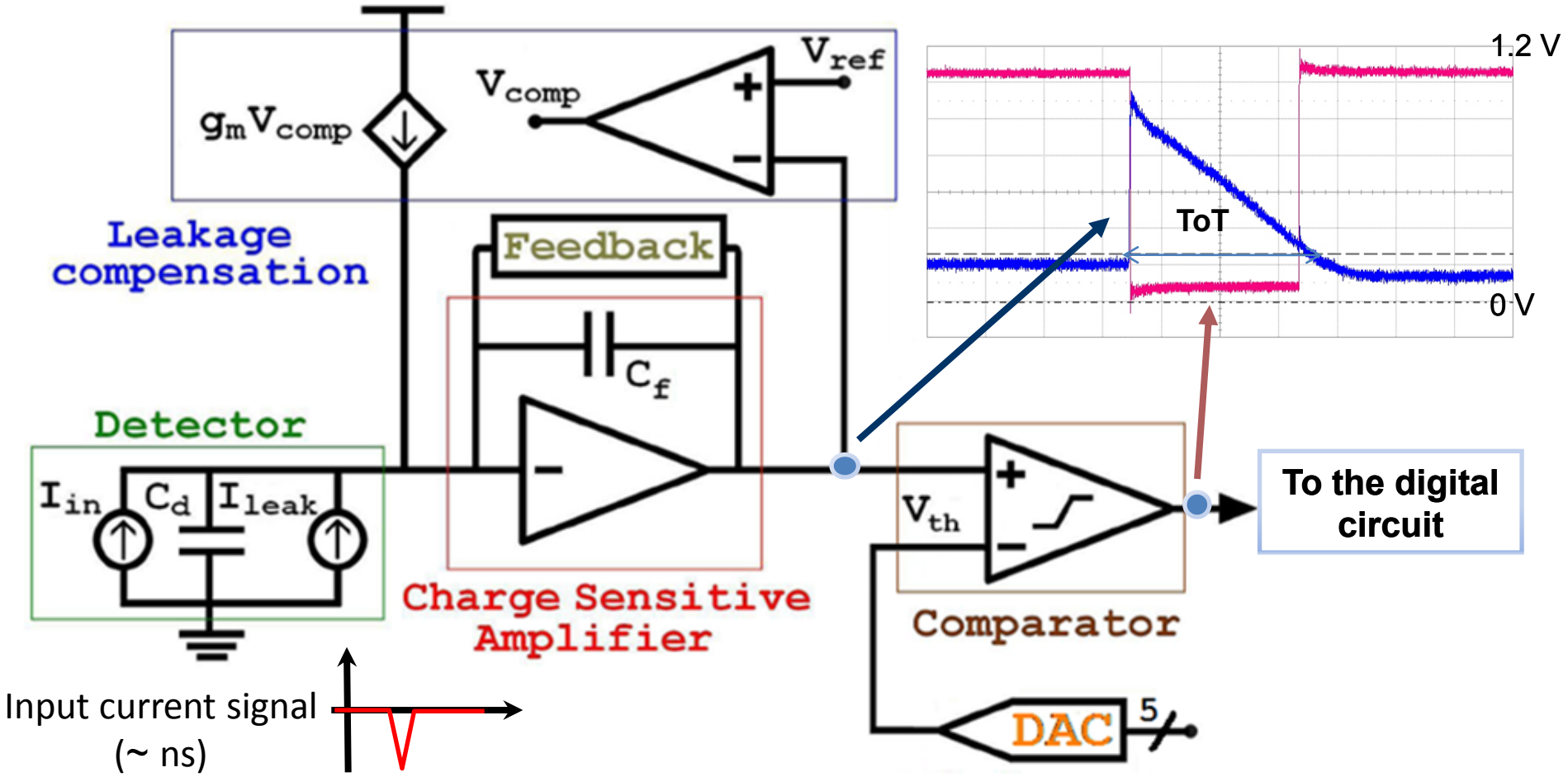
$$ToT = \frac{Q_{in}}{I_{dis}}$$

$$\delta Q = \frac{1}{f_c}\frac{\partial Q}{\partial t}\frac{1}{\sqrt{12}} = \frac{I_{dis}}{f_c}\frac{1}{\sqrt{12}}$$

With I_{dis} = 5nA and f_c = 155MHz the resolution in charge digitization is δQ = 59 e^-

The ToT allows us to achieve good linearity and excellent resolution even when the preamplifier is saturated, thus making room for an high dynamic range.

Analog Front-End



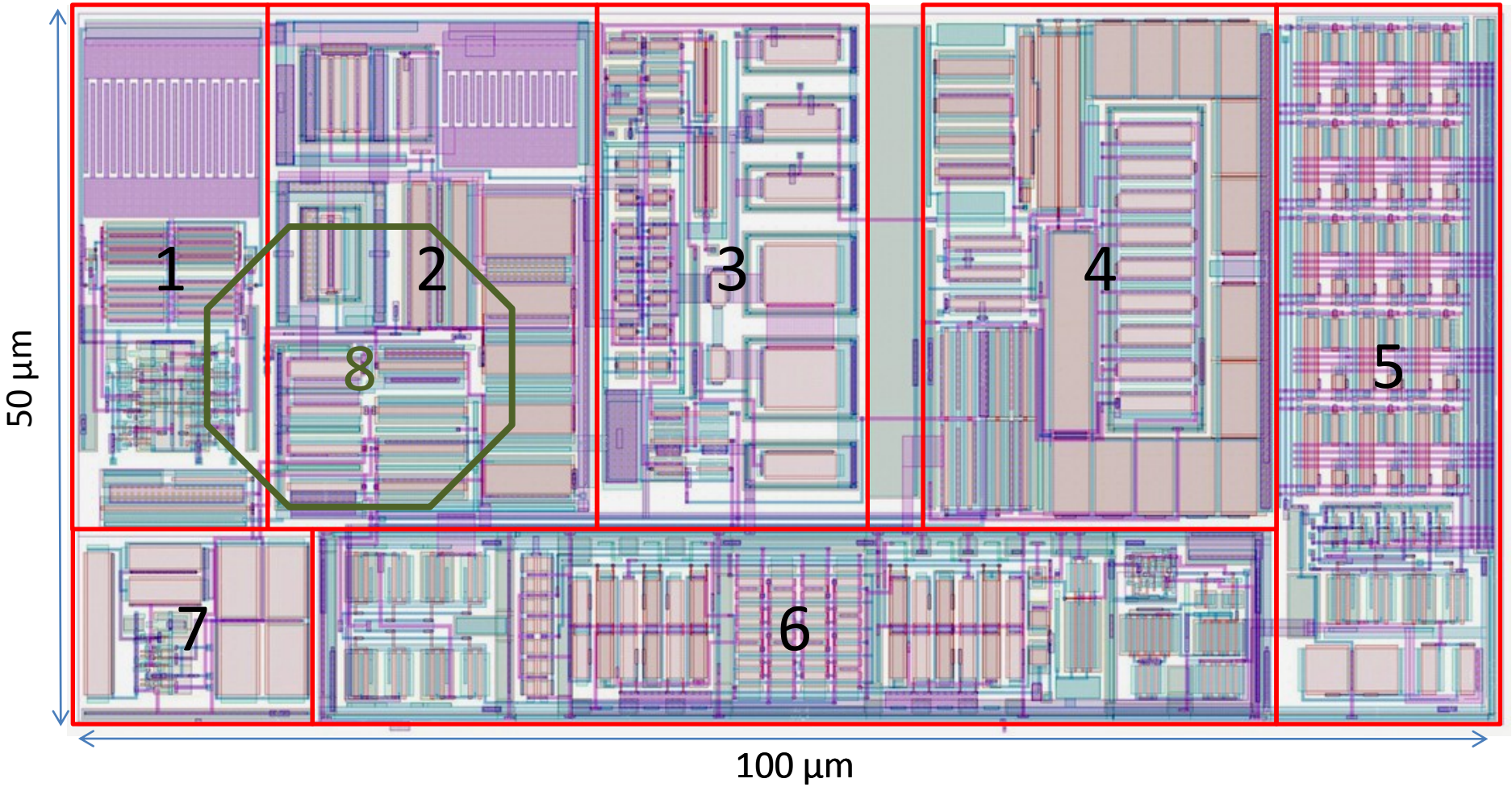
The Analog Front-End generates a pulse whose width is proportional to the injected charge by the sensor.

Analog Cell Upgrades

- Increased gain by 2x (C_f = 24fF -> C_f = 12fF)
- Reduced size of the analog part (70%->50%)
- Cut-off circuit for large signals (>50fC)
- Improved Baseline Holder for a better stability
- Test charge injection circut bug corrected (charge up to 35fC)

$$V_{out,peak} = \frac{Q_{in}}{C_f}$$

Analog Cell Layout

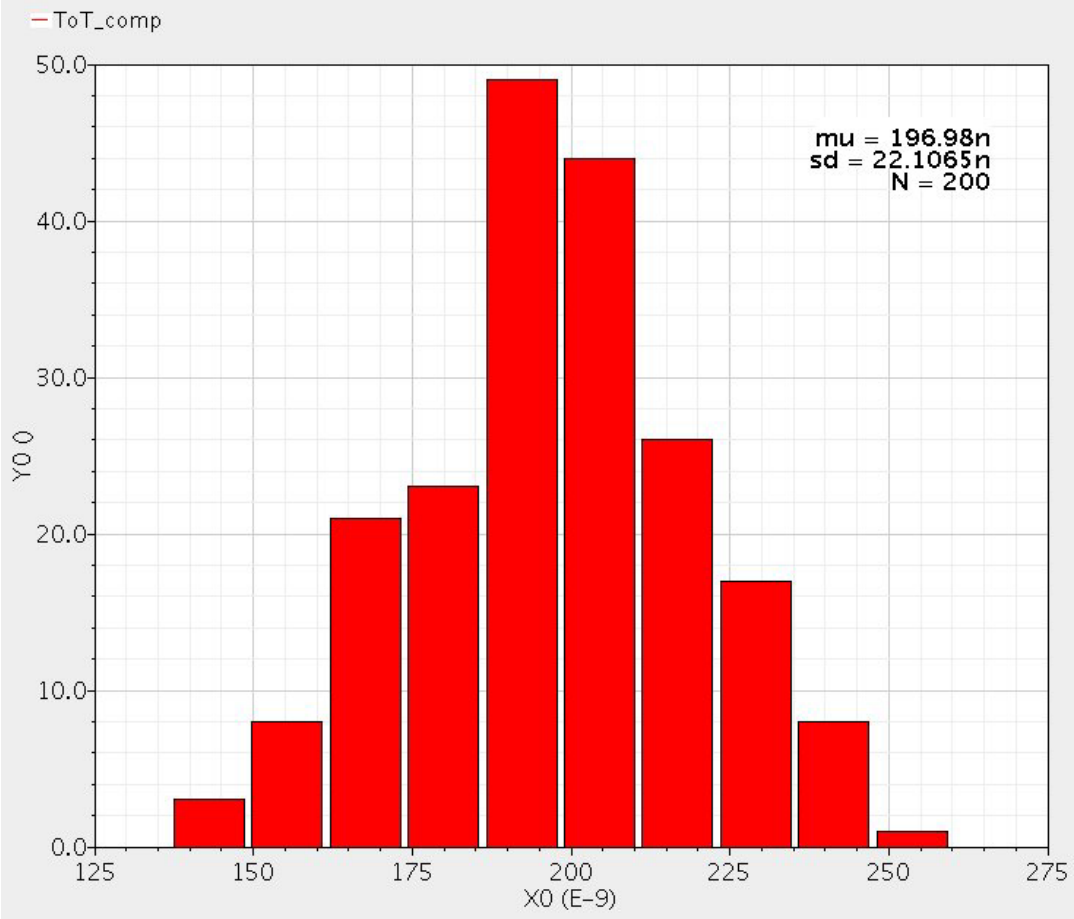


1. Test Pulse Injection
2. Preamplifier
3. Constant Current Feedback
4. Baseline Holder
5. 5 bit DAC for the threshold correction
6. Comparator
7. Large charge cut-off circuit
8. Bump bonding pad

Post Layout - Monte Carlo Simulation

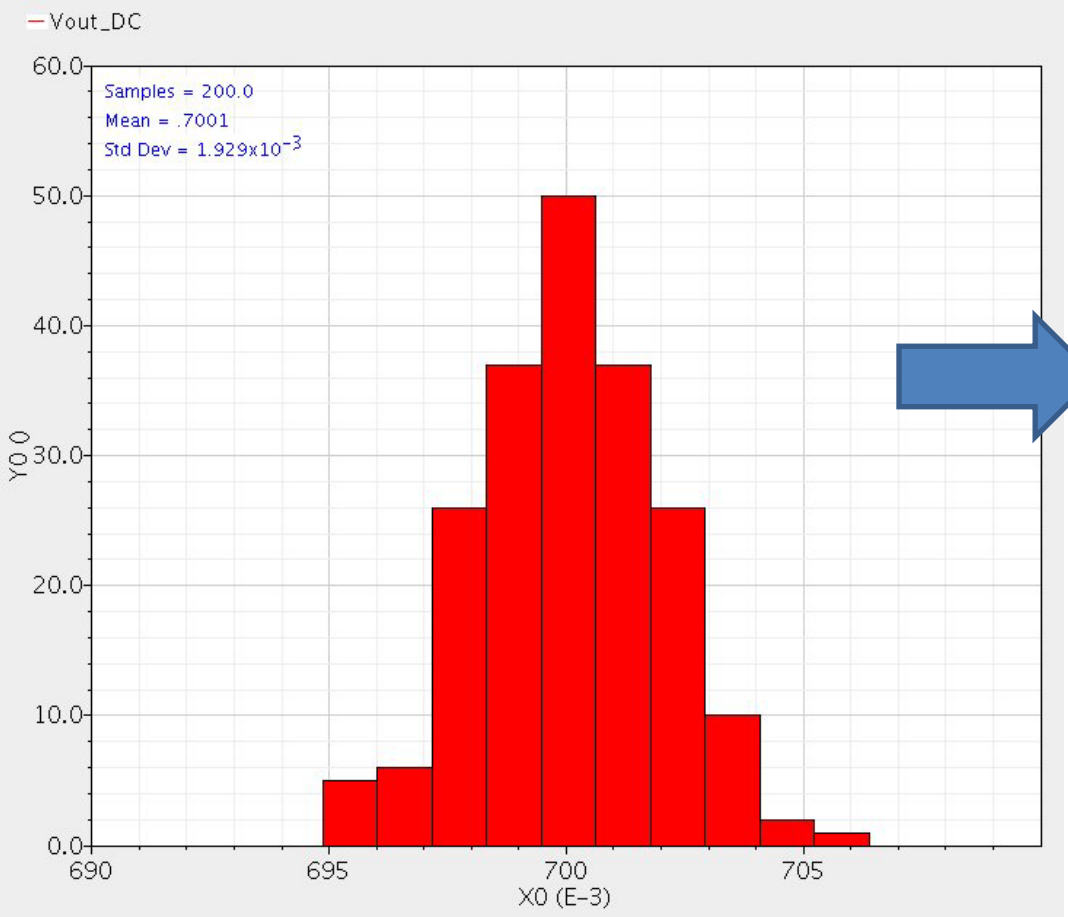
Q_{in} = 1fC

200 Simulations

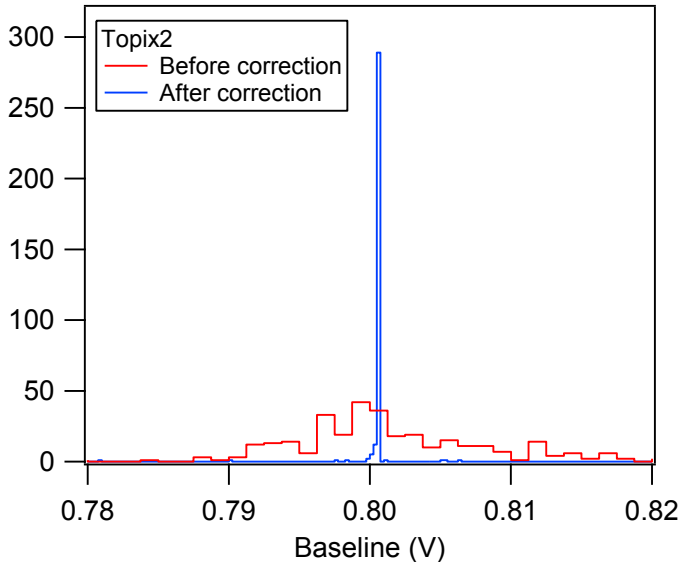


	Min	Max	Mean	Sigma
ToT (ns)	136.9	259.8	197.0	22.1

Baseline dispertion



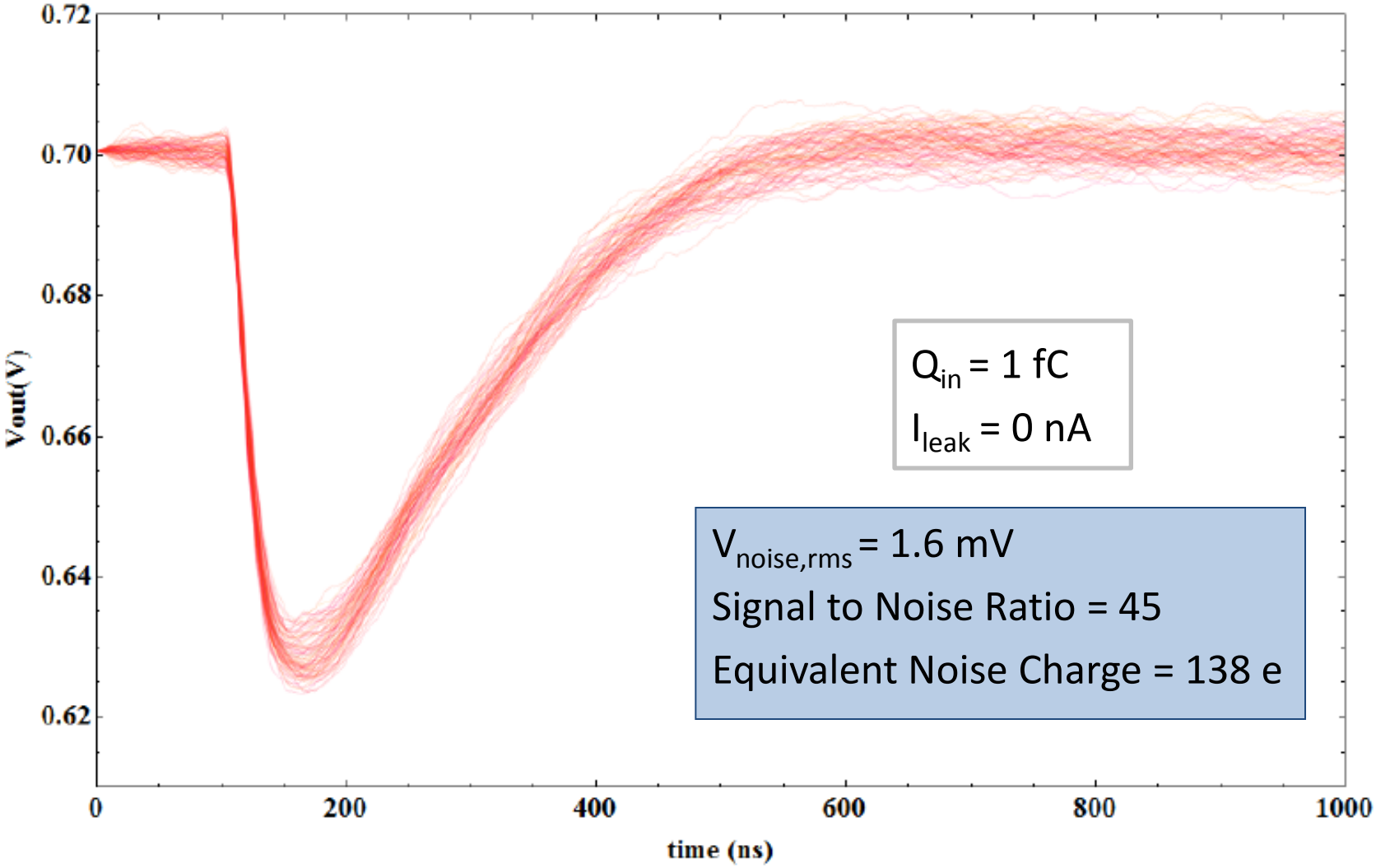
ToPix2 - Threshold tuning on pixel by pixel basis



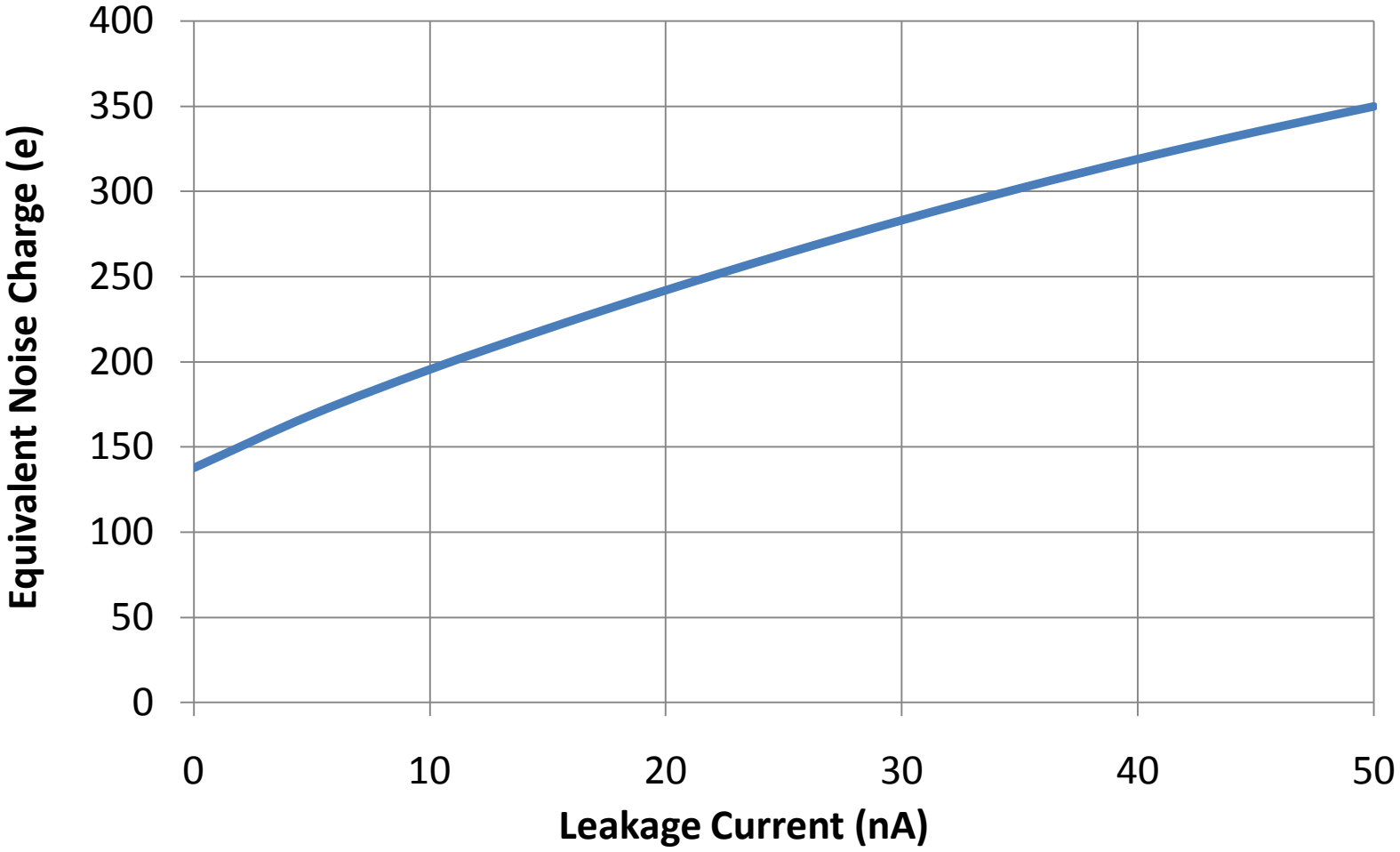
dispertion reduced to 2 mV

	Min	Max	Mean	Sigma
V_{out_DC} (mV)	695.5	707.7	700.1	1.9

Transient Noise Simulation

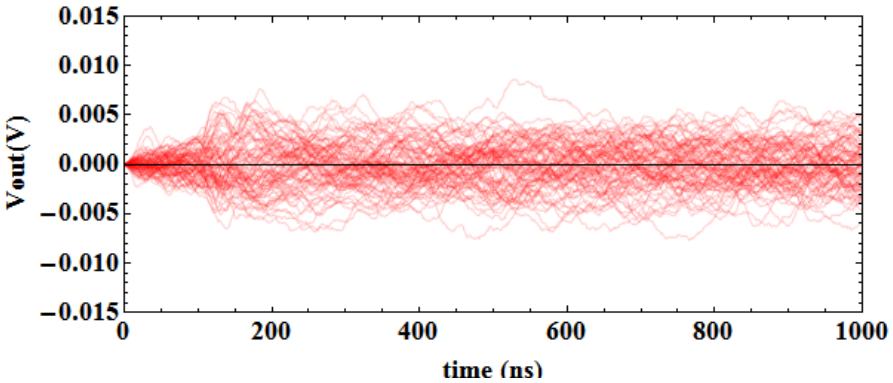


Noise dependence from leakage current

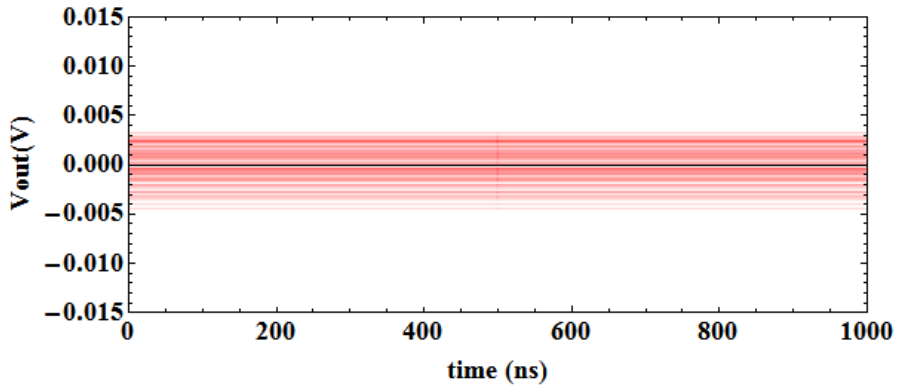


Noise and Baseline

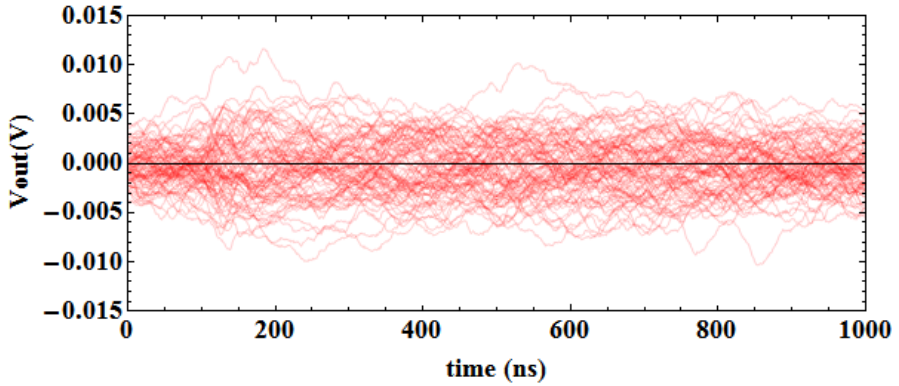
Noise



Channel to channel baseline variation with no compensation

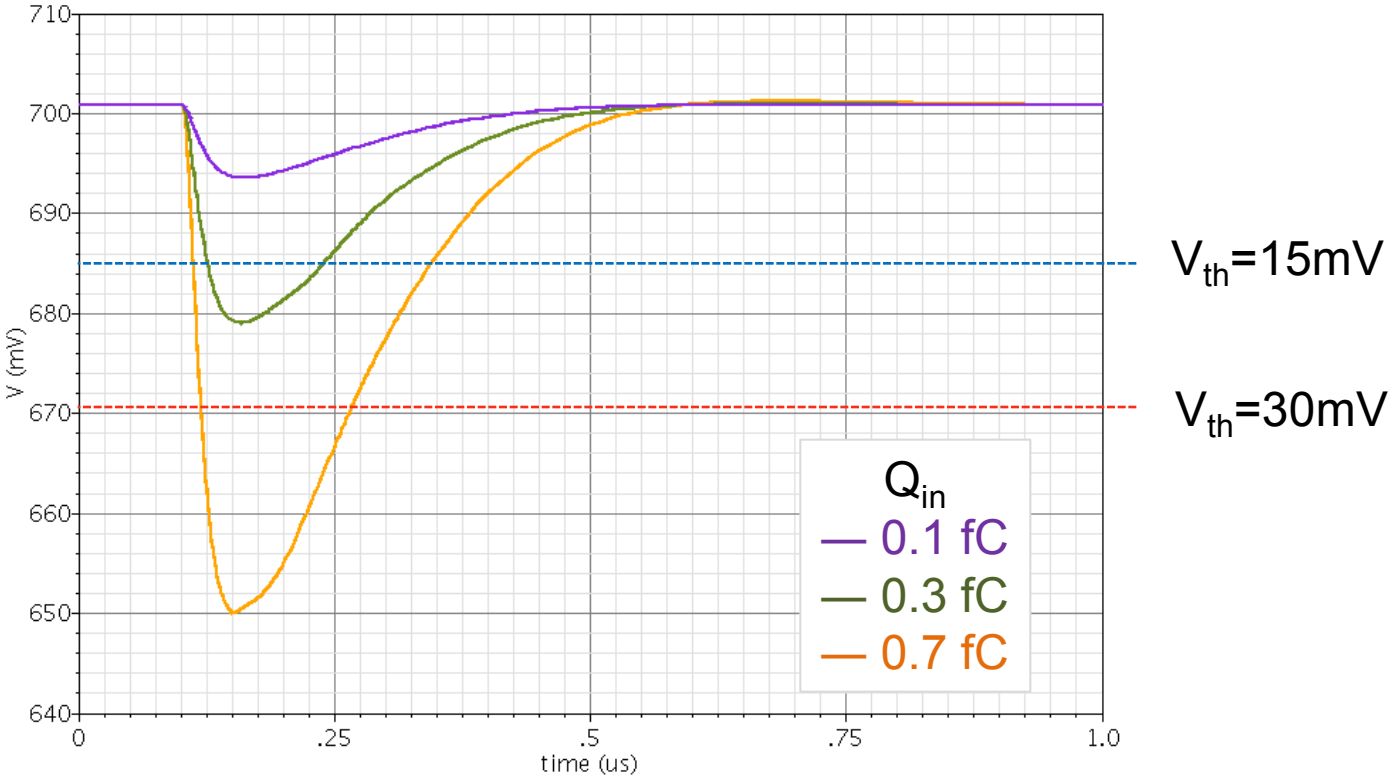


baseline variation
+
noise

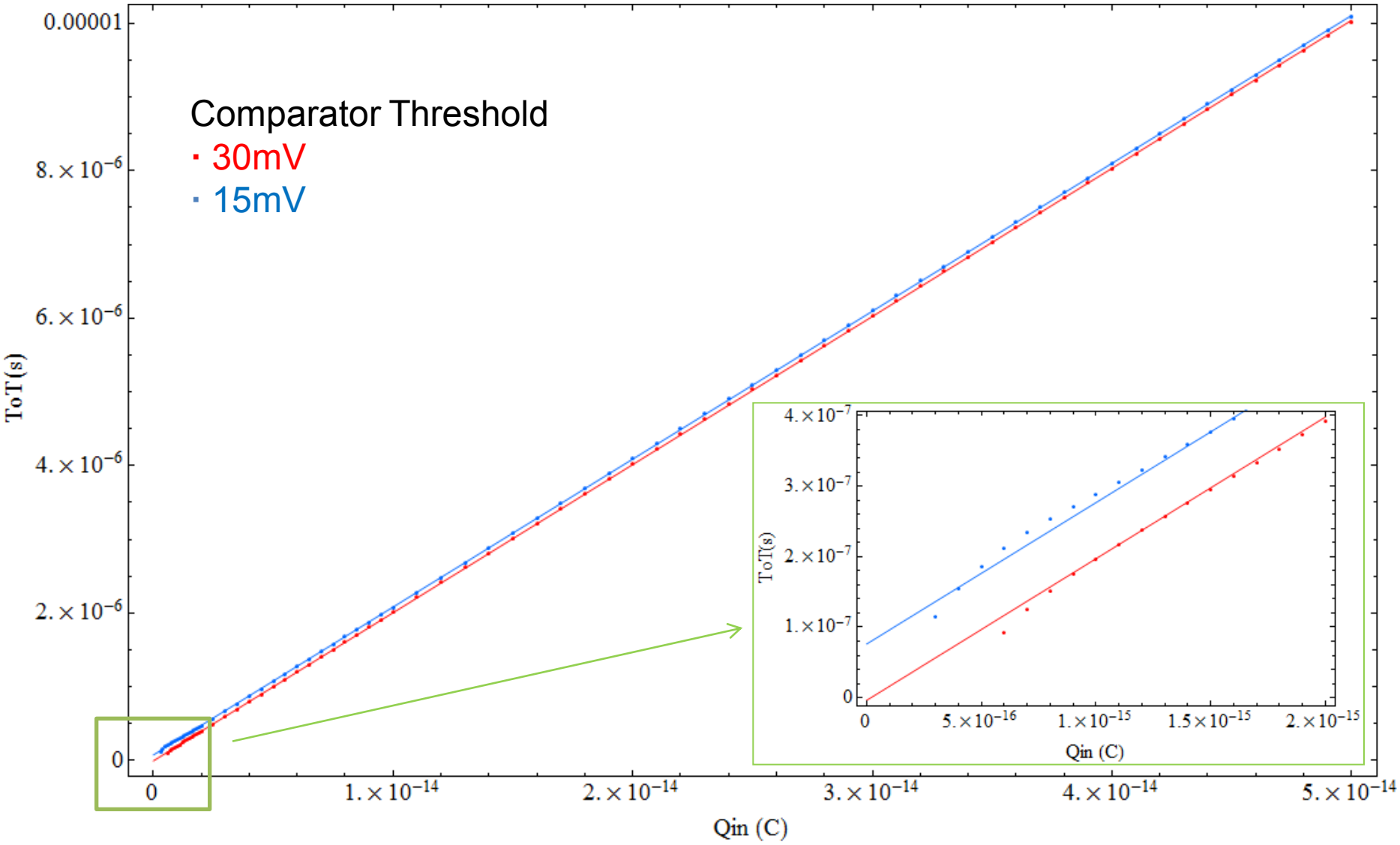


Comparator Threshold

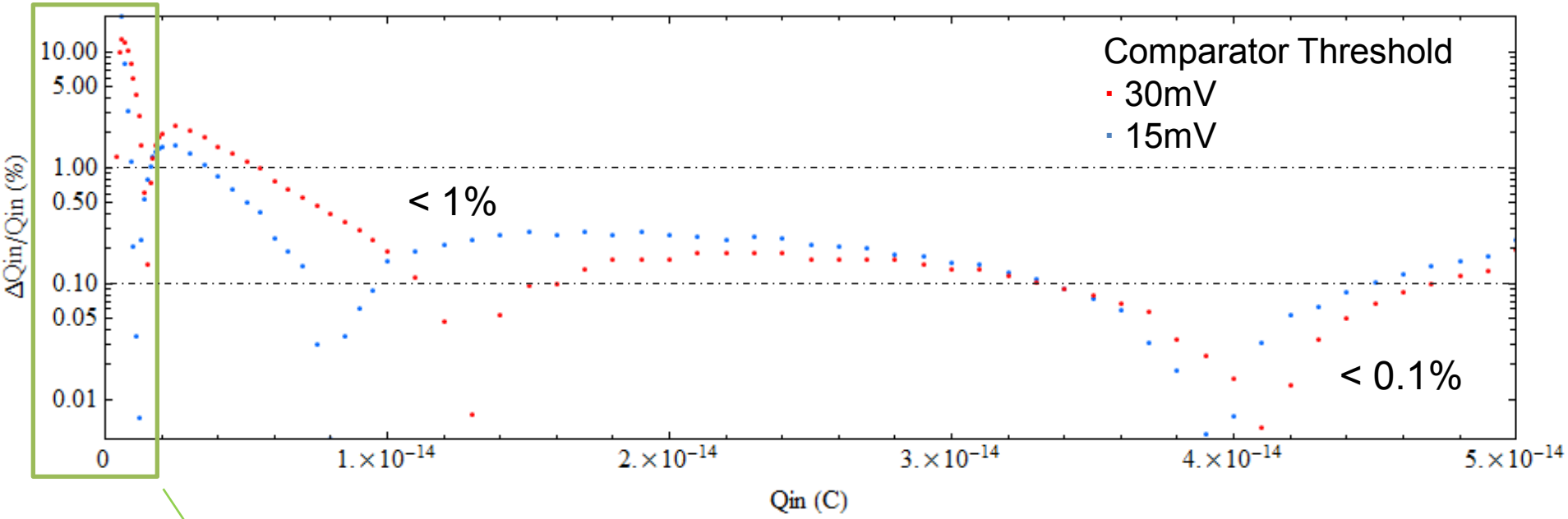
Baseline + Noise < Comparator Threshold

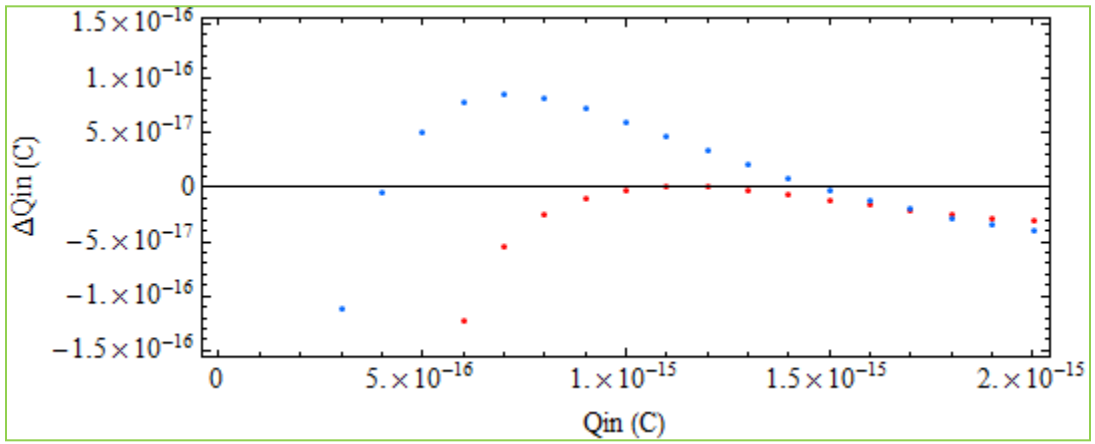


Linearity up to 50 fC



Deviation from linearity

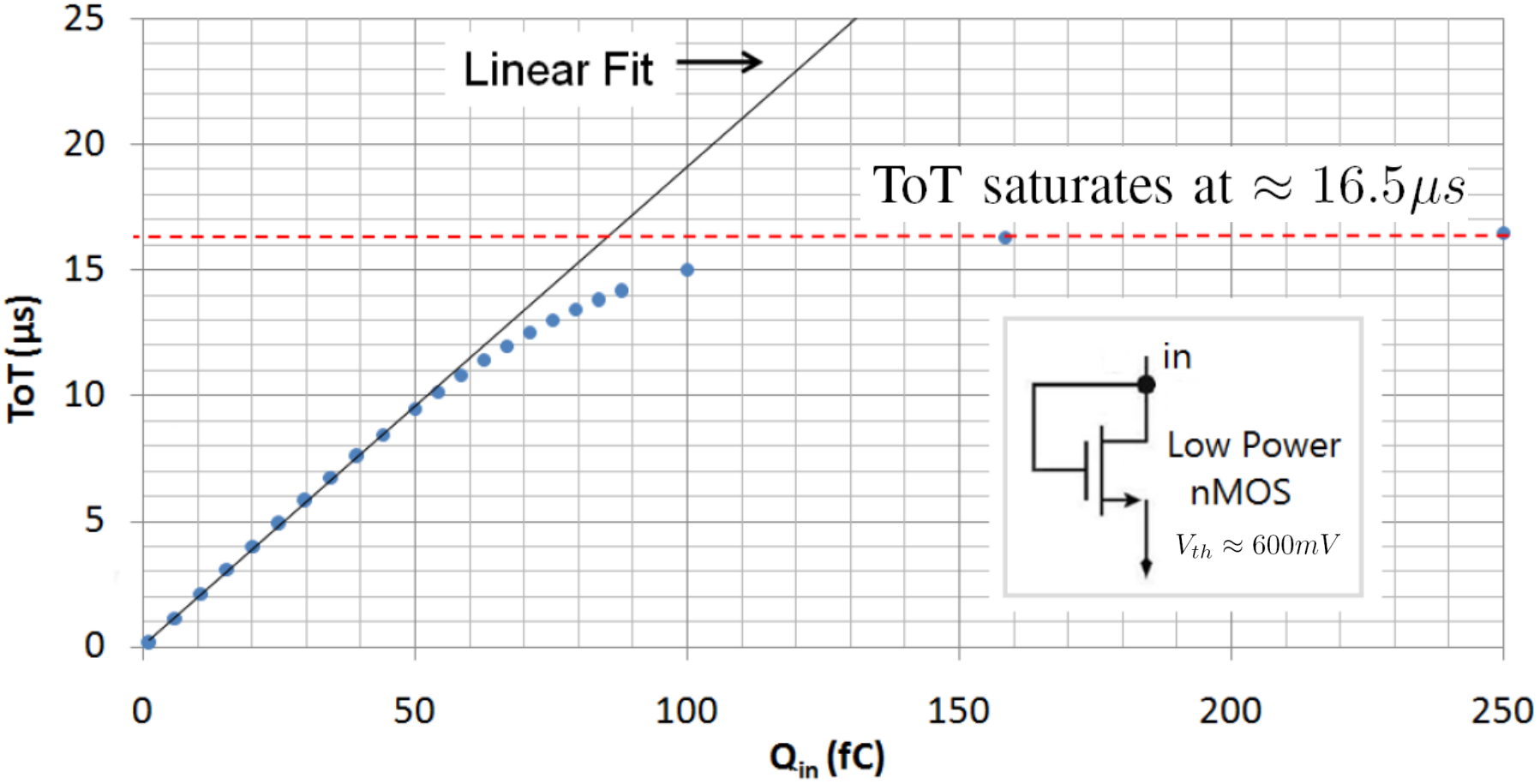




Comparator Threshold	Minimum charge	Error
· 30 mV	0.6 fC	-0.12 fC
· 15 mV	0.3 fC	-0.11 fC

Clipping Circuit

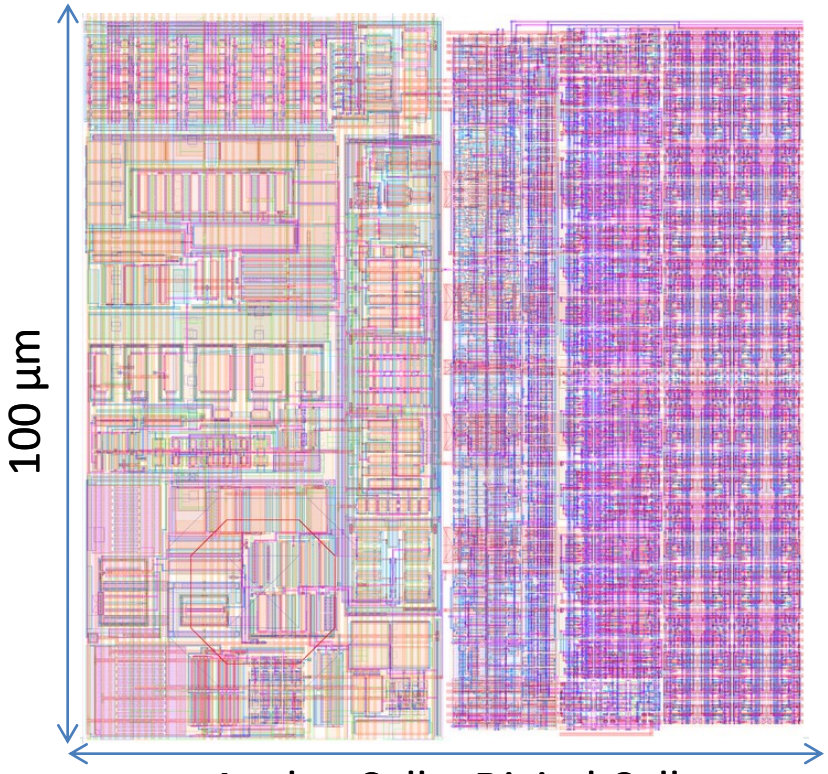
A clipping circuit has been designed in order to protect the front-end when a large charge is presented at the input node, thus avoiding long dead times.



Conclusion

ToPix3 - Prototype chip for the hybrid pixel sensors in CMOS 130nm.

- Based on Time over Threshold readout

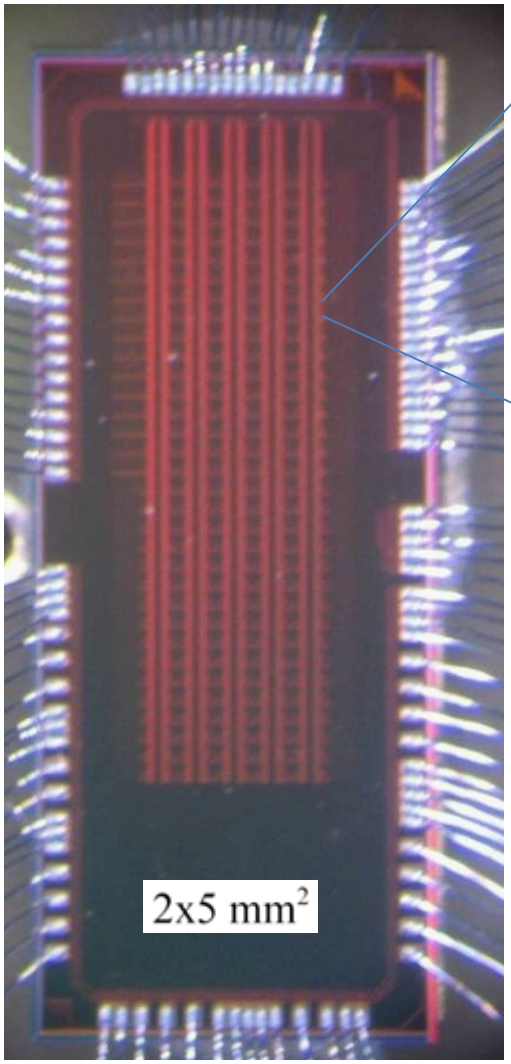


Features

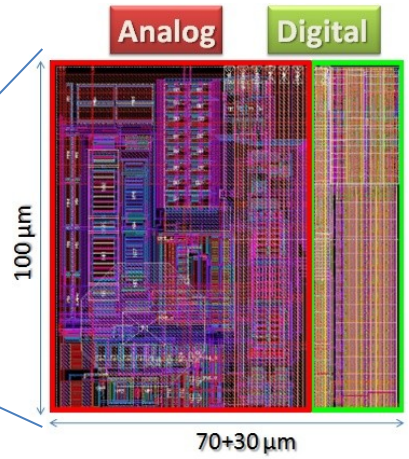
- Increase of the CSA gain (1/12fC) and improvement of the loop stability
- A more compact leakage compensation stage
- Key Features:
  - Analog Cell Size: 50µmx100µm
  - Power Consumption: 15µW/cell
  - Equivalent Noise Charge: <200e^-

BACKUP SLIDES

First Prototype

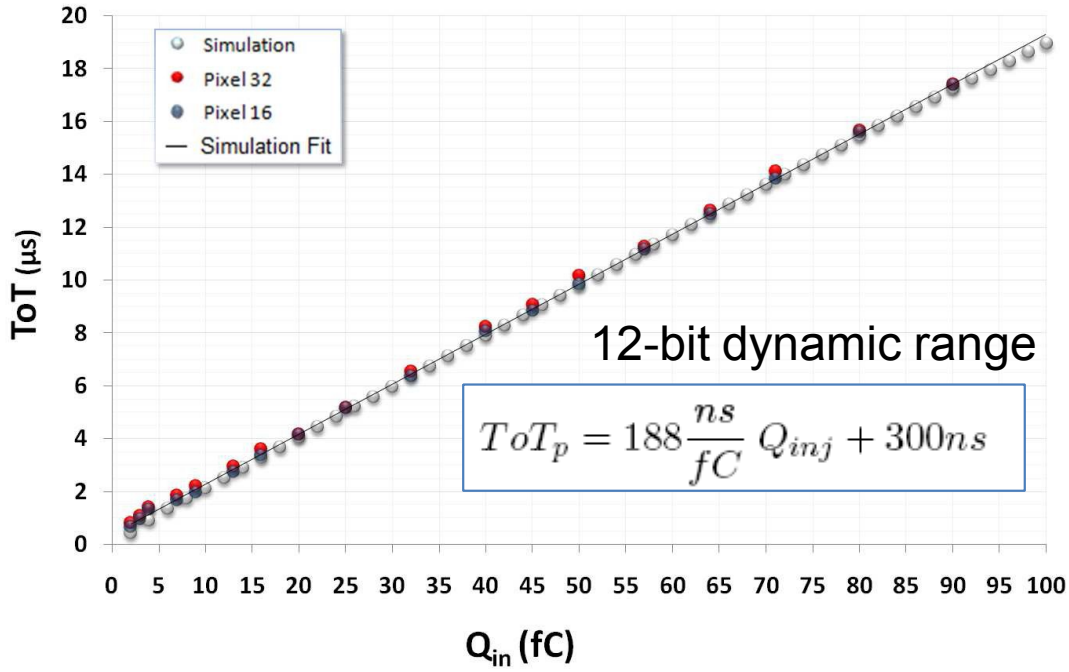


Reduced scale prototype chip (320 cells)

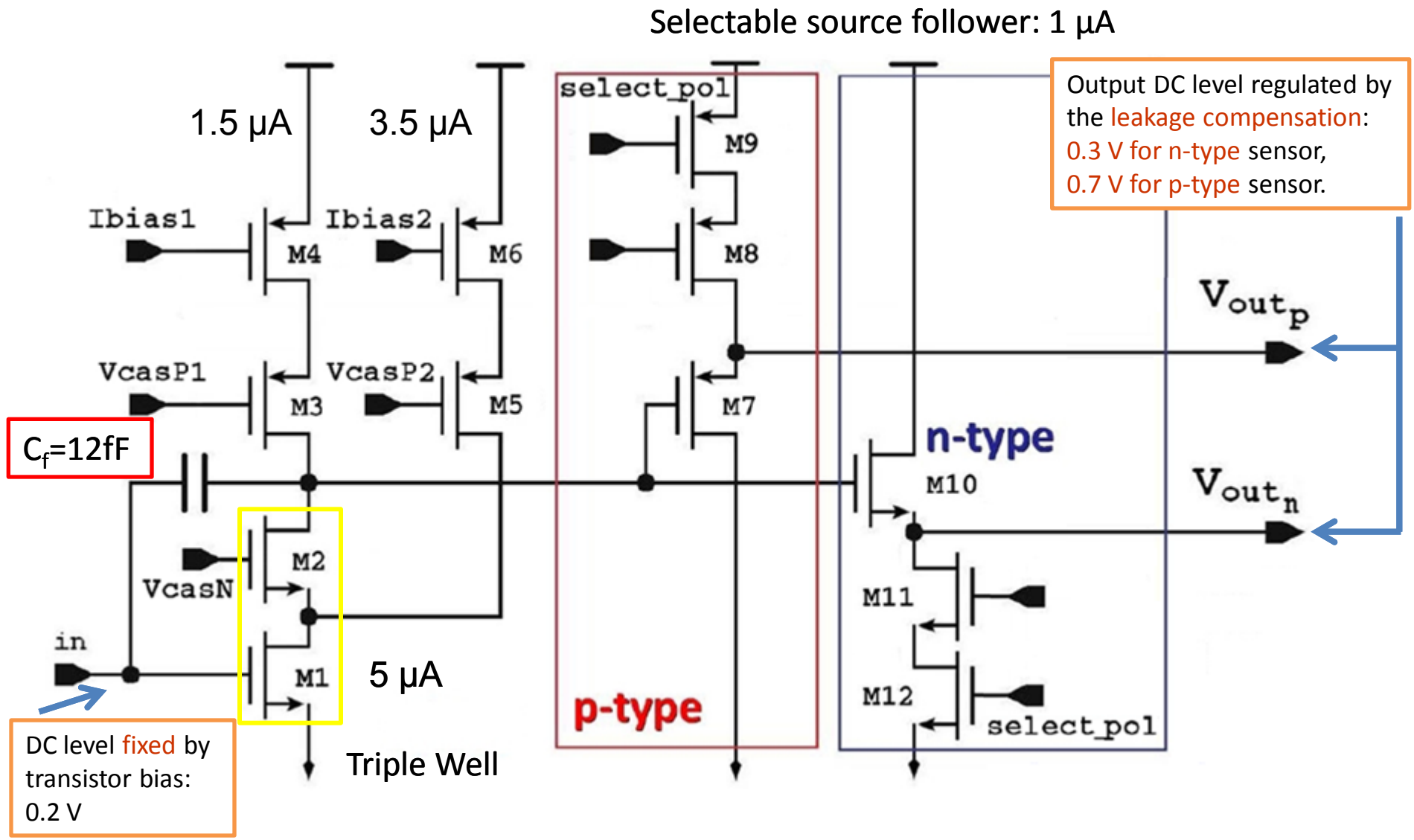


Each cell incorporates the analog and digital electronics necessary to amplify the detector signal and to digitize the charge information.

P-Type sensors ToT Linearity

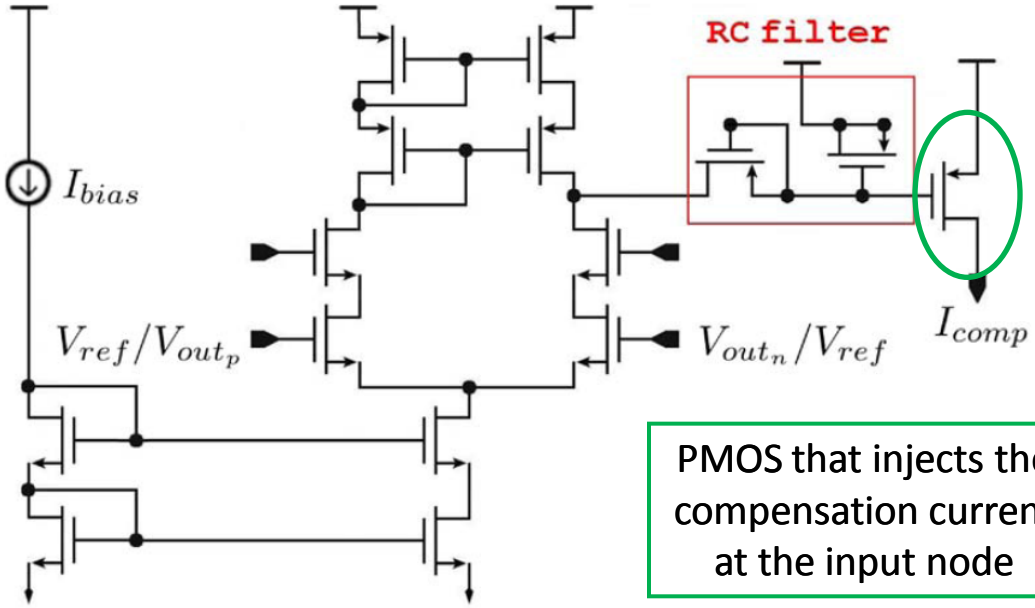


CSA Schematic



Baseline Holder

Compact Low-Frequency Feedback Filter



PMOS that injects the compensation current at the input node

ToT signals can be very long (< 20us)

In order to preserve the signal a very low cutoff frequency (≈10Hz) is required.

The leakage current depends on the Total Ionizing Dose. It may be up to 50nA.

$$f_p = \frac{1}{2\pi R_0 C_0} \approx 10Hz \Rightarrow R_0 C_0 \approx 1s \qquad C_0 \approx 1pF \Rightarrow R_0 \approx 10^{12}\Omega$$

In CMOS technology in an area of few hundreds of µm² it is possible to implement a capacitor of few pF

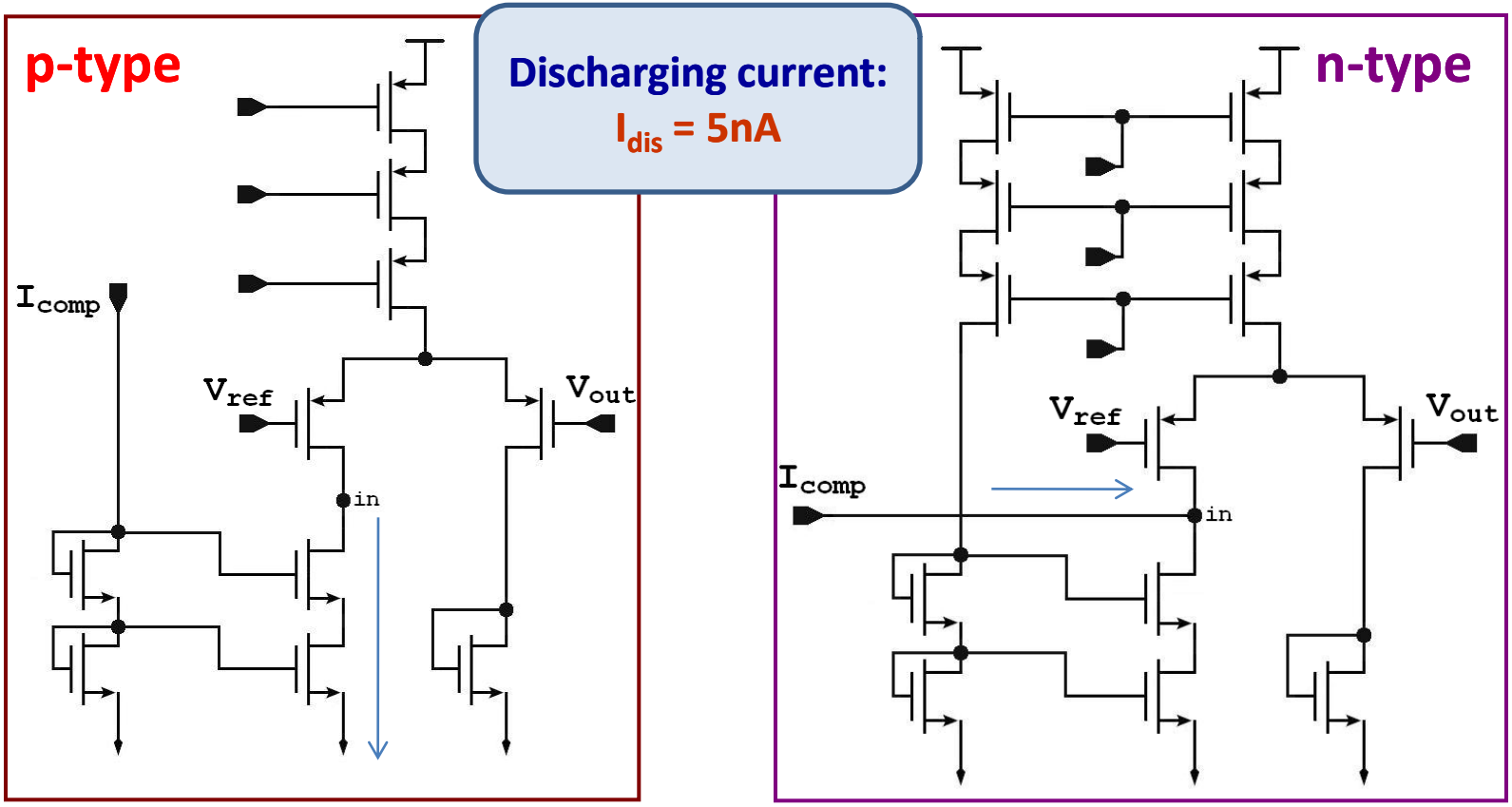
R: Gate-Source shorted MOS

C: Source – Drain shorted MOS

Feedback Circuit

It keeps the output at the reference voltage, discharging the charge deposited on the input node.

This stage provides also the injection of the leakage compensation current at the input node.



Compensation current injected trough current mirror

Compensation current injected directly