



IPHC-Strasbourg Group in CREMLINplus

M.Winter / ex IPHC-Strasbourg, 4 Septembre 2020

- **IPHC \equiv one out of \sim 20 subatomic physics laboratories belonging to IN2P3/CNRS**
- **IPHC-Group: activity driven by future electron-positron collider experiments (e.g. ILC/Japan)**
- **IPHC-Group track: pioneered CMOS Pixel Sensors (CPS) for subatomic physics**

IPHC-Strasbourg Group in CREMLINplus

● PERSONNEL CONCERNED:

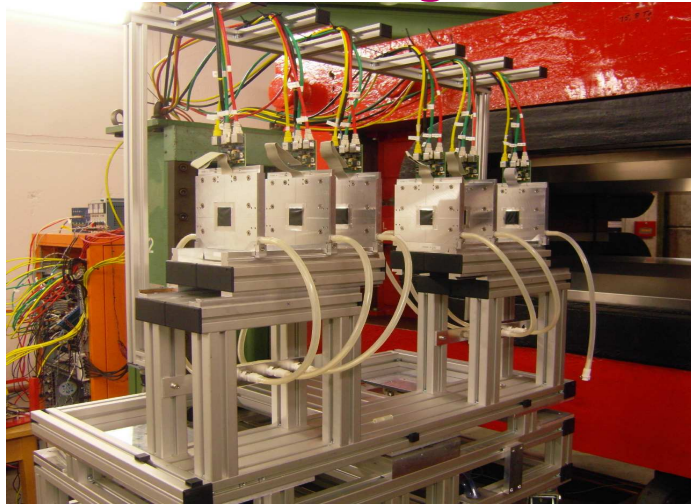
- **Particle Physicists:** 3 staff physicists, 1 staff instrumentation physicist, 2 post-docs
- **ASIC designers (6 PhD):** 10 staff engineers, 2 PhD students
- **Electronicians :** 4 staff engineers
- **Technical support from IPhC services:** micro-technics & mechanics workshops

● MAIN ACTIVITIES:

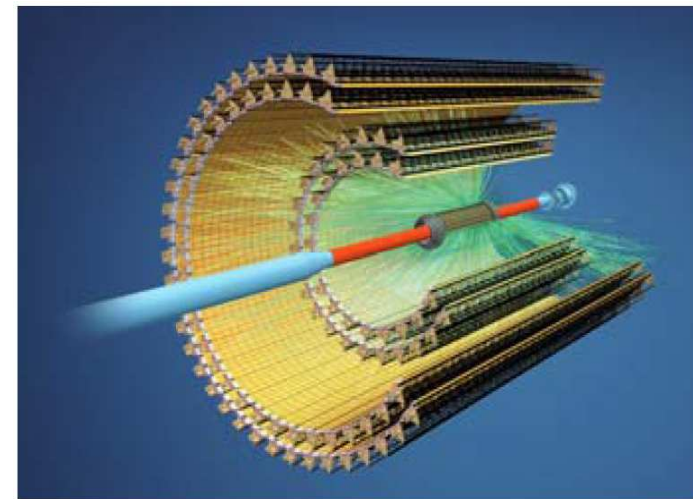
- **Activities mainly instrumental, targetting future e+e- colliders:** (supported by phys. studies)
 - ↳ R&D on highly granular and thin CMOS pixel sensors (+ 2-sided ladders):
design, electronic tests, characterisation, detection performance evaluation
 - ↳ full prototyping until final production
- **Domains of application: predominantly subatomic physics and some spin-off domains**
 - ↳ exploiting synergy between tracking devices for heavy-ion and lepton-collider expts

Emblematic Devices Equipped with CPS

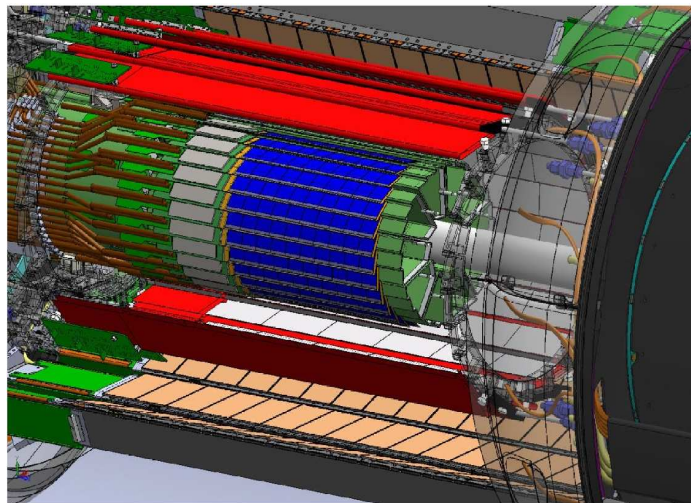
EUDET BT: running since 2009



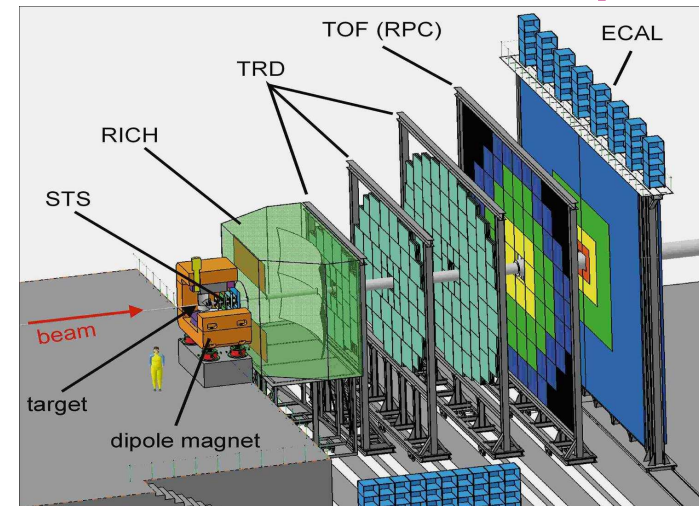
ALICE-ITS2: in construction



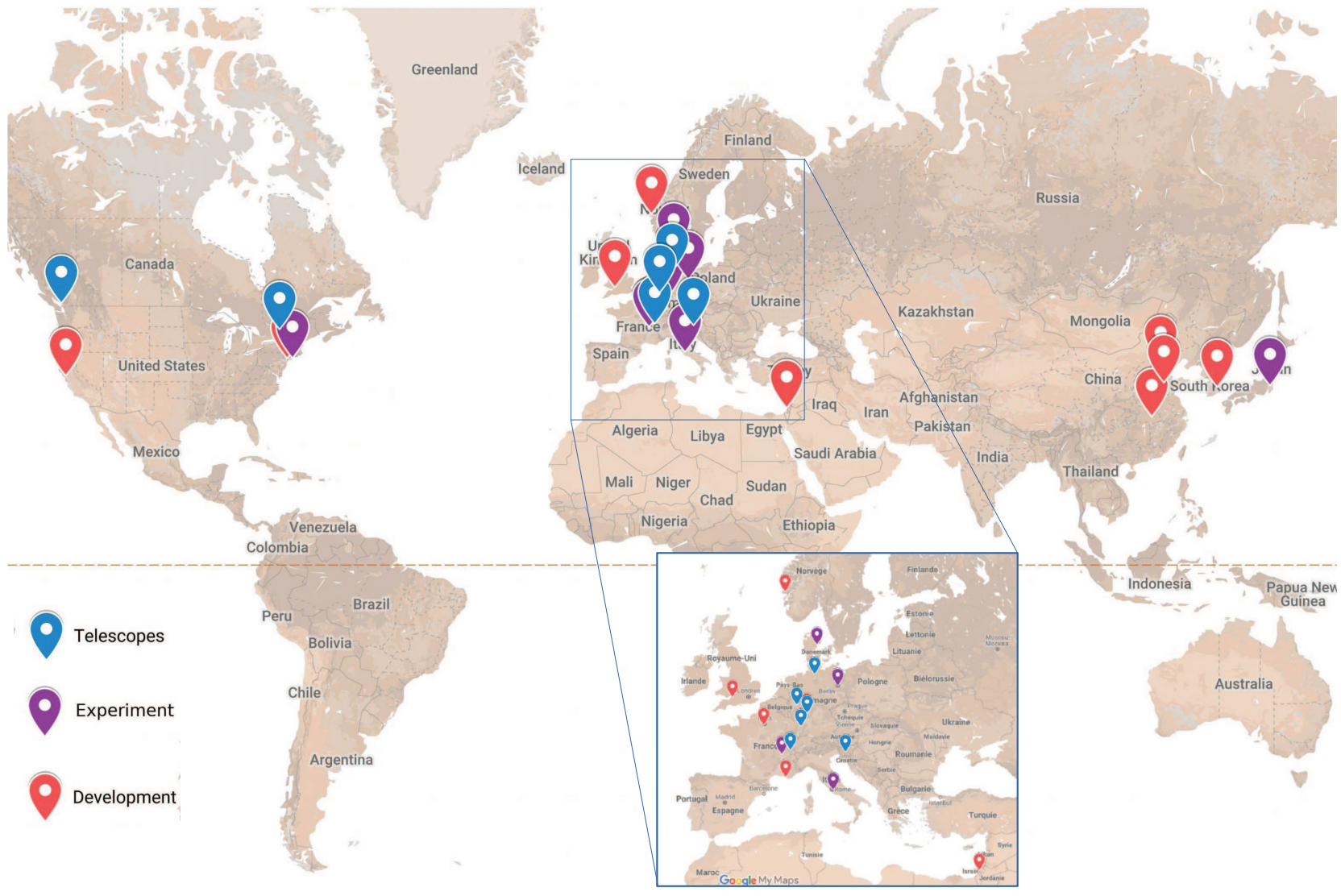
STAR-PXL: Physics 2014 → 2016



CBM-MVD: under development



Location of Devices based on CPS from PICSEL



Activities Foreseen within CREMLINplus

- **Development of the CMOS Pixel Sensor (MIMOSIS) for the CBM-MVD at FAIR:**
 - MIMOSIS-1 expected to be available within consortium \lesssim Q4/'21
 - MIMOSIS-2 expected to be available within consortium \lesssim Q4/'22 (?)
- **Development of CPS for an expt at the International Linear Collider (ILC):**
 - Main objective: vertex detector and inner trackers composed of double-sided layers
 - R&D goals: squeeze time resol. & power consumption while keeping achieved spatial resol. (few μm)
 - Starting point: improve time resolution of MIMOSIS
- **Explore newly available products of CMOS industry:**
 - Exploit stitching possibilities (multireticle sensors) within ALICE-ITS3 project (tbc)
 - Develop CPS in 65 nm CMOS technology within CERN-ALICE R&D project
- **Develop ultra-light double-sided ladder equipped with MIMOSIS:**
 - Follow-up of PLUME ladder concept (2x6 MIMOSIS-26 sensors)
 - ????????????????
- **Others:** CPS in CMOS-Sol, 2-tier CPS, ...

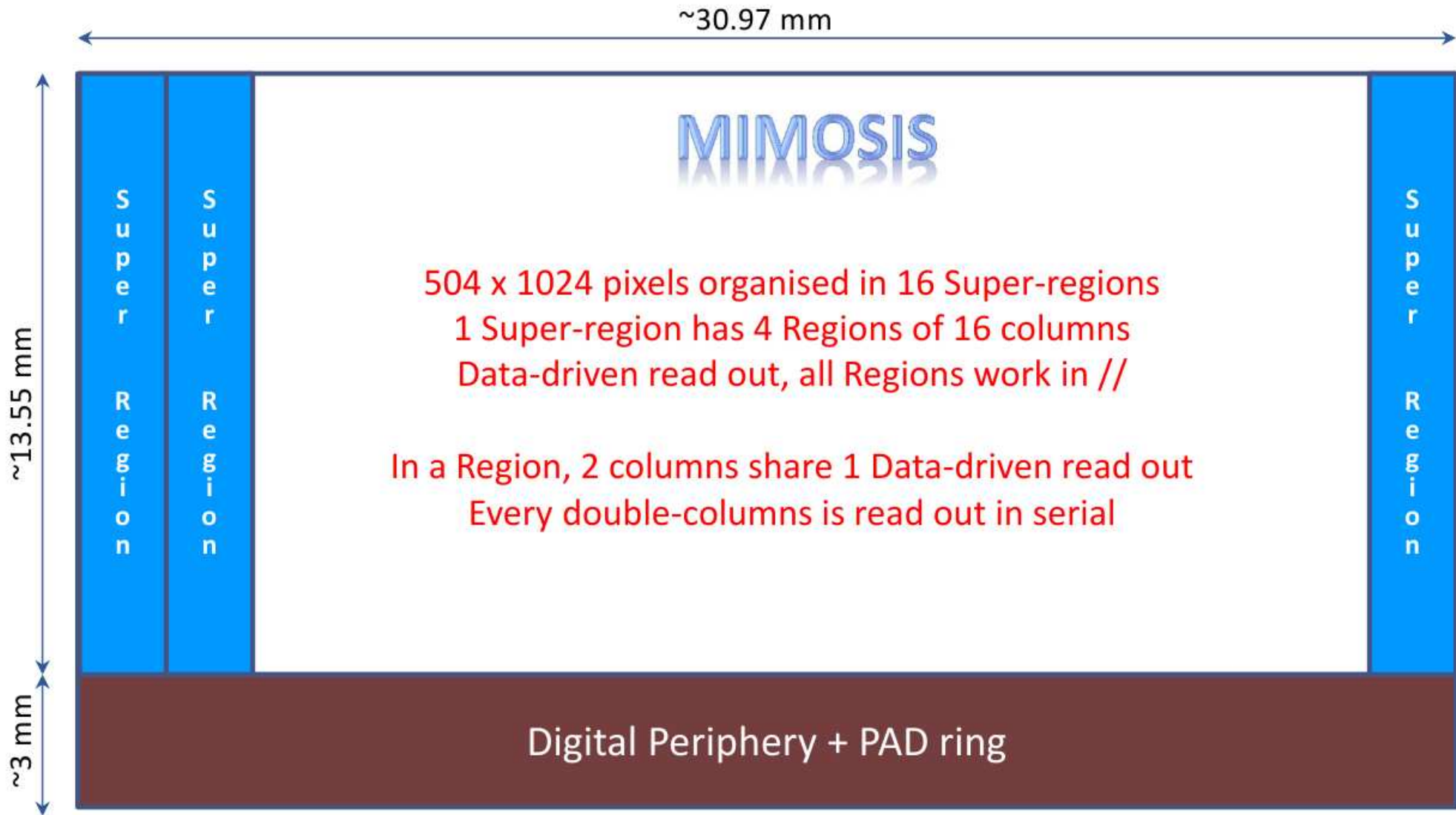
CPS Design Required for the MVD: MIMOSIS Sensor

- **MIMOSIS derived from ALPIDE pixel array read-out architecture (ITS, MFT)**
- **Required radiation tolerance significantly higher than ALPIDE**
($\gtrsim 10$ times higher locally)
- **Required data throughput ~ 10 times higher than ALPIDE**
(hit density actually up to $\sim 10^2$ times higher locally)

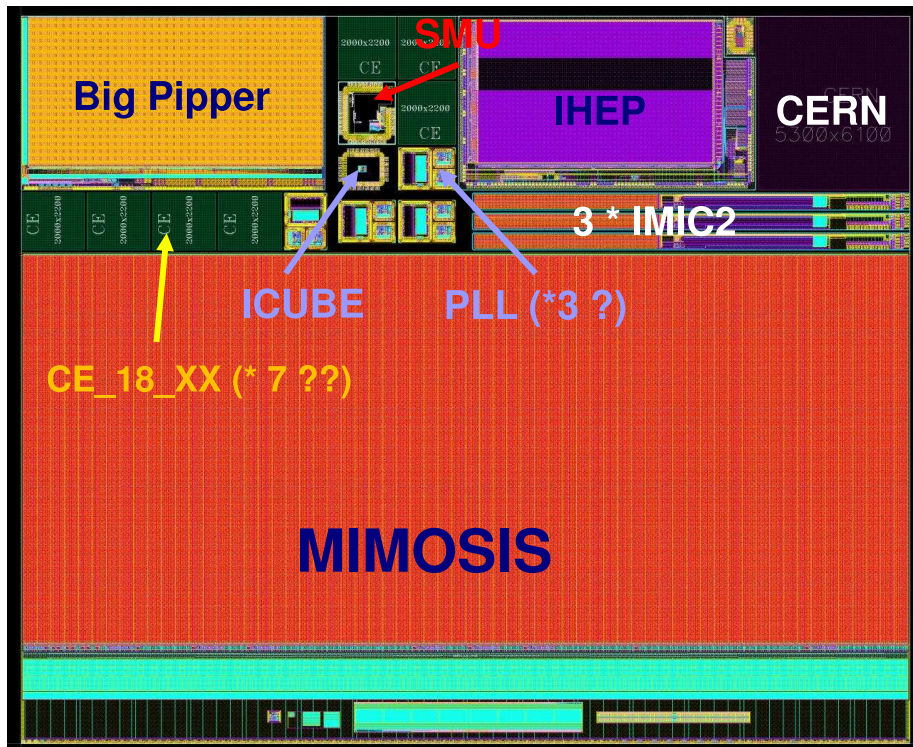
	ITS (IB)	CBM (1 st station)
Radiation Load TID	~ 270 krad	3 Mrad @ -20°C, 1 Mrad @ +30°C
Radiation Load NIEL	$\sim 1,7 \times 10^{12}$ 1MeV n_{eq}/cm^2	3×10^{13} n_{eq}/cm^2 @ -20°C, 1×10^{13} n_{eq}/cm^2 @ +30°C
Peak hit rate	$\sim 1,25 \times 10^6/cm^2/s \rightarrow 1,25 \times 10^4/mm^2/s$	$7 \times 10^5/mm^2/s$ (x 56 times than ITS)
Trigger	yes	no
Heavy Ion Effect		

- **Fully revisited digital circuitry (data sparsification & transfer logic)**

MIMOSIS Overview



Mimosis Reticle status (19 Sept 2019)



- Dimensions :
X = 31 100.16 μm
Y = 25 500 μm
- Around 25 to 27 reticle / wafer
- For all chips, a first version have been provided by the collaboration
- Need to adjust the dicing plan

19/09/2019

gregory.bertolone@iphc.cnrs.fr

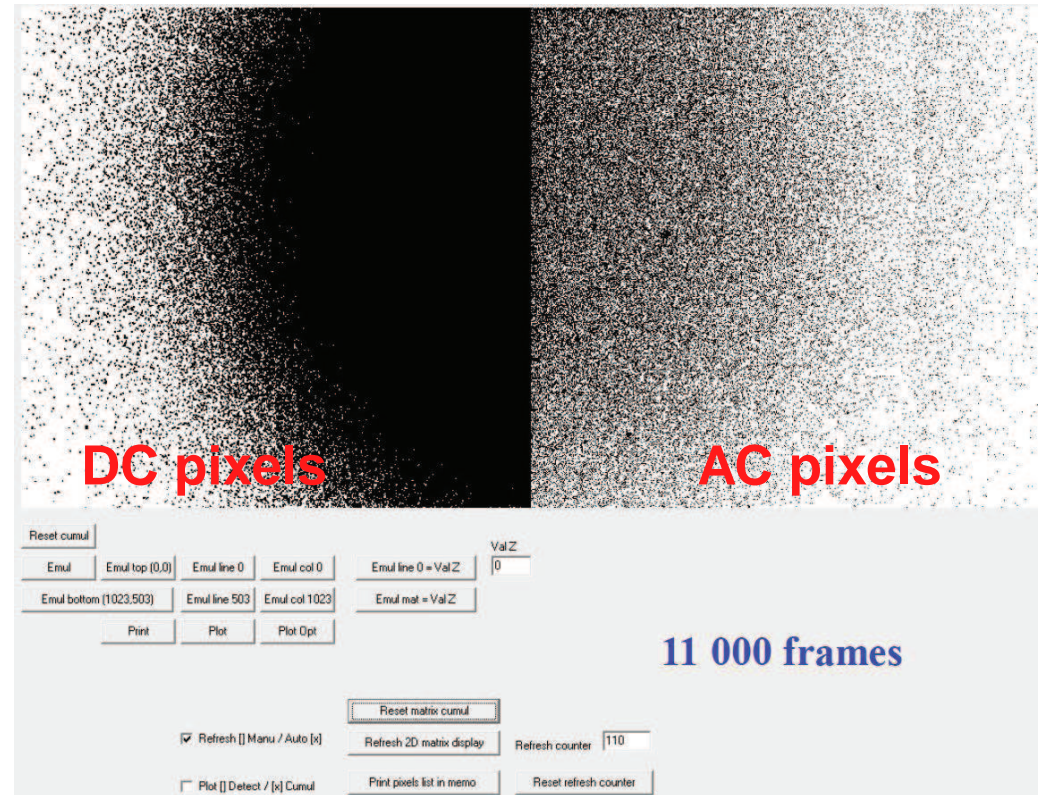
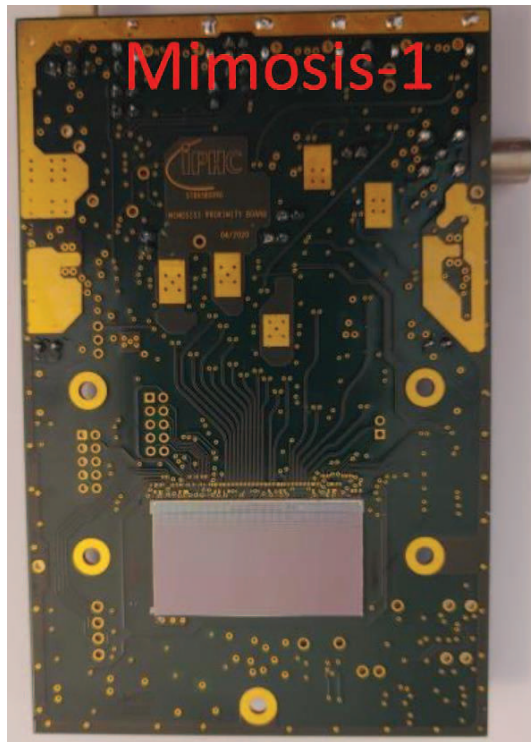
6 variants of epi-layer to achieve $T_{coll}^Q < 1 \text{ ns}$

Partners of the submission besides IKF-GSI-IPHC:

- IHEP-Beijing: CEPC
- CERN: ATTRACT & LHC
- IMNC-Orsay: β imaging
- SMU-TX: PLL/MIMOSIS
- CPPM-Marseille: β imaging
- ICUBE-Strasbourg (CNRS): ultra-fast imaging

Back from foundry and diced in July 2020

First Functionnal Tests of MIMOSIS-1



- Reacts to I2C Slow Control commands, gets configured as expected
- Data flow properly acquired by DAQ and decoded (header, data information, trailer)
- Various hit pixel patterns generated, which get all faithfully encoded and read
- The whole pixel array reacts appropriately to ^{55}Fe source illumination

Exploration of TJsc 65 nm CMOS Technology

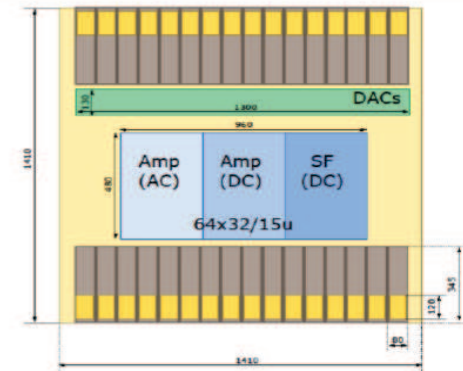
- Newly accessible 65 nm imaging CMOS technology via ALICE-ITS coll. and CERN-EP
- Submission for fabrication of exploratory structures & chips foreseen at "end of Septembre" (MLR-1)
- IPHC: small pixel arrays ($15\mu m$, $25\mu m$, possibly $20\mu m$, pitch; DC & AC); in-pixel VFE variants; analog DACs contributions to O(100) ps in-pixel amplification circuitry (AC/DC input node)

CE65 VARIANTS



➤ Variant A

- pixel pitch: 15um
- matrix size: 64x32
- 3 sub-matrices: Amp (AC)/ Amp (DC)/SF (DC)
- provides space for DACs (fully separated from matrix)



➤ Variant B

- pixel pitch: 25um
- matrix size: 32x32
- 2 sub-matrices: Amp (AC)/SF (DC)

