CREMLIN PLUS

Connecting Russian and European Measures
for Large-scale Research Infrastructures

Task 2.2 – WUT contribution

Developments for the data acquisition chain, for data preprocessing and computing

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This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No. 871072

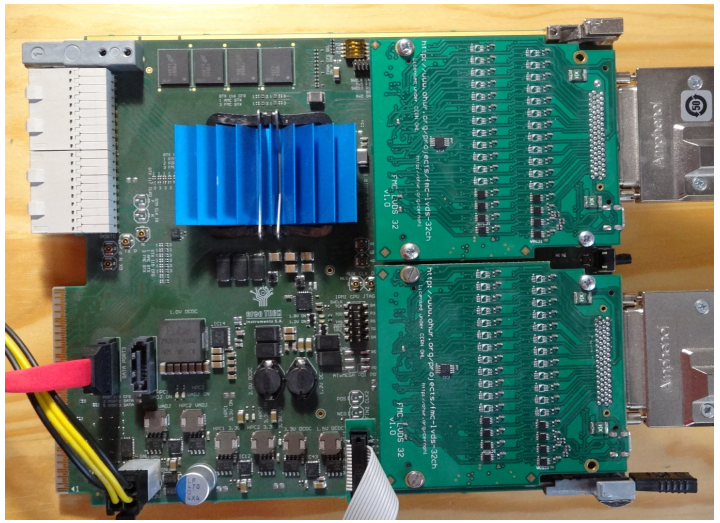
What WUT will contribute

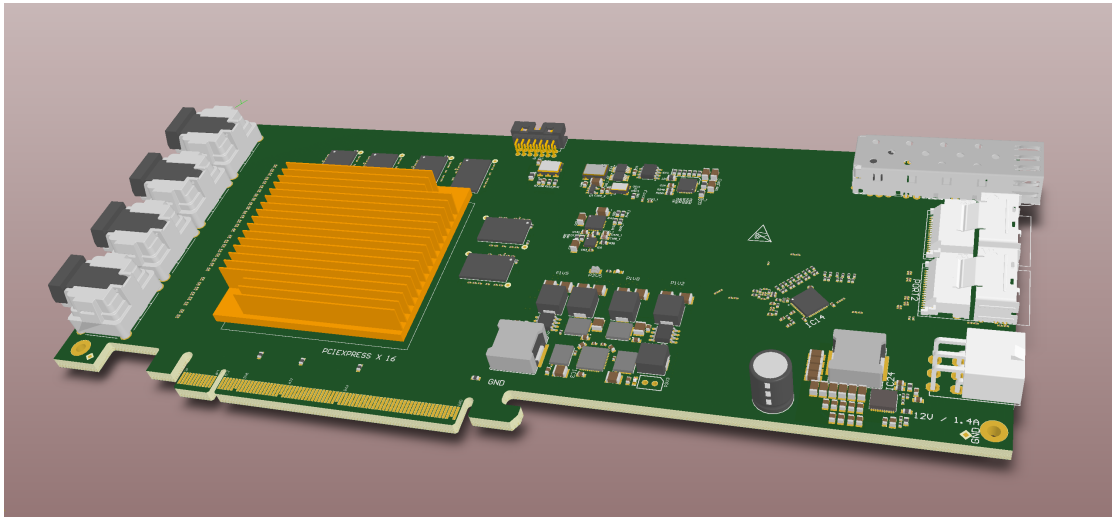
- Allocated resources: 2xFTE
  - Hiring process completed on 15.05.2015 – 2 persons employed for ¾ FTE (Marek Guminski – with 5 years experience in cooperation with GSI, Piotr Miedzik – with previous experience in working at GSI)
  - Additional support from staff not hired for the project (ca. 3 * ¼ FTE)
- Main involvement:
  - FPGA FW development + low level supporting software development
  - Testing of the HW with developped FW+SW
  - Consulting regarding the readout architecture
- Additional involvement
  - Consulting regarding the HW design
  - Consulting regarding the SW implementation

Background

- Our team is involved in preparation of solutions for CBM for a long time
  - First contacts in 2008
  - In 2010 first cores developed with CBM in mind (e.g. heap sorting in FPGA – published in 2011)
  - Since 2012 we are the members of collaboration
  - Since 2014 the serious development of FW (initially also HW) for CBM started.

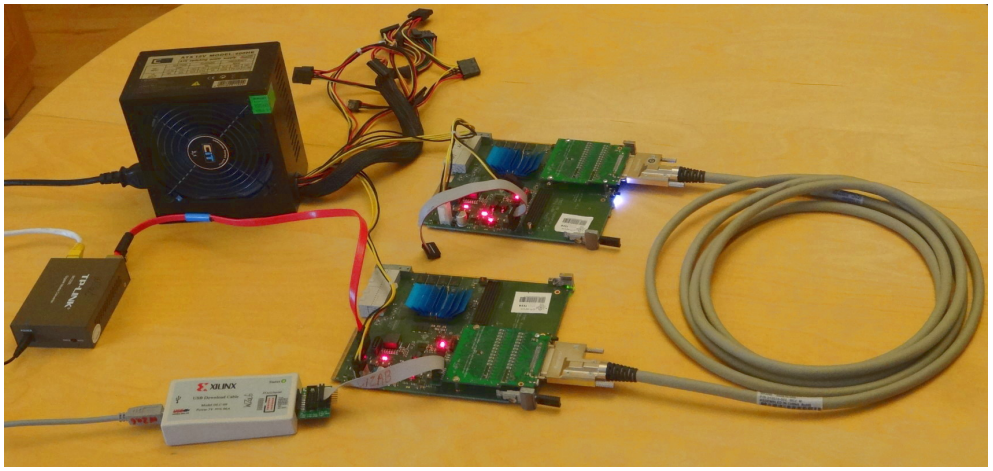
HW development





- The AFCK board used for DPB prototyping was developed at WUT and manufactured by Creotech
- Also the proposal of an enhanced version to be used as CRI was created in 2017, but was dropped in favor of using an already existing and tested solution

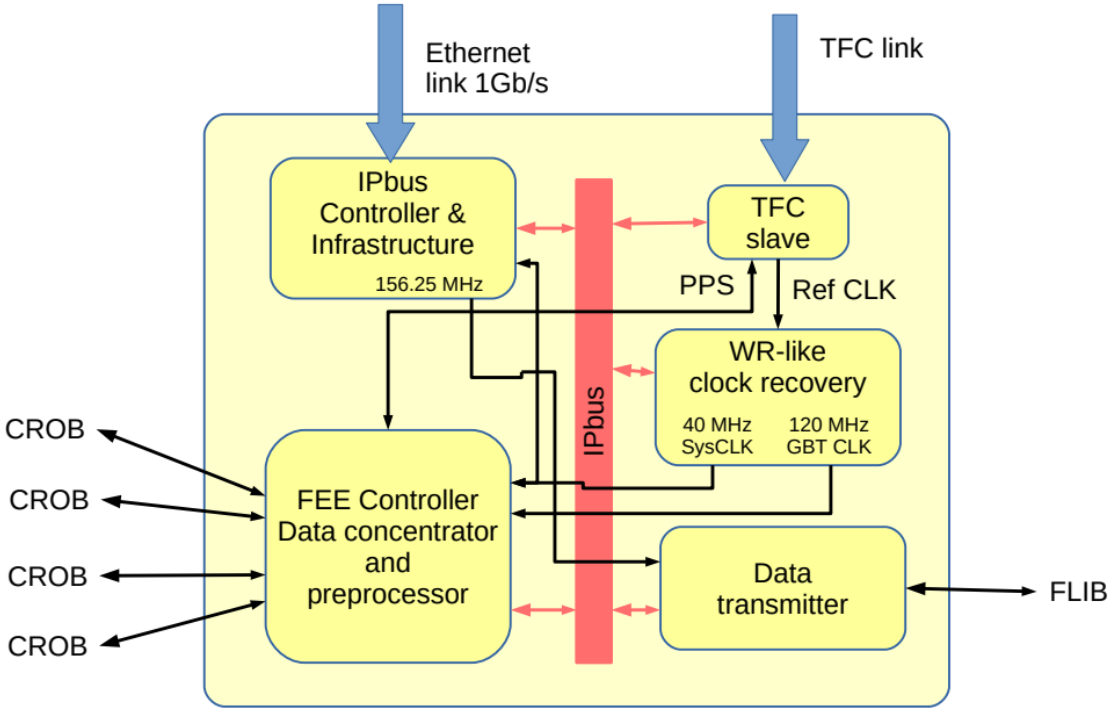
FW development



- We have participated in development of the STS-XYTER (SMX) communication protocol
- Various FW blocks were developed in that process
  - The SMX model in FPGA
  - The SMX controller
  - The SMX protocol tester
  - Low level control and communication software
- Those solutions will be reused for BM@N , either directly or as parts of other designs

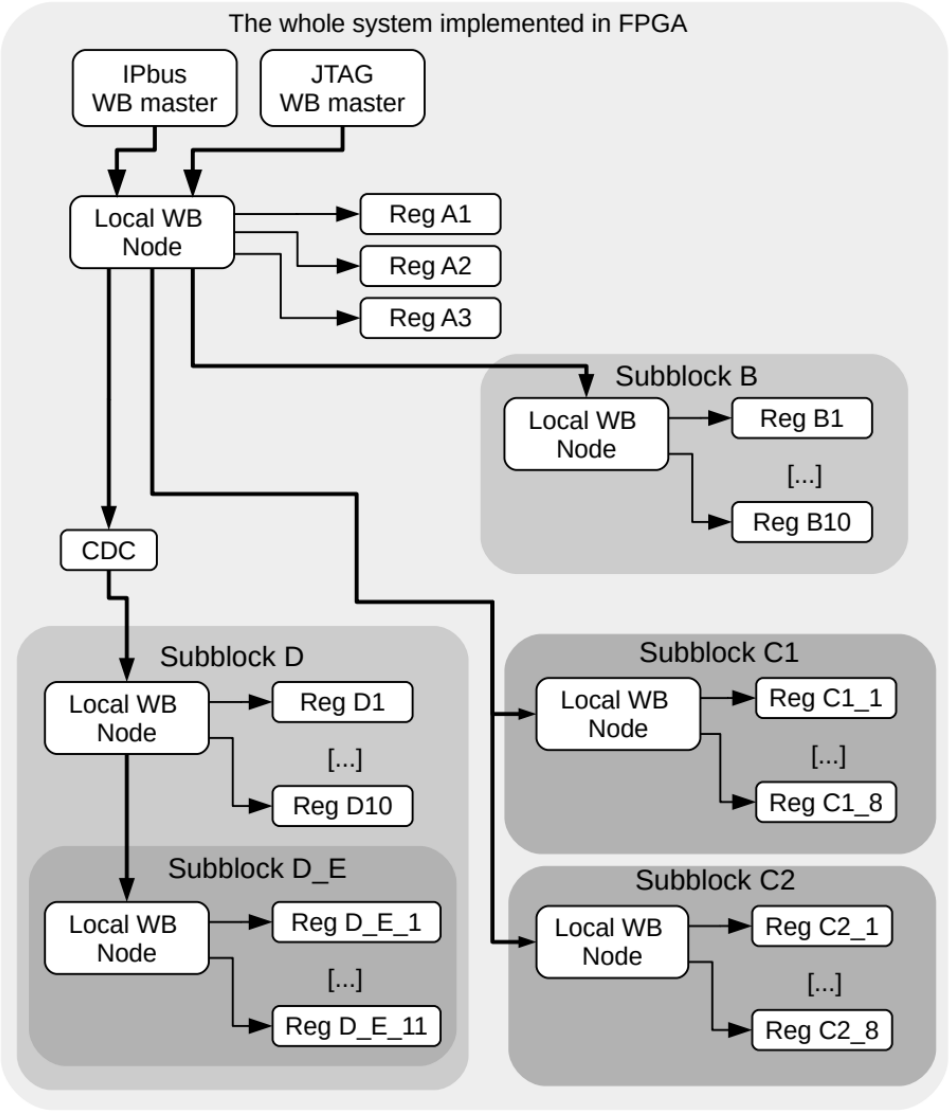
FW development – cont.

- The DPB FW used as development basis and in STS/MUCH setups was mostly developed at WUT
- The FW has been refactored with portability in mind
- The port to CRI platform will be done for CBM
- Similar port to the GERI platform will be needed for BM@N
- That allows us to utilize the synergy effects



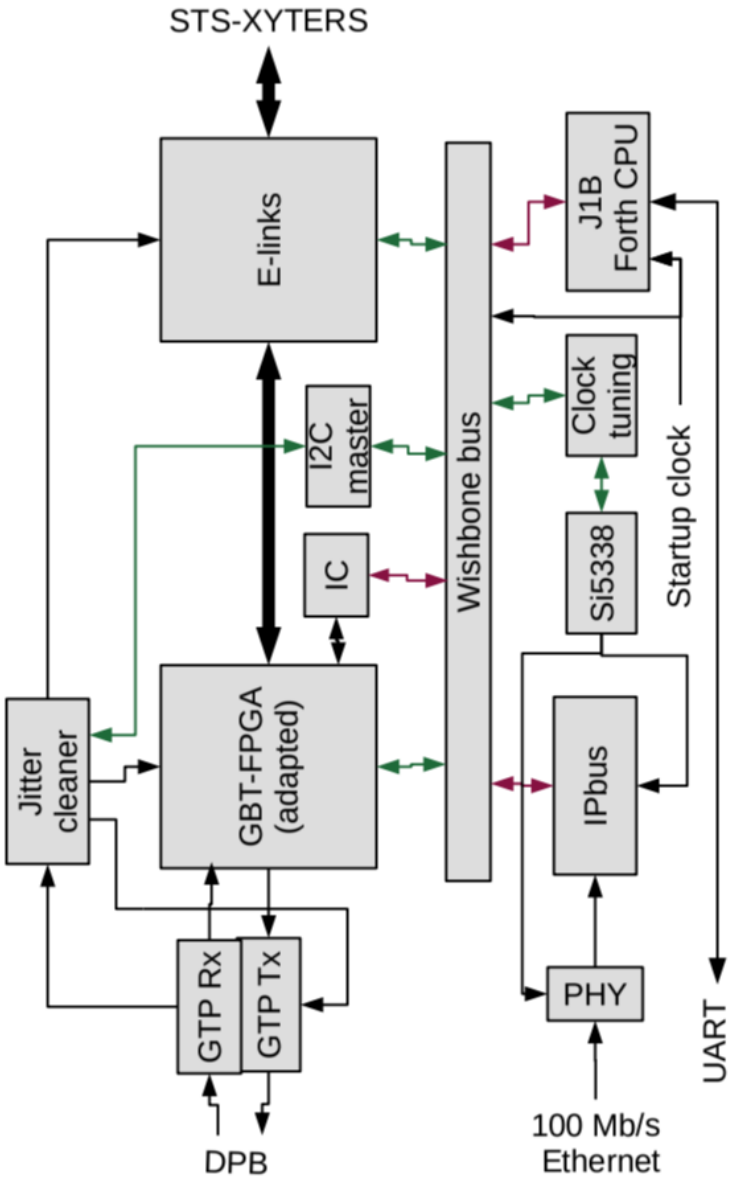
Dedicated solutions for complex FPGA FW

- To support complex hierarchical designs in FPGA we have created AGWB – the local control bus management system
- It has been tested, when developing the GBTxEMU firmware
- It will be used for CRI port
- It will be used for GERI port (full synergy)

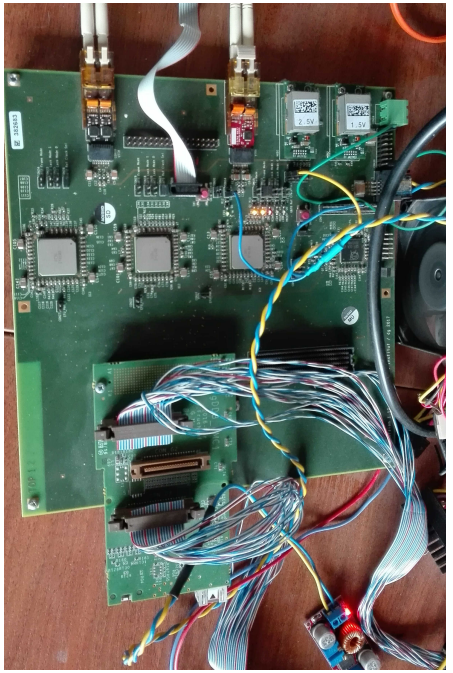


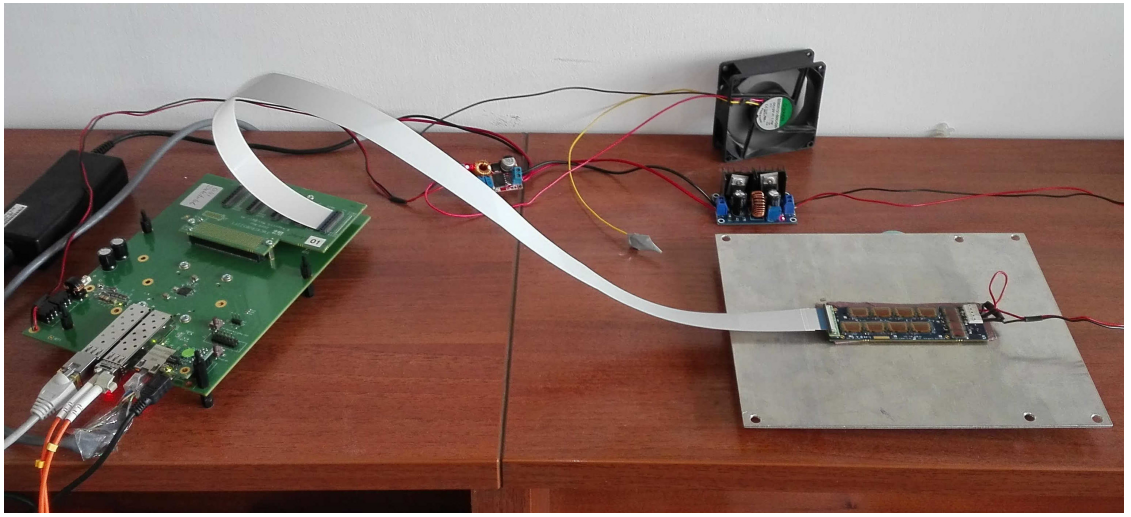
GBTxEMU firmware

- The firmware for GBTxEMU was developed mainly in 2019
- It provides functional emulation of the restricted GBTx ASIC
- It will be used in prototype version of BM@N readout chain
- It will be also used for preparation of the SMX testers (synergy)



Test setups at WUT





- Currently we have limited test setups prepared for GBT-based and GBTxEMU based readout development
- We also have dedicated machines with UltraScale and UltraScale+ FPGA boards
- However a possibility of remote debugging is essential

Remote testing and debugging

- Our group has rich extensive experience in remote testing and debugging of FPGA-based systems
  - We have successfully used this approach in CMS experiment in CERN (since 2006, using our own tools)
  - We have used that approach in JET (Culham) using standard tools provided by Xilinx
  - We were using that approach to test solutions used in CBM and to support mCBM
  - It is essential, when the same experts should be used to support systems both in FAIR and in JINR (synergy)

Future activity

- Evaluation of consequences of transition from IPbus control to PCIe control
  - Potentially it may reduce the complexity of the firmware
  - Full synergy with CBM
- Porting of GBT-FPGA to GERI platform
  - Previous experience with adaptation of GBT-FPGA
  - BM@N specific
- Porting of other components of DPB firmware to GERI (partial synergy)
- Development of new components specific for BM@N – e.g. adaptation for triggered acquisition (depending on final structure of the reaudout)
- Preparation of low level control software for new design (full synergy)

Influence of the COVID-19 crisis

- The hiring procedure at WUT was significantly delayed (by ca. 3 months) due to lockdown – our specialists are hired since 15.05.2020
- Fortunately most part of the FW development/testing can be done remotely
- We have faced certain lockdown-related problems with preparing the test setups. E.g., the setup for PCIe development that required physical access to the machine was located at home and was available only for a single developer.Posibility to modify/fix other test setups was also limited.

Thank you for your attention