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Status of straw detector readout

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24 June 2020, Kraków

Current activities

- Front-End development and tests
  - Talks on FEE and Tracking sessions
  - M. Idzik, A. Malige
- Digitizing boards upgrade
  - M. Michałek
- Preprocessing firmware
  - A. Malige
- HPC data analysis
  - B. Soból, P. Poznański, J. Płażek

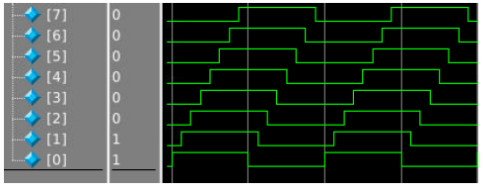
Digitizing boards upgrade

- Current platform TRB3
  - High resolution TDC
  - 48 channels per TDC (3 FEE cards)
  - 4 TDCs to one output link

Trb.gsi.de

- TRB5SC
  - Lattice ECP5
  - Revision 2 produced, under tests in Frankfurt (J. Michel)
  - Basic TrbNet components migrated

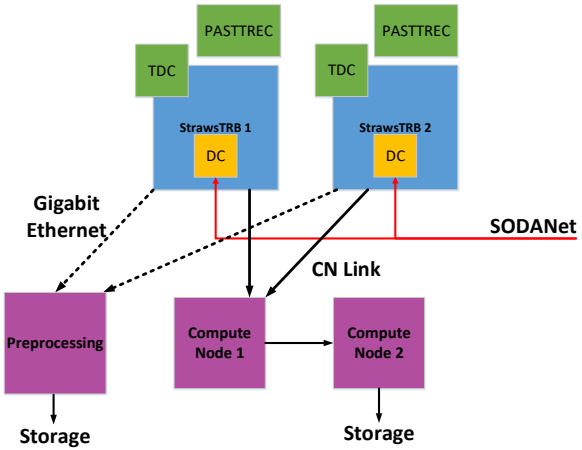
  - Project carried out by Mateusz Michałek (Technical University in Cracow)
  - Low resolution TDC under development
    - Reduced data volume, optimised data format, avoid high resolution calibrations and errors problems
    - Aim is to fit 64 channels (4 FEE cards) per TDC/FPGA
    - 8 clocks shifted in phase -> 16 samples within one master clock cycle
    - Current design has 250 MHz master clock -> 250 ps resolution
    - Ongoing hardware tests on Lattice ECP5 Dev board

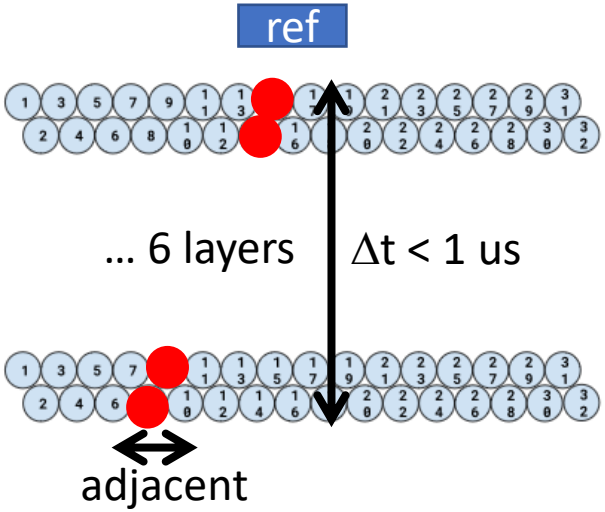


Preprocessing firmware

- Setup from Juelich 2019 beamtime

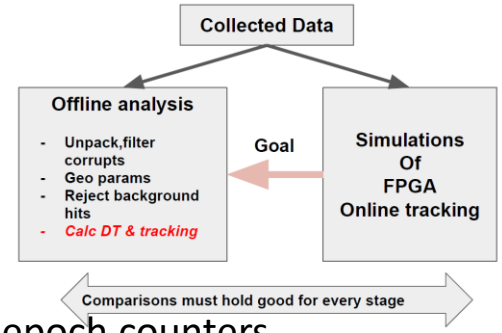
- Preprocessing firmware on ZCU102 dev board
  - Mirrored data forwarded to the preprocessing
  - Accept or drop current SB decision
  - Decision criteria:
    - Hits on all 8 layer
    - Hits on adjacent straws within double layer
    - Time coincidence – 1us time window
    - Hit on external reference sinctillator





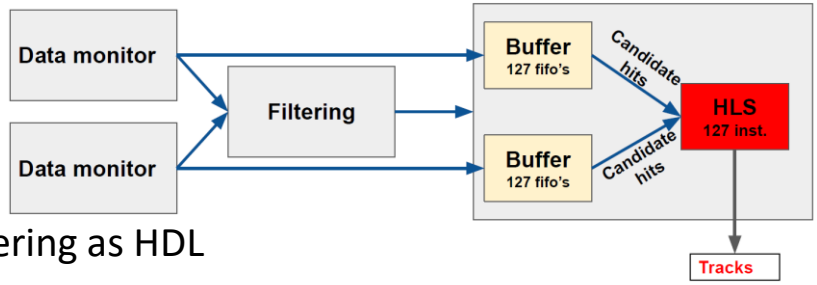
Preprocessing firmware

- Project carried out by Akshay Malige (UJ)



A. Malige

- Find agreement with software, offline analysis
  - Differences on handling TDC errors (missing edges, corrupted epoch counters, etc.) by software and hardware data unpackers



A. Malige

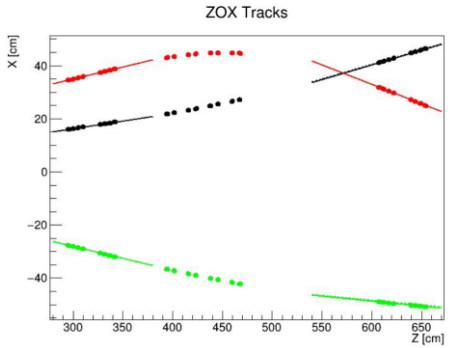
- Firmware:
  - Data reception / unpacking / filtering / buffering as HDL
  - Track fitting in High Level Synthesis

  - Superburst time window segmented into 127 timebins
  - Valid hits, sorted into timebins
  - Timebins with track candidates (decision conditions) processed in parallel

HPC data analysis

- Project carried out by Bartosz Soból (UJ)

- Evaluation of the tracking algorithm (FT TDR) implemented by J. Płażek and P. Poznański (Technical University in Cracow) on HPC platforms (server with GPU or FPGA)



B. Soból

- Complete code refactorization
- Input data from PANDAROOT simulations
- Tracking procedures isolated into functions dedicated for acceleration
  - Linear track fitter
  - Circular track fitter

HPC data analysis

- At the moment, preliminary CPU-only software validation

- Next: Evaluation of SYCL
  - High-level, heterogenous programming model
  - Superset of tools and compilers to target diverse hardware platforms
  - Single-source for any platform
  - Modern C++ standard support
  - Host main <–> accelerated function architecture
  - HDL kernels intergation

- Hardware access:
  - HPC cluster Prometheus Cyfronet Cracow (CPU + GPU)
  - ETH Zurich (CPU + Xilinx Alveo)
  - Ongoing ordering procedure for workstations and Alveo cards