university of groningen

kvi - center for advanced radiation technology

DAQ TDR status

M. Kavatsyuk

KVI-CART, University of Groningen

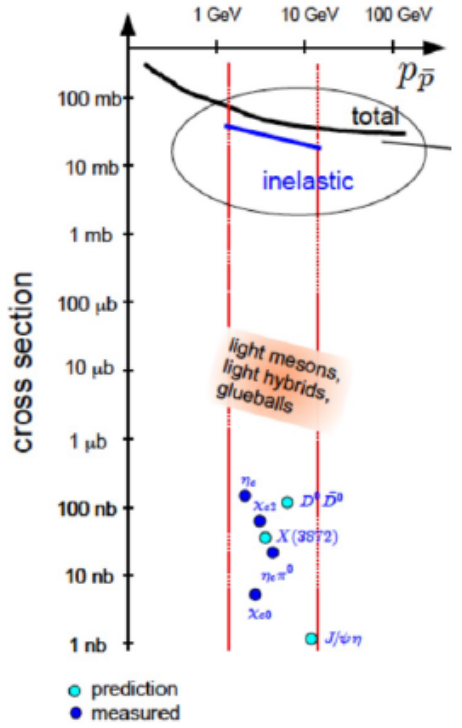
for the PANDA collaboration

Technical Design Report for the:
$\overline{\text{P}}$ANDA Data Acquisition and Event Filtring

(AntiProton Annihilations at Darmstadt)
Strong Interaction Studies with Antiprotons

$\overline{\text{P}}$ANDA Collaboration

November 7, 2018



TDR Status

- TDR passed internal review with positive outcome
  (Many thanks for reviewers and for everyone who contributed to the TDR)

Internal Review of the Technical Design Report for the PANDA Data Acquisition Final Report

Holger Flemming[1], Niko Neufeld[2], Stefan Ritt[3], and Carsten Schwarz[1]

[1]*GSI Helmholtzzentrum für Schwerionenforschung GmbH, Darmstadt, Germany*
[2]*CERN, Geneva, Switzerland*
[3]*Paul Scherrer Institut, Villingen, Switzerland*

May 18, 2020

- Revision is ongoing with aim to submit in August revised version to ECE

Reviewers Observations

1. **The PANDA Data Acquisition and Technical Progress**
   The DAQ concept described in the TDR relies on several components especially developed for the PANDA experiment. While this is mandatory for front-end components for the back-end data processing there might be options to use commercial off-the-shelf products.

Be aware of commercial solutions

2. **The Interface between Data Acquisition and Detector Control System and Experiment Control System**
   The Data Acquisition system has certain connections to the DCS as well as to the ECS. In this context the reviewers got the impression that the organisational interfaces and responsibilities are not always pointed out clearly. It might be that tasks are not assigned completely.

Do not underestimate required manpower

3. **FPGA Firmware Upload**
   It is practical experience that FPGA firmware will improve over time and an in-field reprogramming of FPGAs will be necessary. It is not described how a firmware upgrade for all FPGA boards in the system will be done after the system has been installed. In particular it is not described how the situation is handled if the new firmware has some issues which are only discovered after deployment and which effects the firmware upload functionallty itself.

Fail-safe firmware should be used for complete system

4. **Organisation and Resources**

- **Toolkit for data-processing algorithms**
- **How to keep knowledge within collaboration**

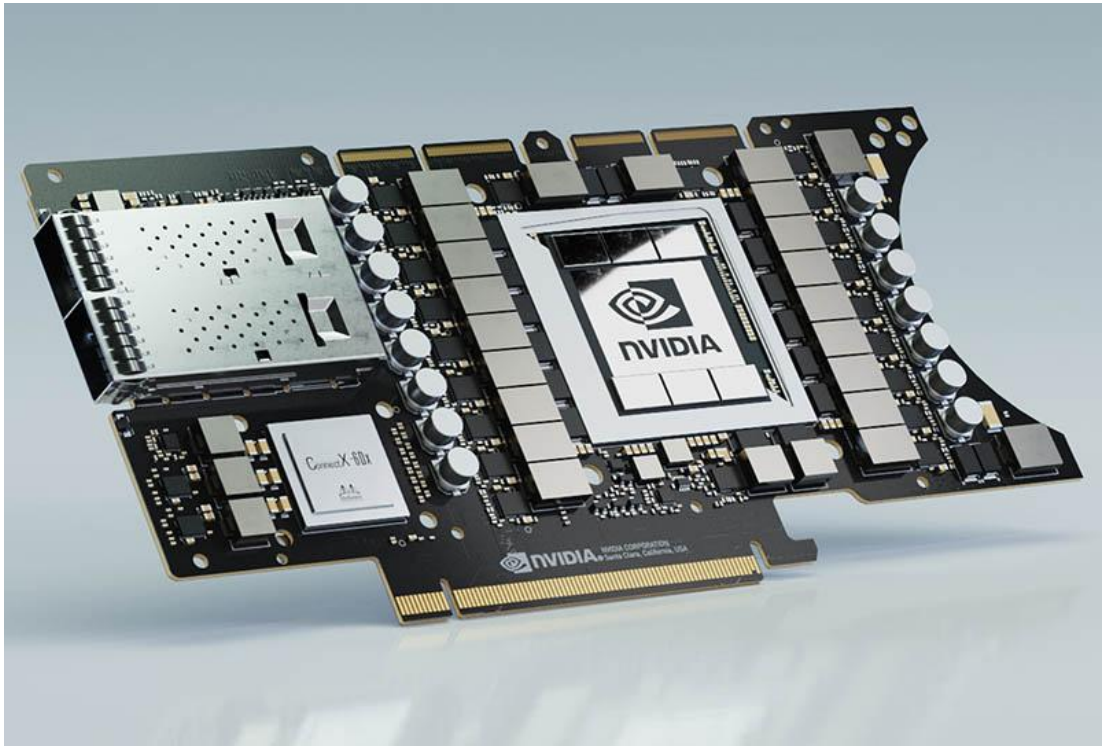
Reviewers Recommendations

- **Be aware of commercial solutions**
- **Set up a common test of ECS together with a vertical slice of DAQ hardware as soon as possible**
- **Fail-safe firmware should be used for complete system**

Commercial Solutions for DAQ?

NVIDIA EGX A100:
GPU with network interface

Xilinx Alveo:
FPGA-based accelerator cards



- Ethernet as standard communication protocol above DC level?
- RoCE (RDMA over Ethernet) – data transfer between FPGA and PC hardware?

Fail-safe FPGA programming

Possible solutions:

- Extrnal supervisor – separate CPLD of FPGA with SODANET communication with access to the FLASH memory
- External watchdog circuit which boots “golden image” if communication with SODANET can not be established

Manpower

DAQ-related work packages: Hardware

(R&D, design, testing, production and screening)

- **Data Concentrator**
  (core of the DAQ, used for the burst-building network as well)
  - hardware design (Uppsala) – done for the prototype
  - prototype testing/debugging (DAQ core) – 0.5 PY
  - production screening (Uppsala)
- **Compute Node**
  - design/testing/production (IHEP)
- **HPC interface**
  - design/testing/production (KIT)

DAQ-related work packages: Firmware

(R&D, design, testing)

- **SODANET**
  - support, development (DAQ core) – 0.5 PY
  - DAQ-accelerator interface (DAQ core) – 0.5 PY
- **Framework for data-handling IP cores** and **Communication protocols**
  - development / testing / deployment (DAQ core) – few PY
- **Data-processing algorithms**
  - Event and burst-building (DAQ core) – 0.5 PY
  - Tracking (Lanzhou?)
  - FW tracking (Krakow)

DAQ-related work packages: Software

(R&D, design, testing)

- **DAQ functionality** (so far only SODANET protocol)
  (DAQ core)
- **DAQ control** (communication with DSC, ECS)
- (DAQ core)
- **DAQ – online computing interface**
  (DAQ core)
- **Stand-alone DAQ** (KIT/Bochum/Julich)

Development/deployment strategy:

- Develop stand-alone DAQ
- Stimulate of the stand-alone DAQ by all subsystems
- Deploy DAQ at FAIR

DAQ Interface to PANDA Subsystems

SODANET interface implemented for:

- EMC
- TRB-based TDCs (Fw tracker, DIRC,..)
- Luminosity monitor (in progress)...

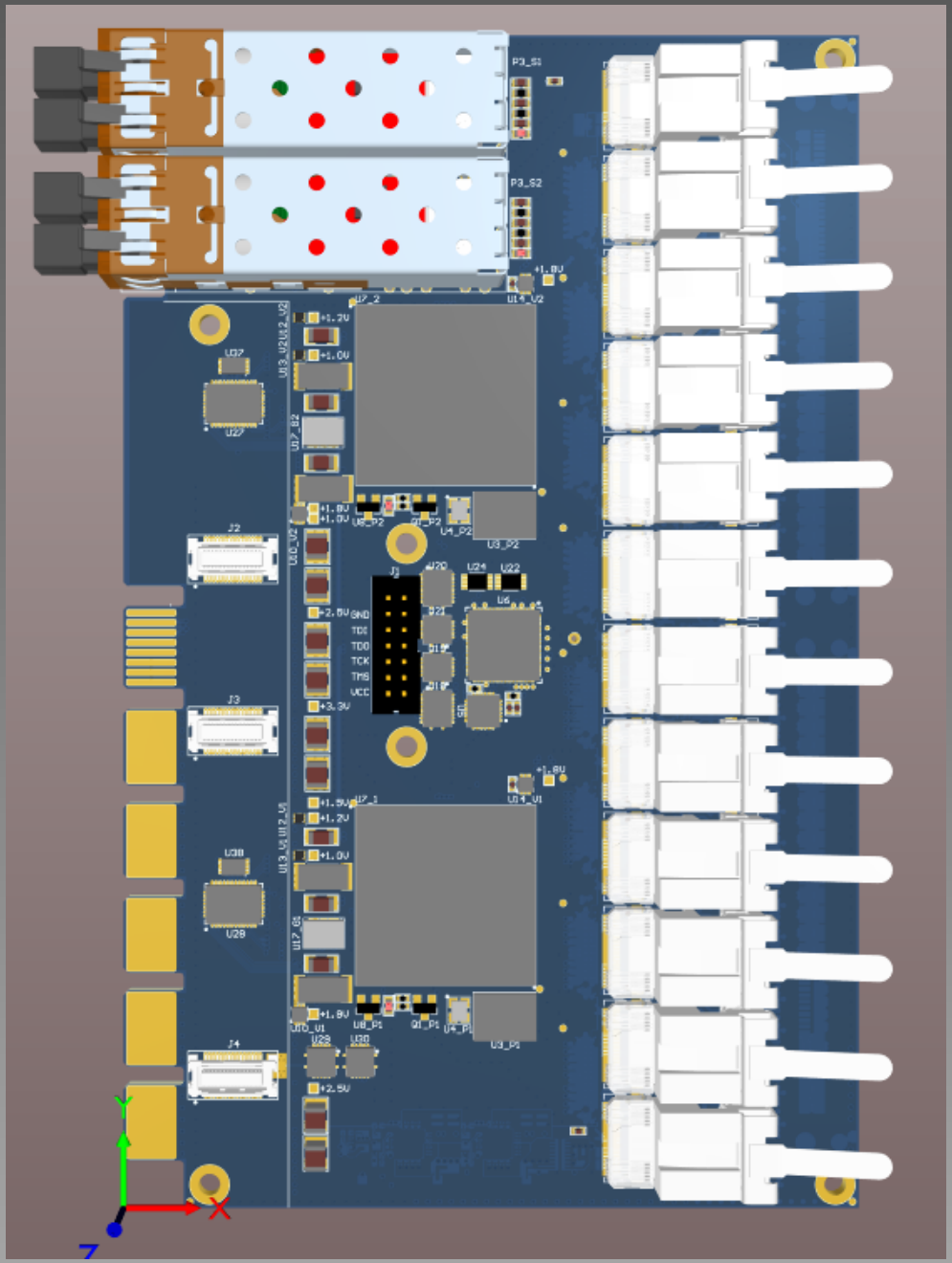
SODANET endpoint project is available for those who would like to start implementation of the SAODANET into other subsystems.

Each subsystem should take care of SODANET implementation!

It is encouraged to use the same hardware...

EMC Barrel Electronics

- LVDS ROB



Readout Board obtained from the 64-channel ADC for the EMC Forward Endcap

Status:

- Design started
- Data connector type needs to be decided
- Proposition:

  - Samtec ECUE (12-channel)
  - safe transfer with buffers (400 Mb/s)
  - AC transfer up to 1.2 Gb/s up to 3 m
  - 144 I/O