News about TRB Readout for STS1 and ADC Readout for Straws

Paweł Kulessa
(FZJ, IKP)

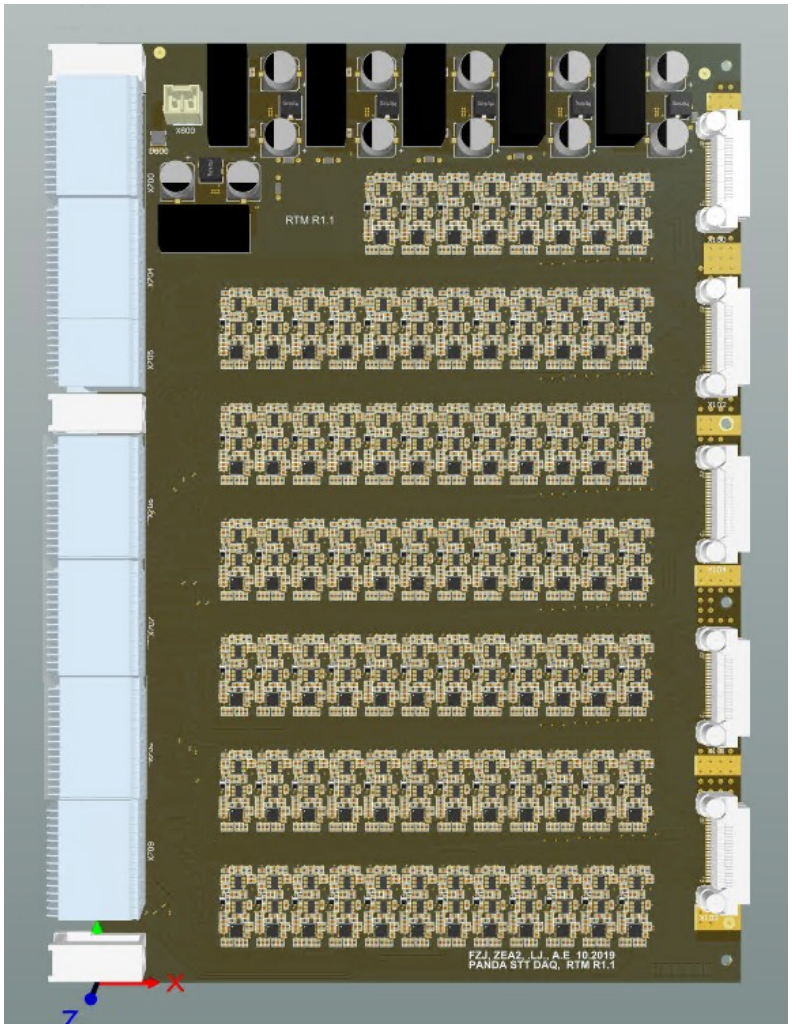
TOPICS

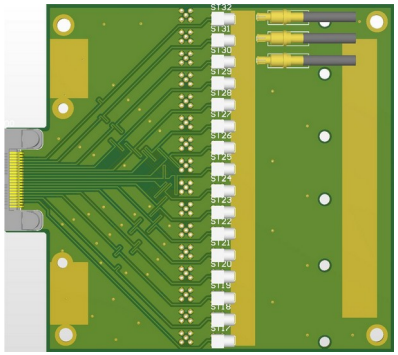
1. Front-end free sADC readout
   – new amplifiers board
   – new adapter for tests
   – crate modification

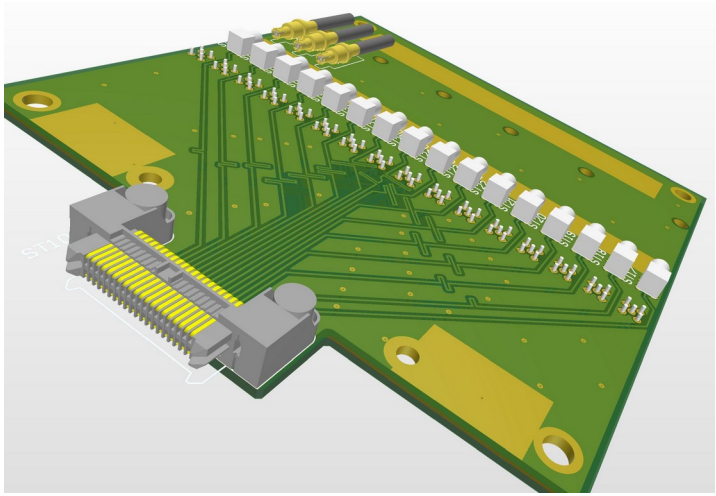
2. STS1 TRB3 readout
   – PASTTREC board tests – baseline scans
   – TRB3 firmware modifications for straw
   – TRB3 crate modification for “advanced” triggers

3. Summary

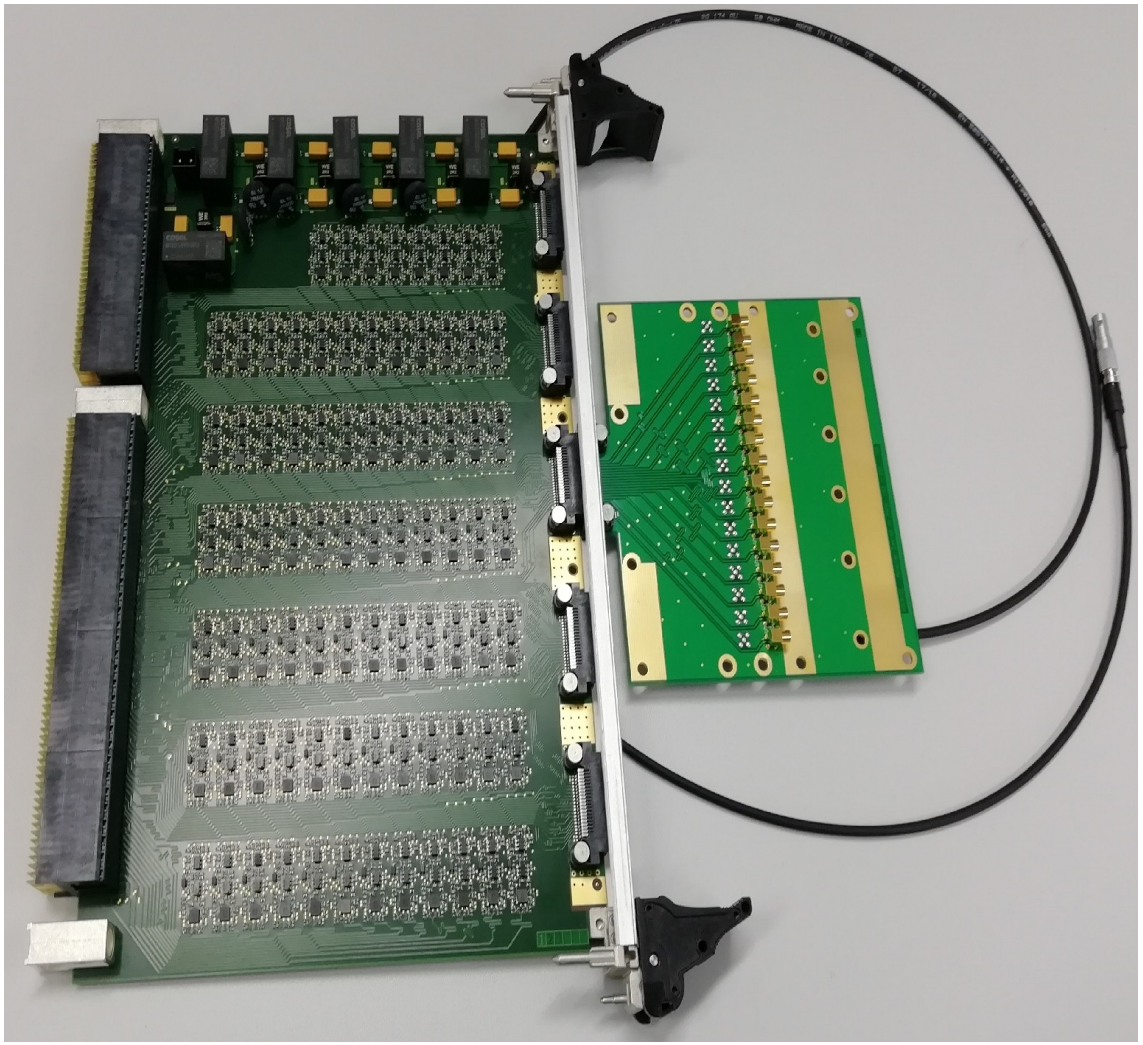
Front-end free sADC readout I



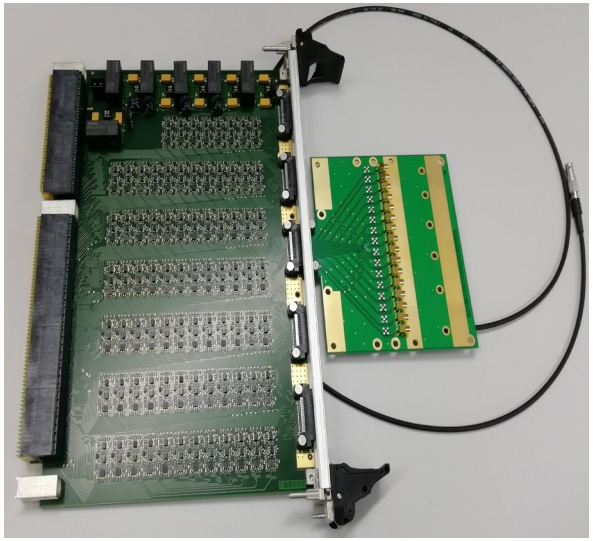




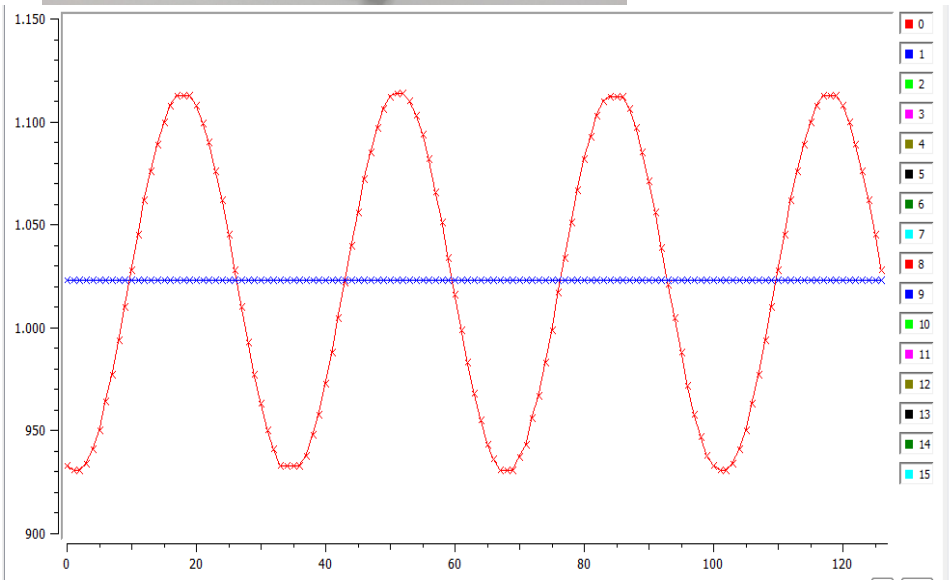
Front-end free sADC readout II



Front-end free sADC readout III

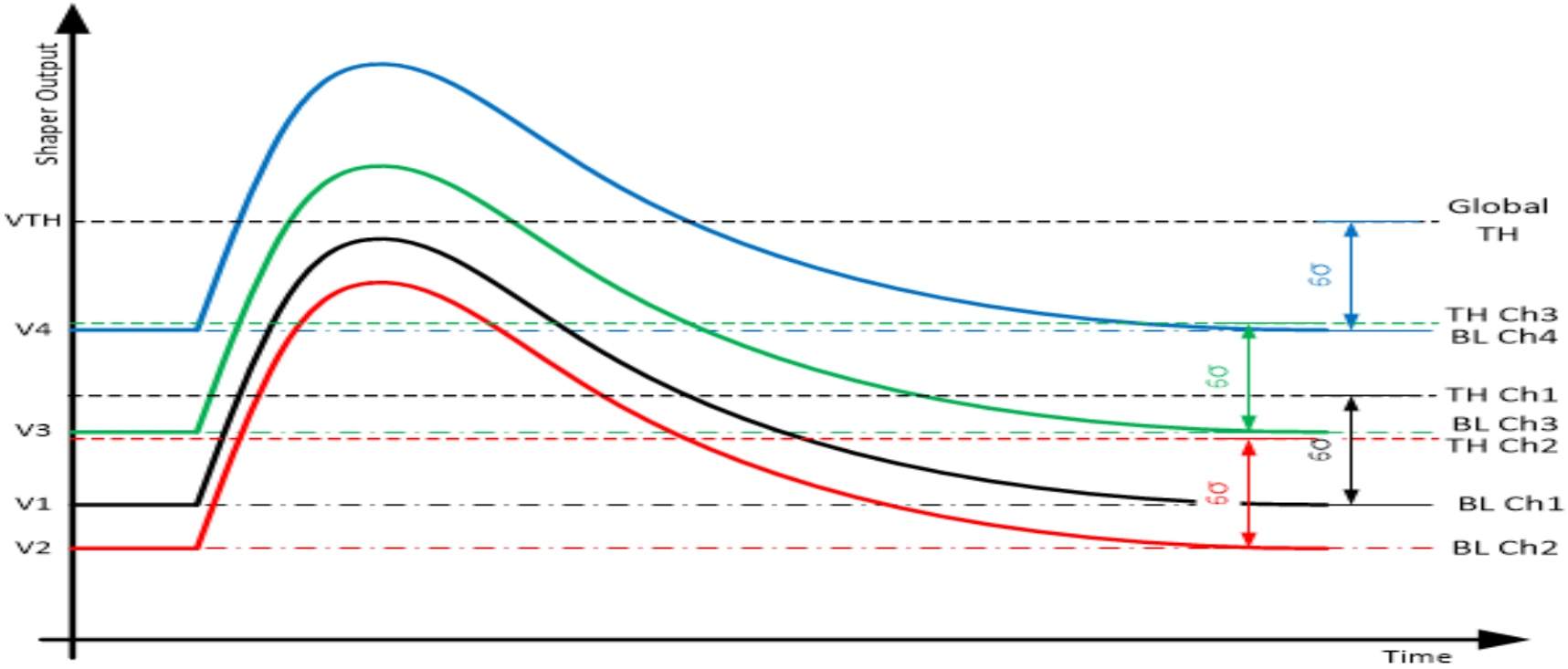


– 3 new ampl. boards made all 160 channels usable
– crate mechanical changes done
– test adapter boards made
– ampl. board with ampl. factor 1 for test, firmware development and to be used as scope.



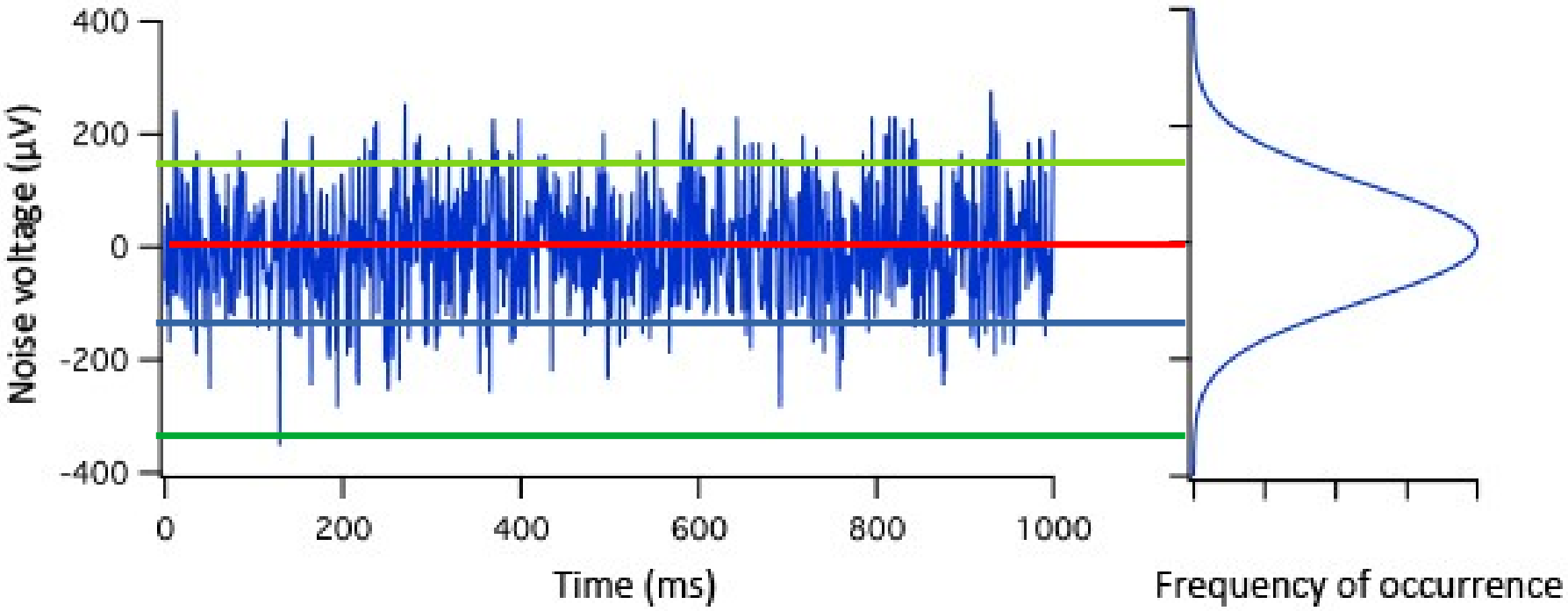
Plans:
– firmware development scope mode,processing
– second crate mech. modifications
– taking data with "analog" PASTTREC

STS1 TRB3 readout – baseline scans I



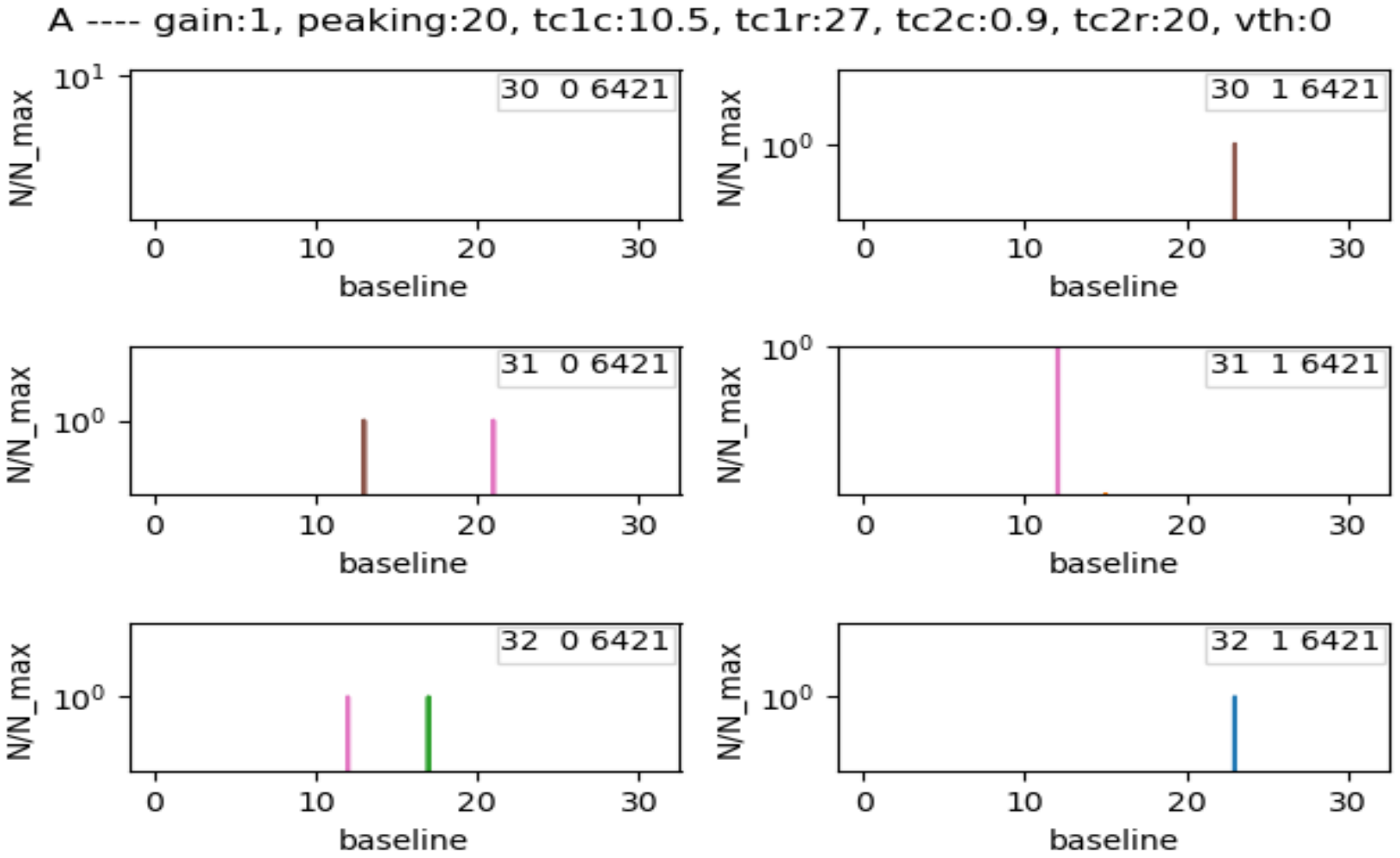
– differences in shapers – different baselines
– adjust baseline for each channel
– assumption – channels have same amplification

Baseline scans II

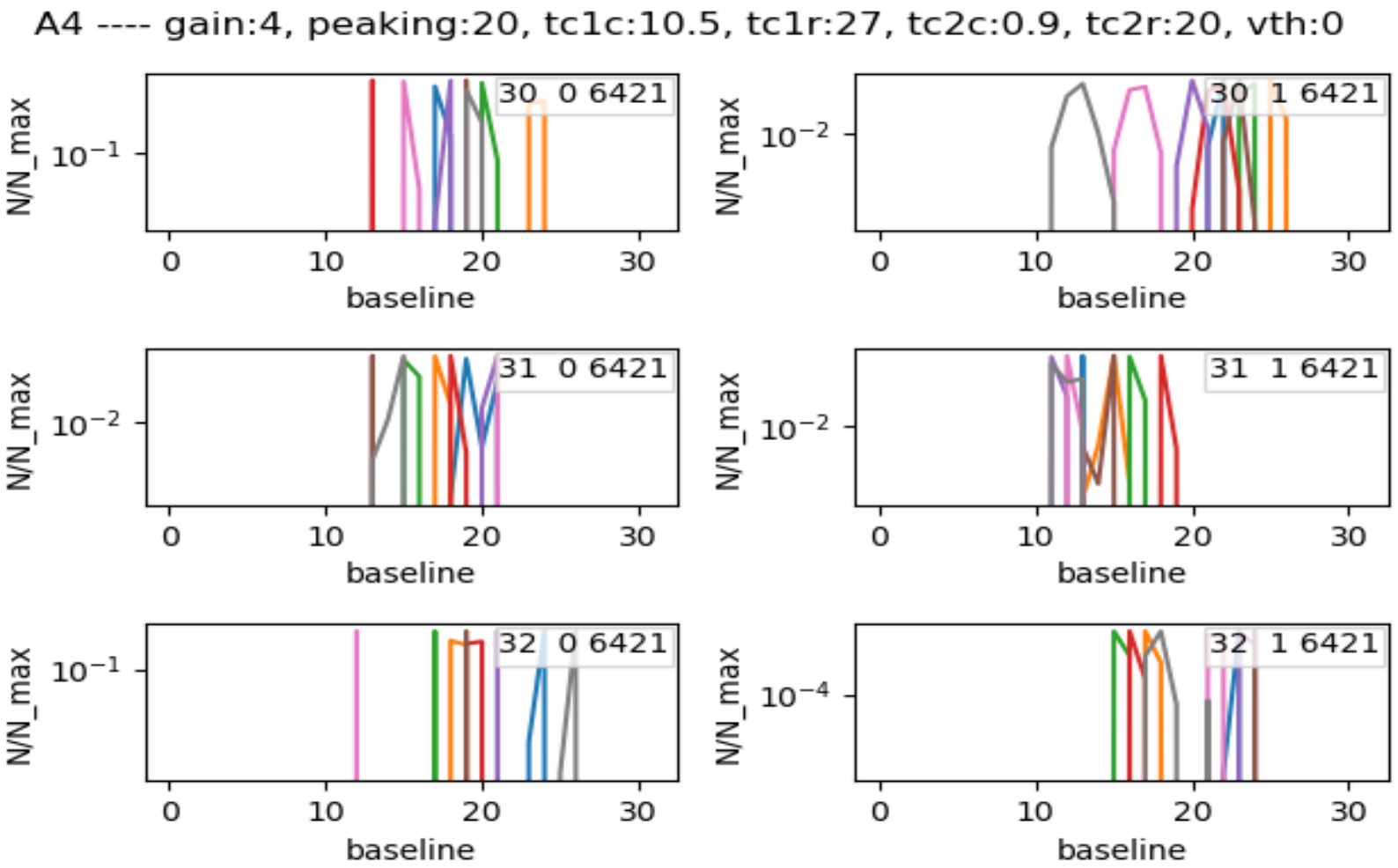


– scan detector noise moving baseline in full range (+/- 32 mV) [at threshold 0]
– maximum expected at baseline level (red line)
– noise is needed for correct working

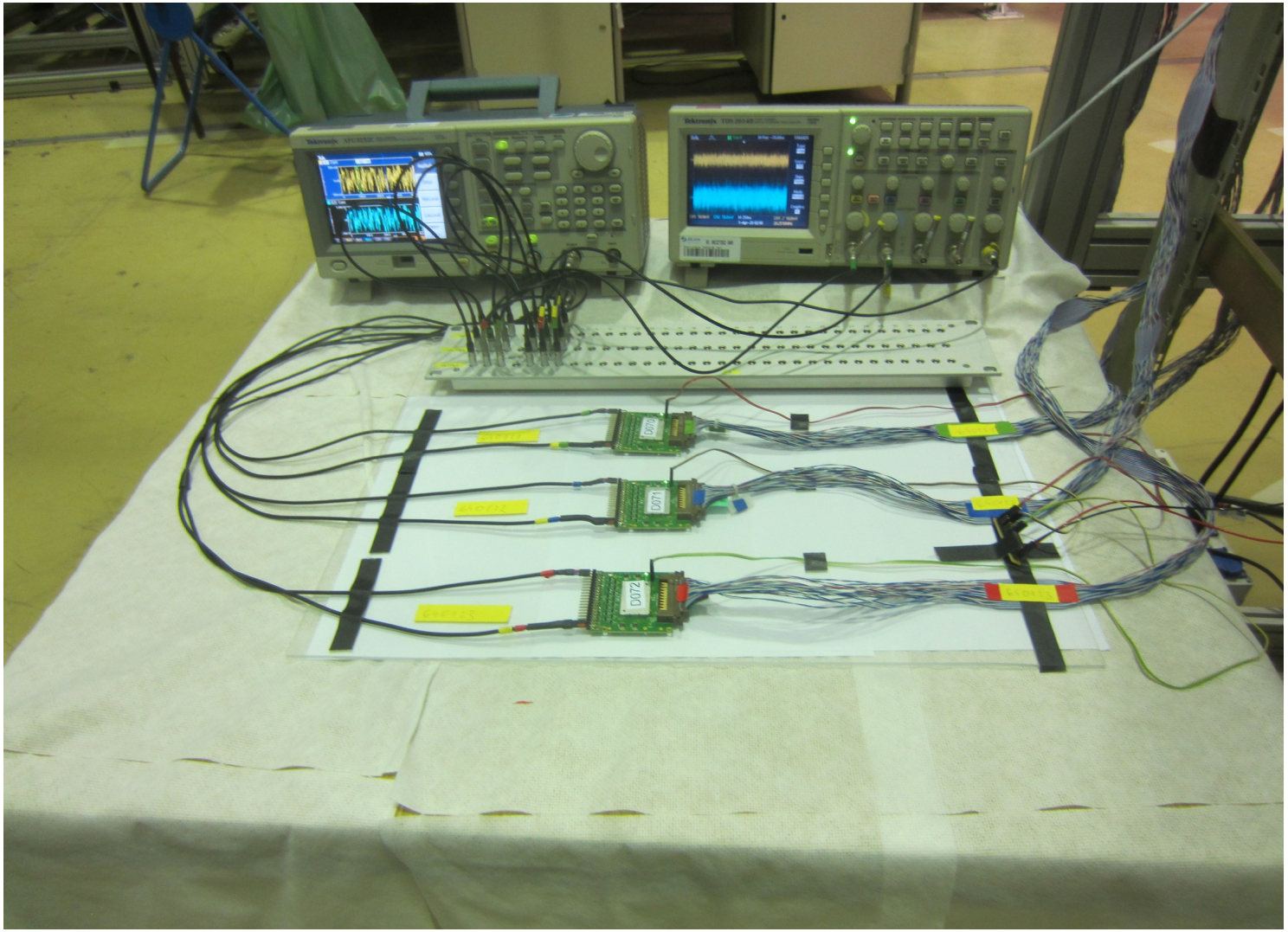
Baseline scans III (boards on det.)



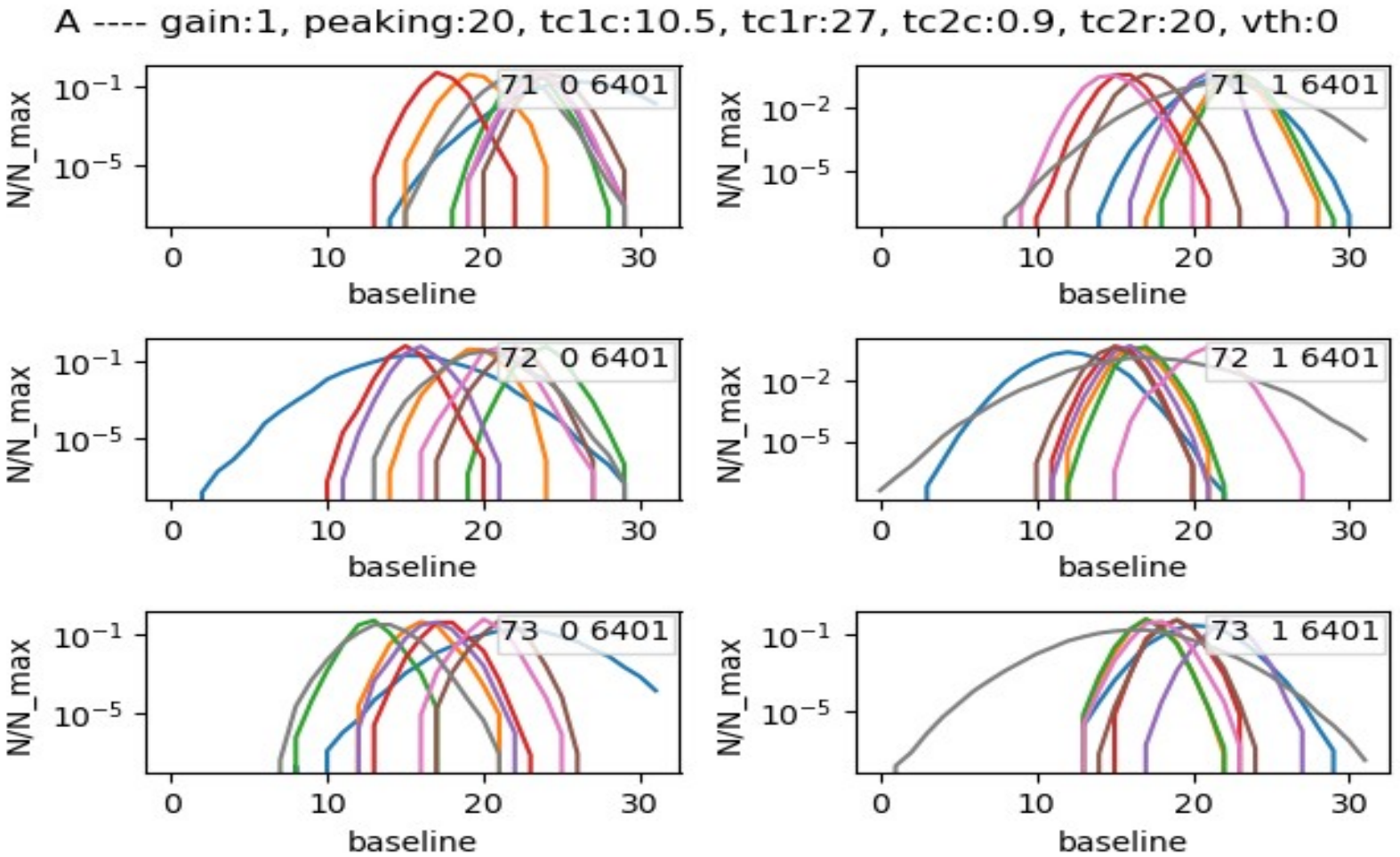
Baseline scans IV (board on detector – higher ampl.)



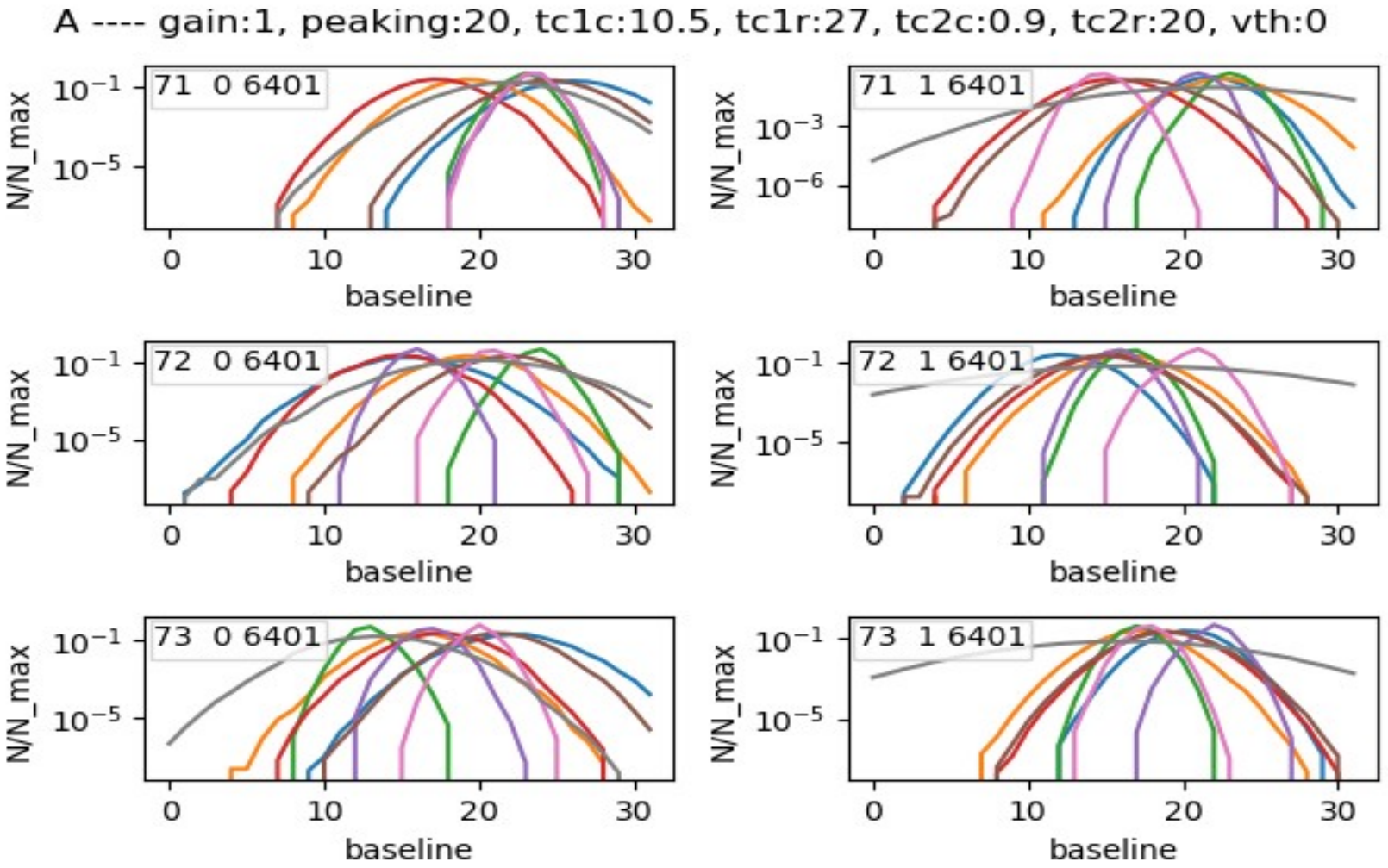
Baseline scans V – Test stand with function generator



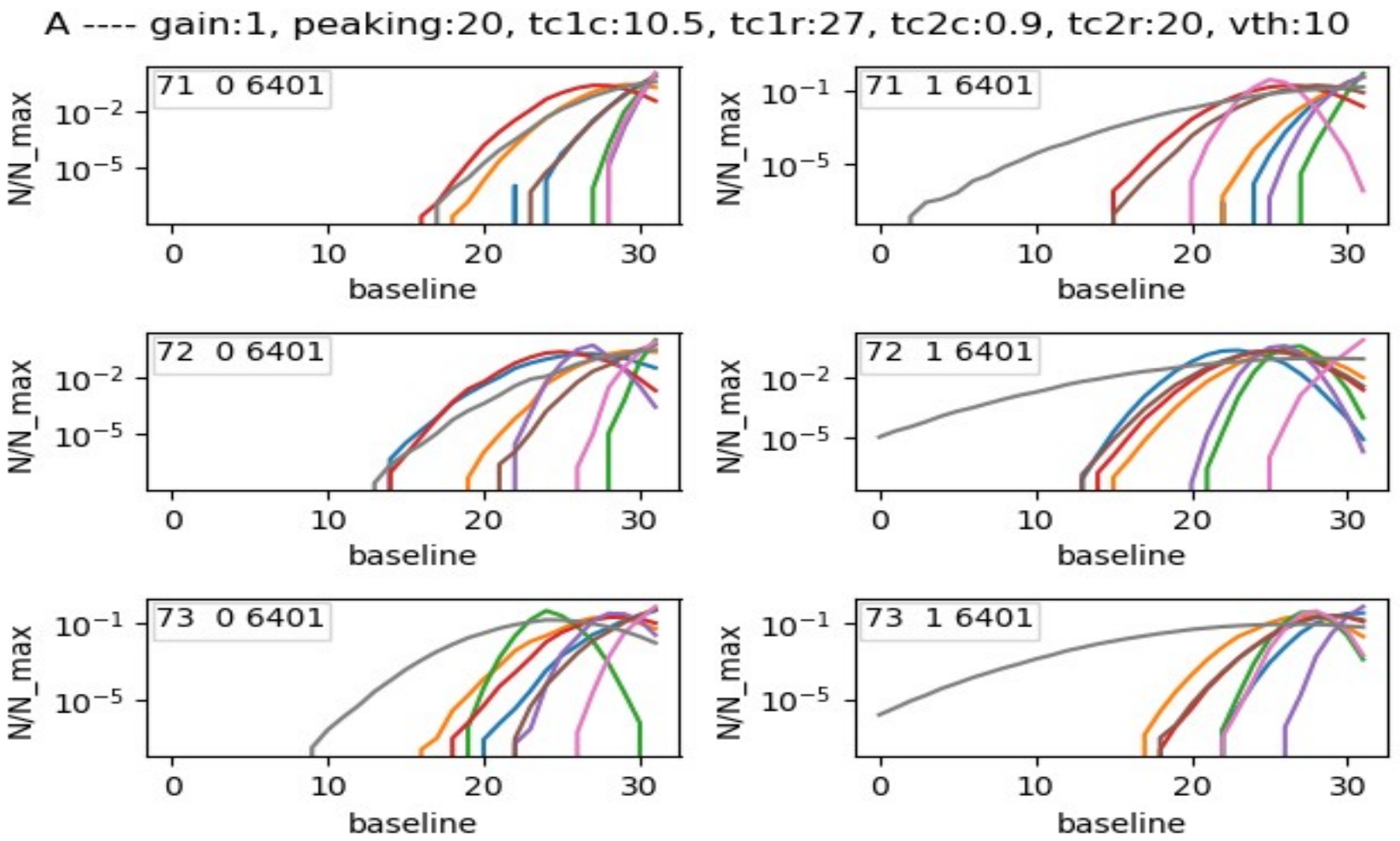
Results I



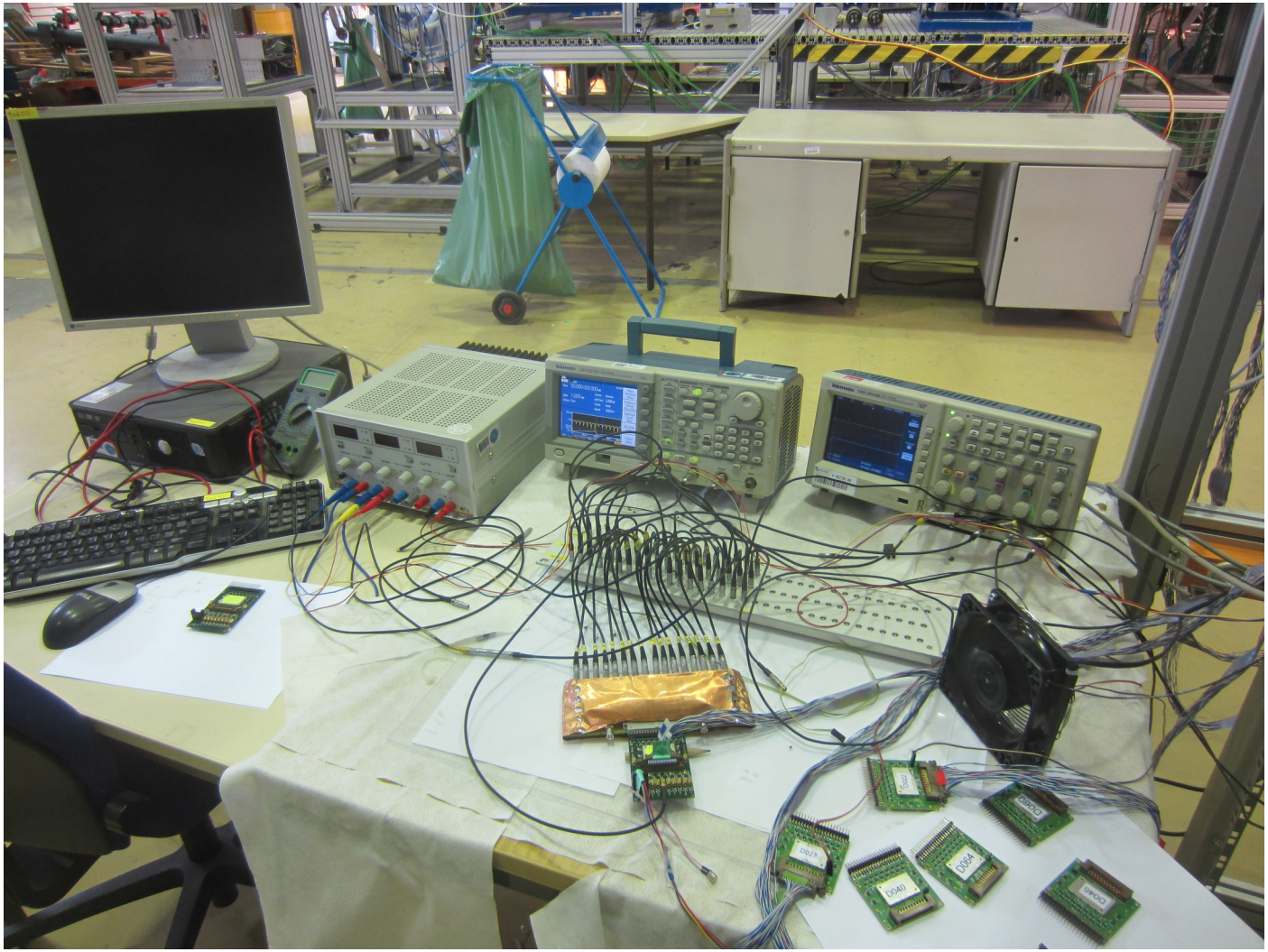
Results II – higher noise amplitude



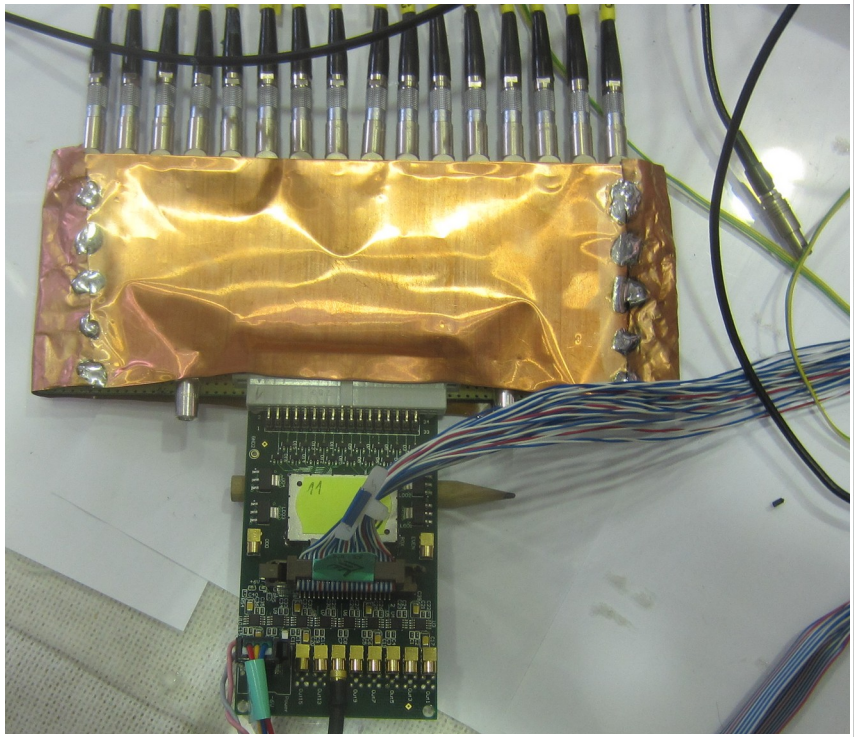
Results III – higher threshold level

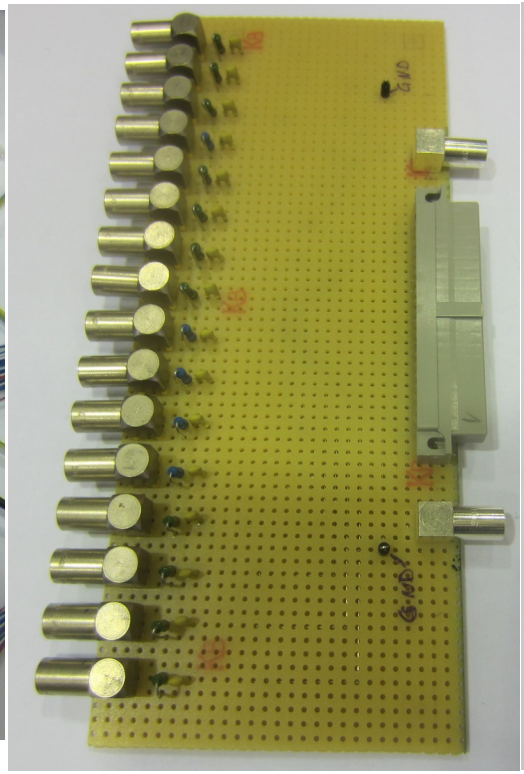


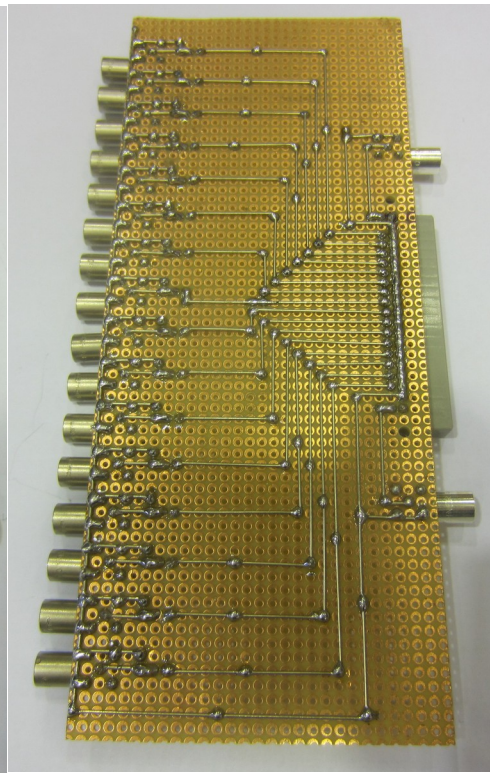
Threshold tests – test stand update and new adapter



New adapter for ASIC tests – thresholds, timing

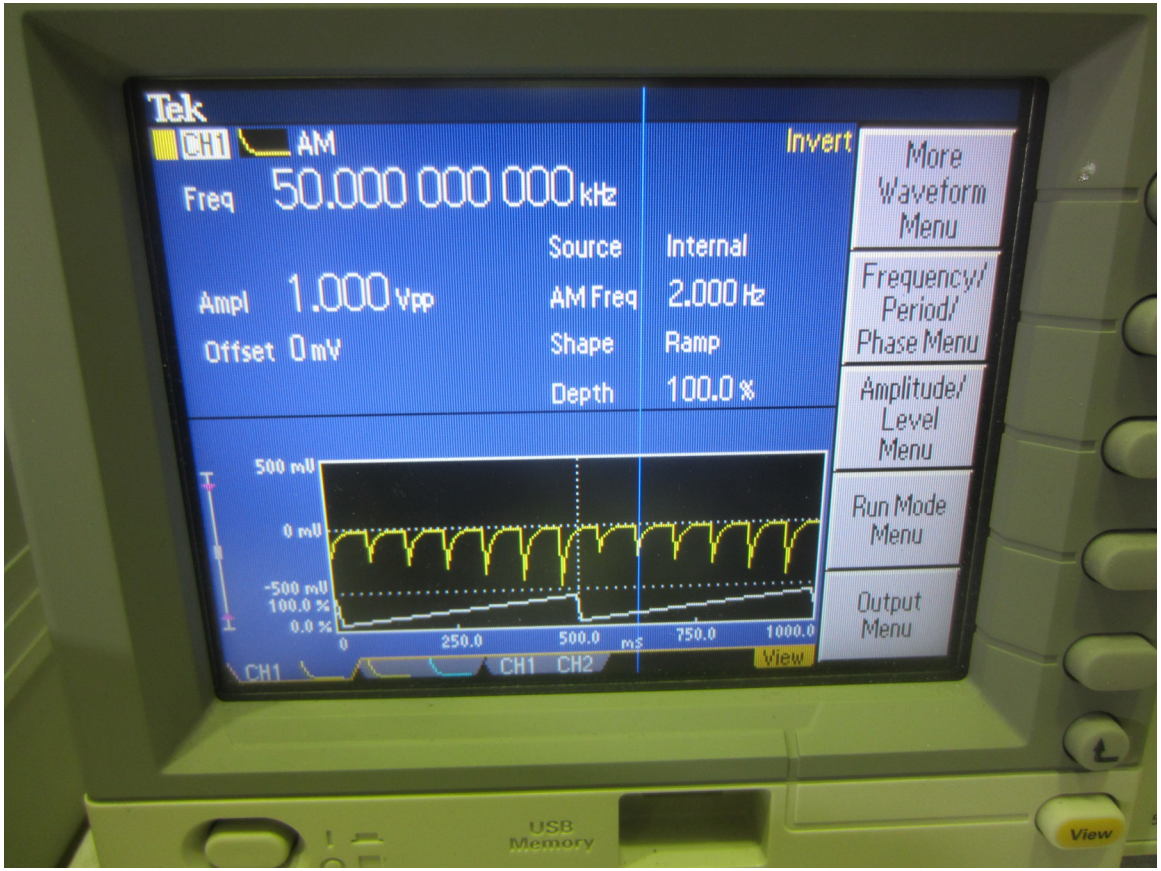






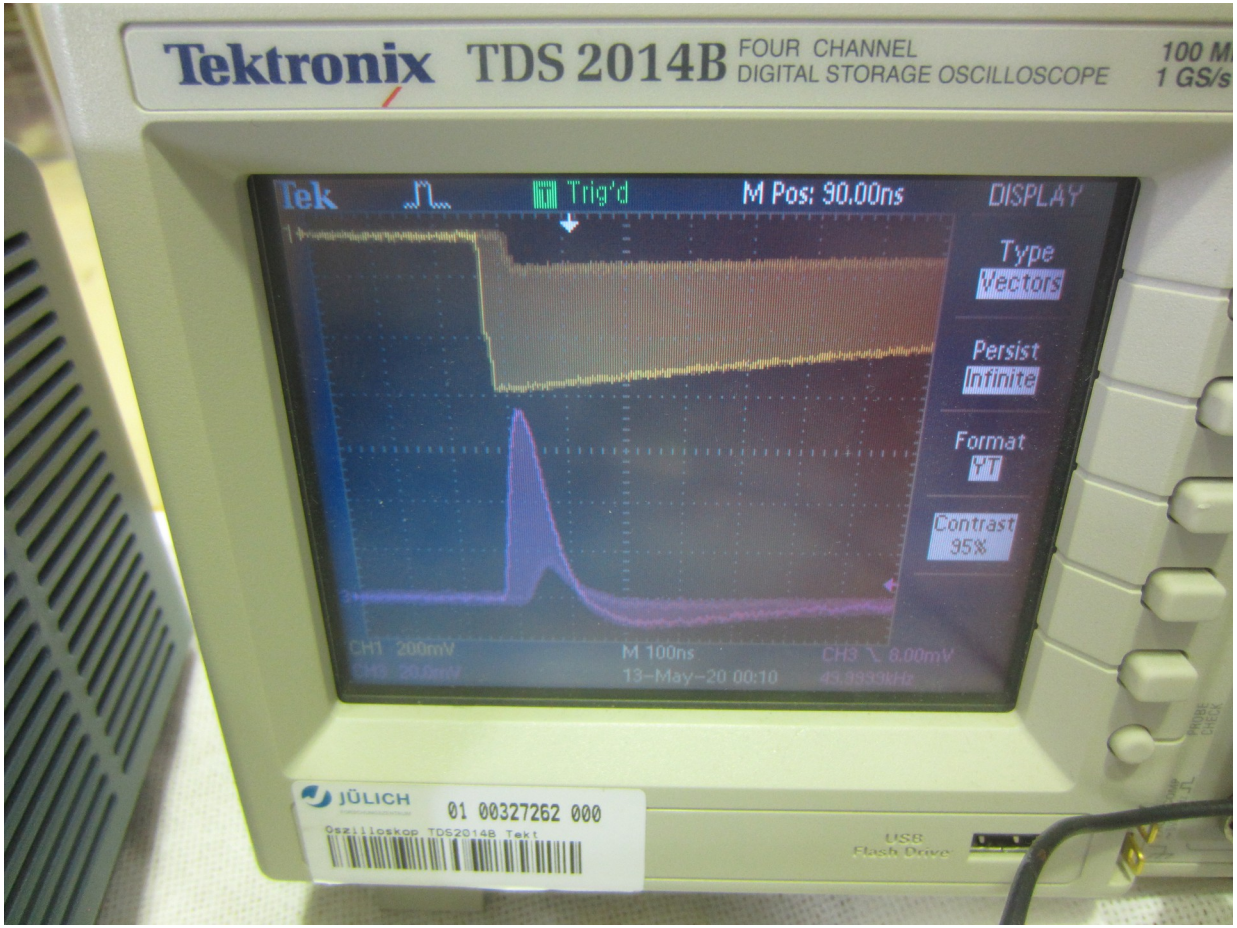
– To be used also for sADC readout tests

Threshold test I



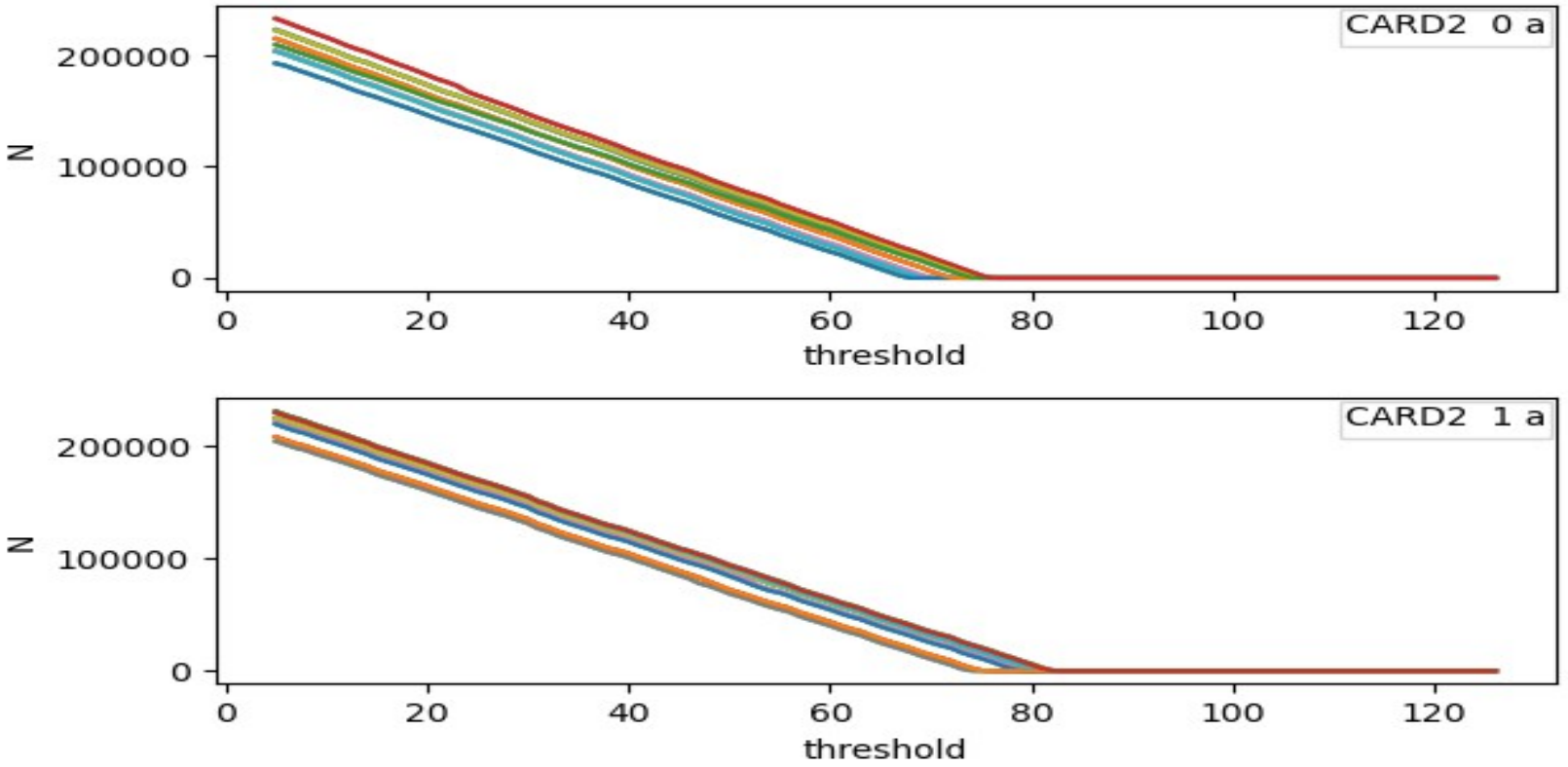
– AM (Amplitude Modulated) signal as input
– AM as linear ramp

Threshold test II



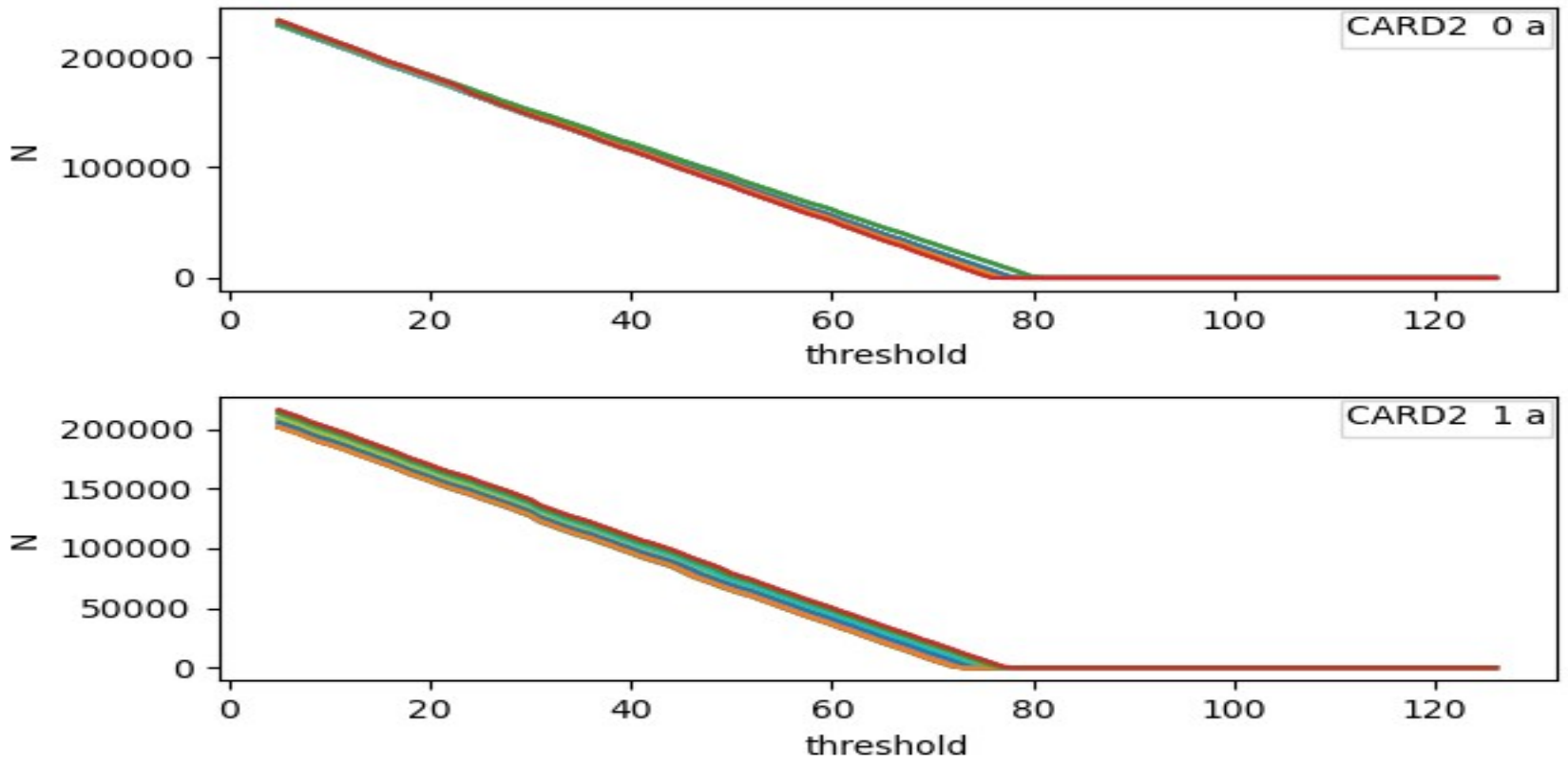
– 50 kHz signal rate
– 1 Hz AM modulation “rate” (1s from 0 to max)

Threshold test with AM Signals I



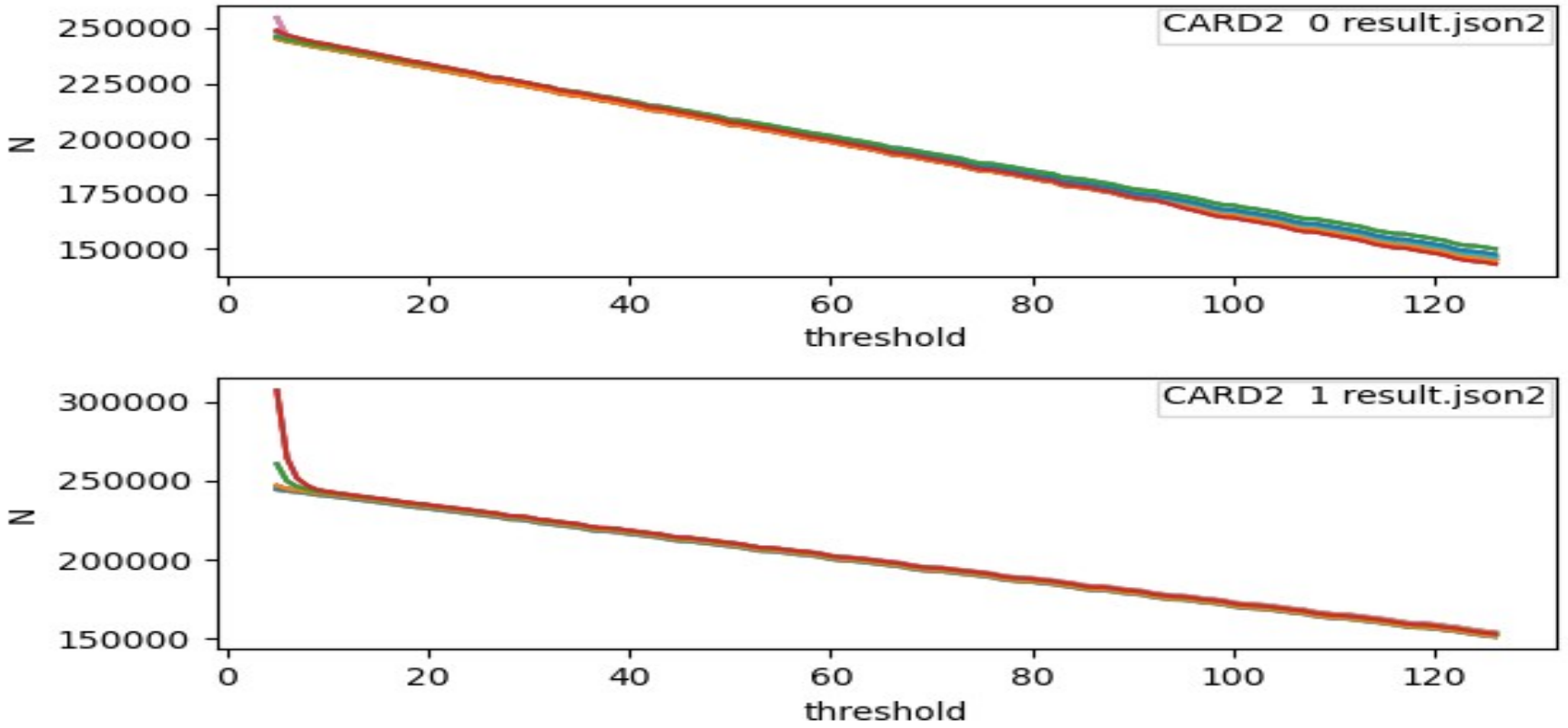
– 5s per threshold point
– all threshold correction set to same value

Threshold test IV



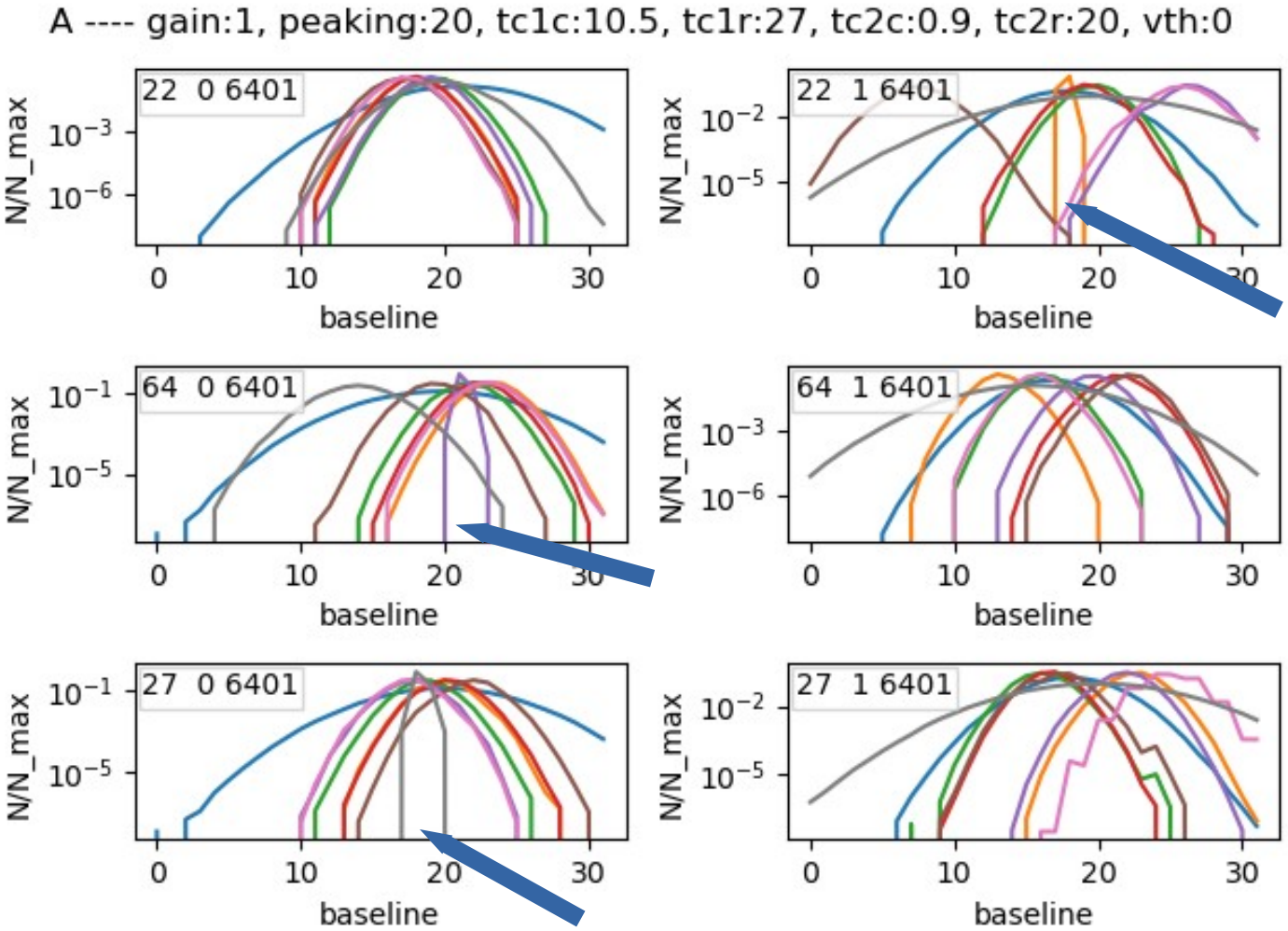
– correction set to values obtained from “noise” test

Threshold test V

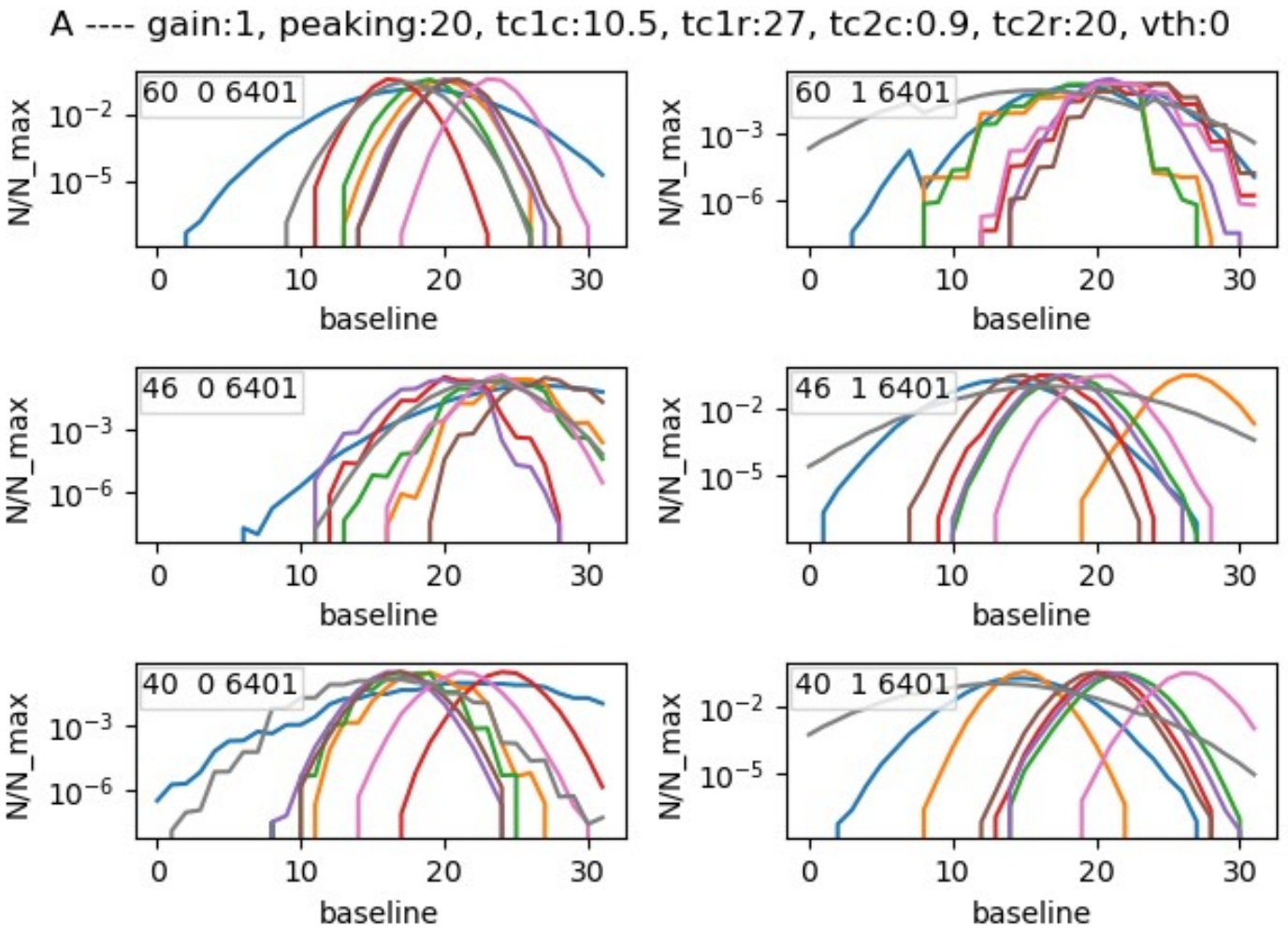


– Gain set to 4 (before 1)

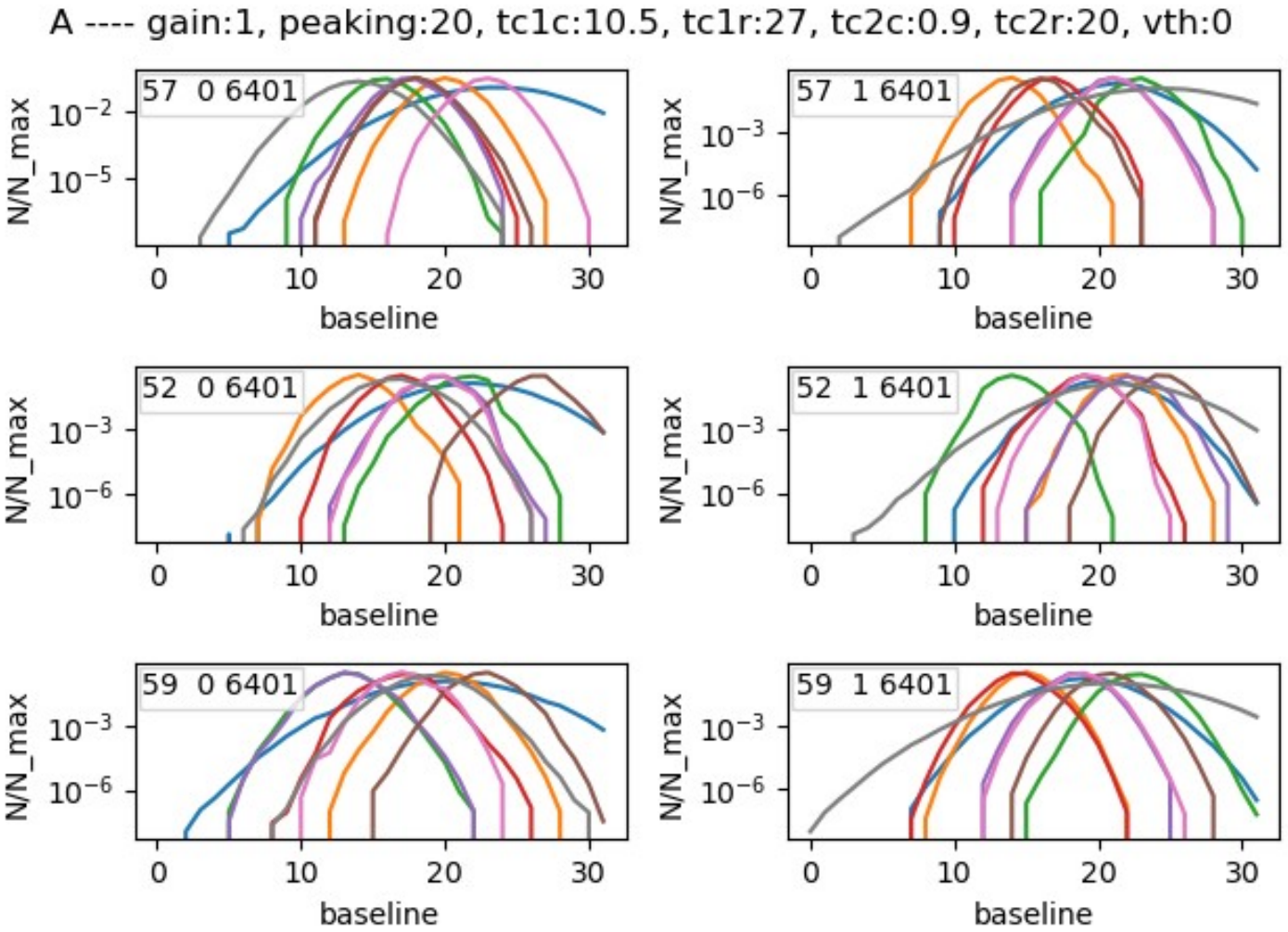
Findings I – boards with “bad” channels



Findings II – boards with “bit” problem ?



Findings III – not so “nice” boards



Baseline scans results

- all boards tested
- 3 boards with one “bad” channel
- 3–6 boards with “bit” problem?
- no differences seen between old and new TDC firmware
- 6 “bad” boards – no spare boards

- values for baseline correction dose not depend on shaping setting !!! (+/-1)

Firmware modification for straws

Goal:

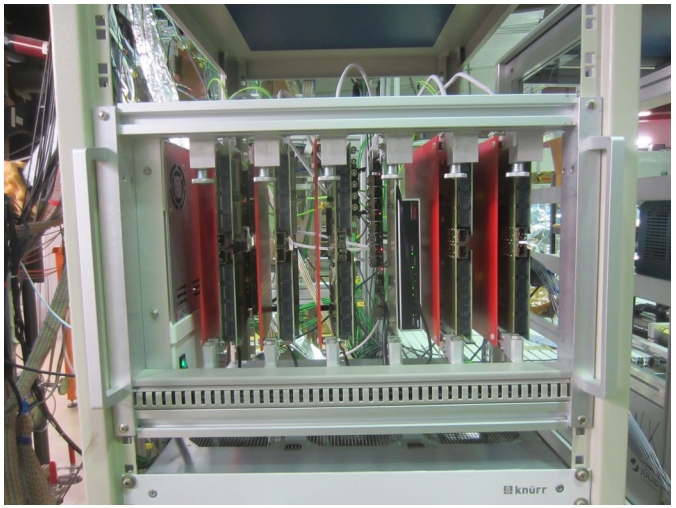
- use TRB3 trigger possibilities for straw tests
- self “straw” trigger
- coincidences between planes, or in plane
- multiplicity per TDC

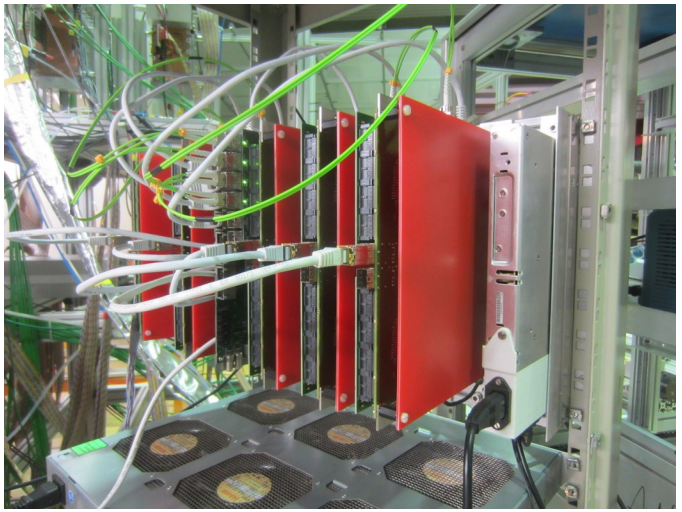
What to do:

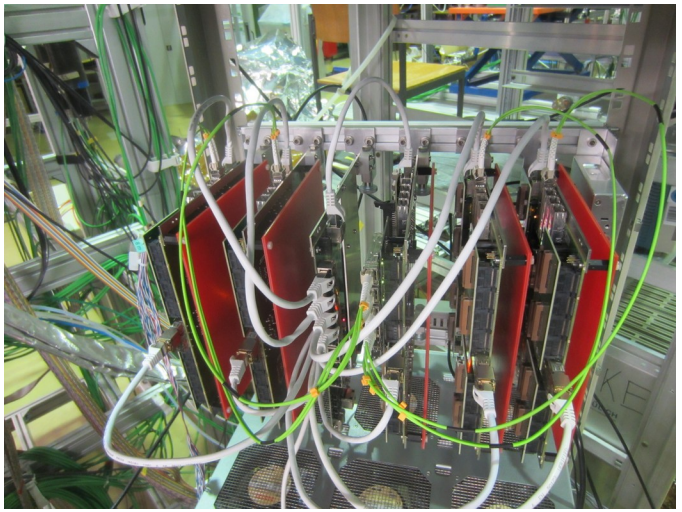
- increase gates and coincidences length to 630 ns for CTS, central FPGAs
- extend number of trigger outputs from each TRB board to 4
- new TRB crate organization

Many thanks to Jan Michel for new firmware's !!!!

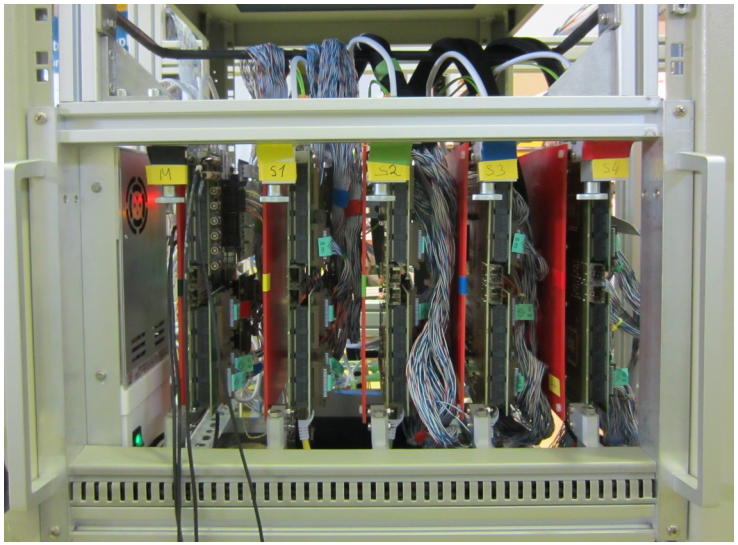
TRB3 crate before modifications

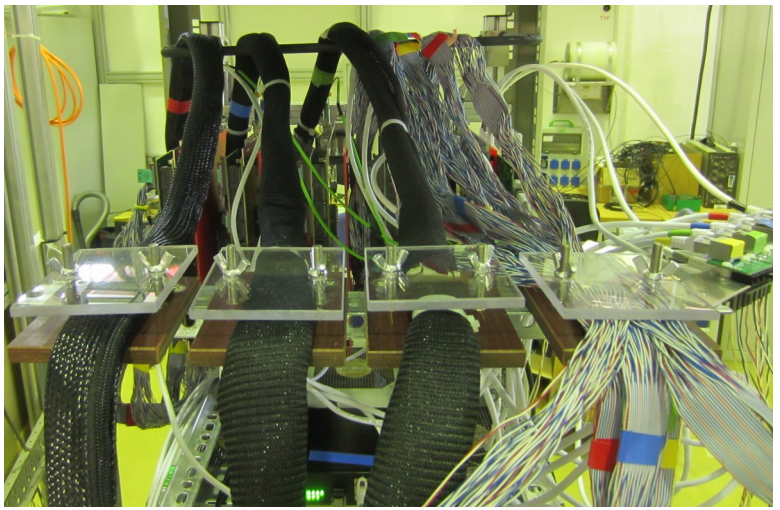


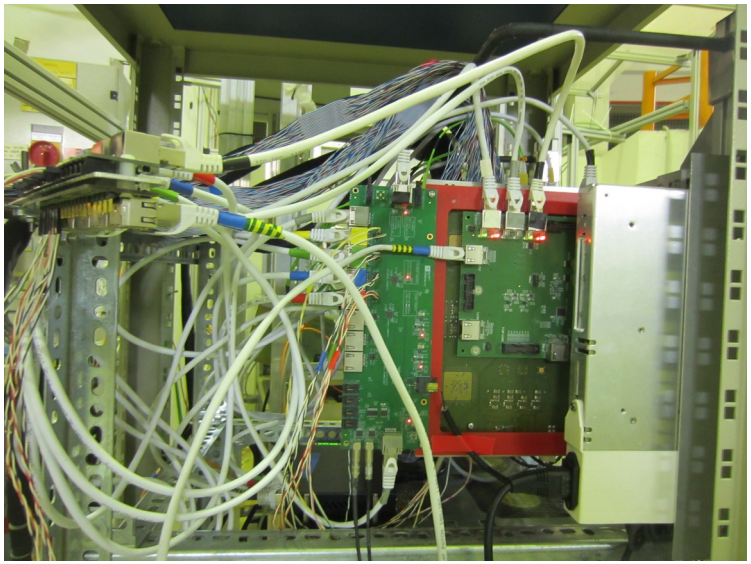


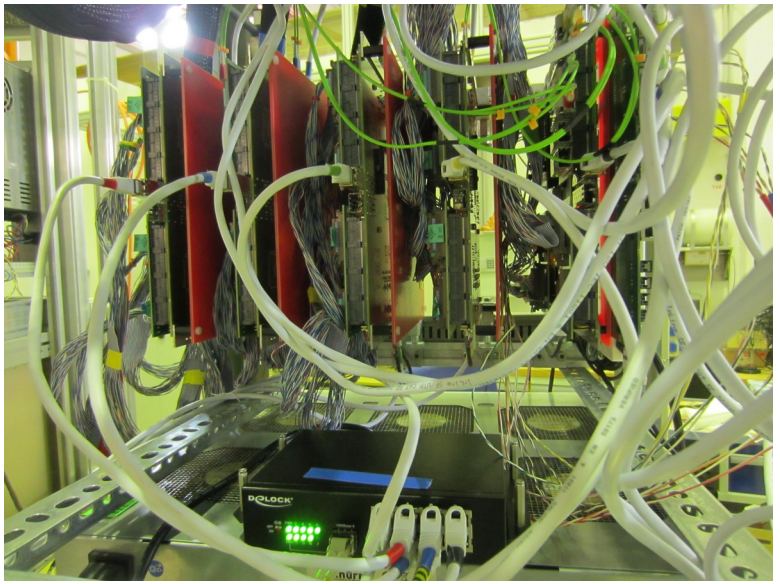


TRB3 crate after modifications I

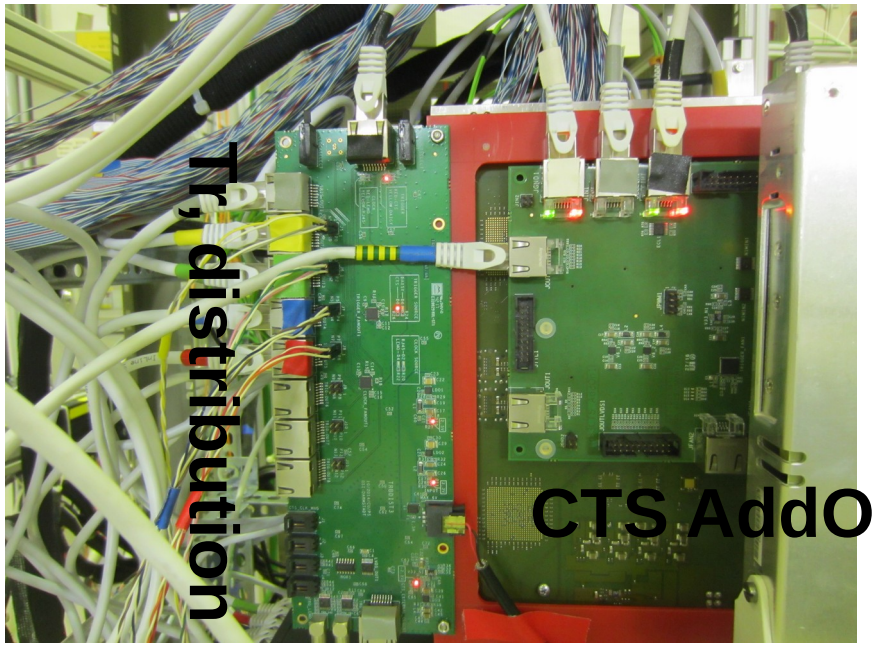


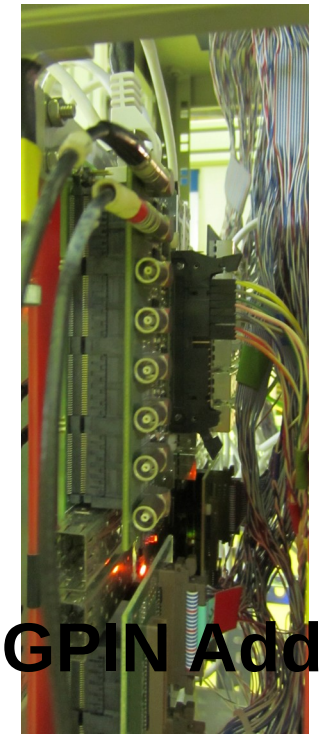


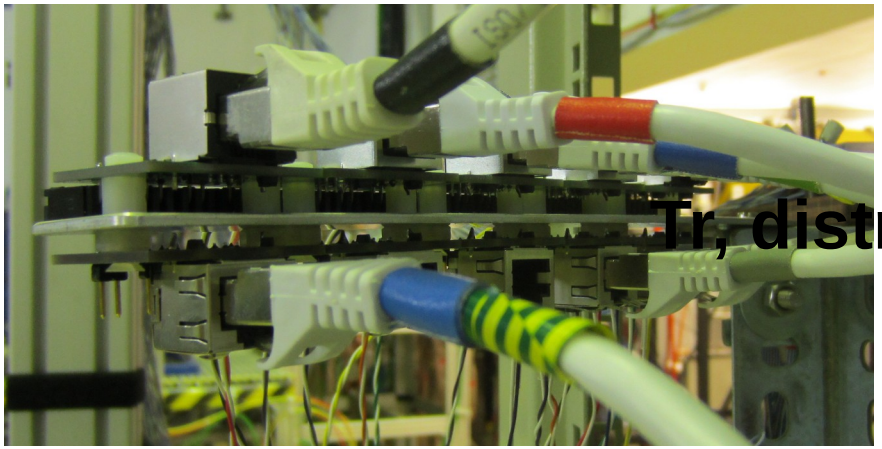


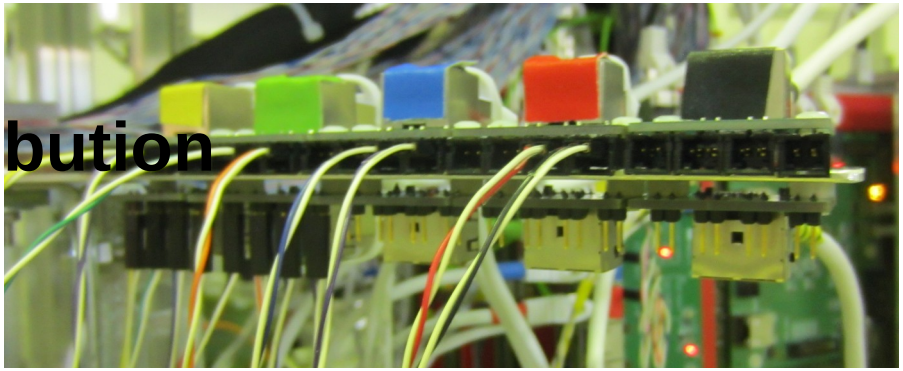


TRB3 crate after modifications II









Summary

Front end free sADC readout
- **new ampl. boards ready**
- **ampl. board with ampl. factor 1**
- **board for direct signal coupling**

STS1 TRB3 readout
- **all PASTTREC boards tested**
- **baseline corrections for all boards (shaping independent)**
- **adapter board for individual ASIC channel test**
- **new firmwares adjusted for straws (Jan Michel)**
- **readout crate prepared for “TRB3 triggering”**

Tanja Hahnraths-von der Gracht, Thomas Sefzick, Lioubov Jokhovets, Artur Derichs, Michael Holona, Valery Serdyuk, James Ritman, Peter Wintz, Jan Michel

Thank you