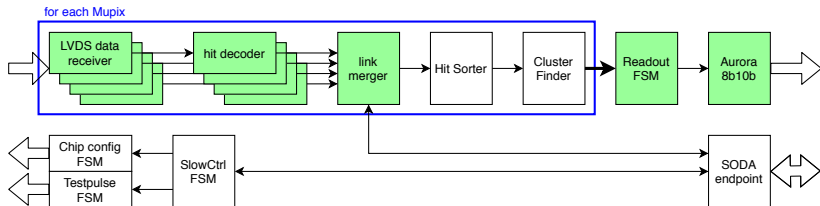# Data Aquisition for the PANDA LMD Prototype

**PANDA CM 20/2**

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# MuPix8 Readout



- MuPix8 read out via 4 LVDS links
- Self triggered with 0 suppression
- Configuration via SPI-like interface
- Readout via Kintex7 FPGA
  - ▶ Final detector: readout board from P. Marciniewski
  - ▶ Prototype: Kintex7 Evaluation Board
- Each FPGA connected to 8 MuPix chips

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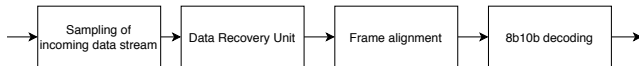
# LVDS Data Receiver



- Asynchronous data stream from MuPix
- Using 4x Oversampling
- Data recovery based on Xilinx XAPP1112
- Recovered data and real data might be phase shifted by up to 9 bit
⇒ Search for Komma words for frame alignment
- 8b10b decode received frames

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# Hit decoder and Link merger

- Remove unneeded data from the stream (e.g. Link ID)
- Decode Timestamp information (Gray counter $\rightarrow$ binary)
- Convert RAM address of pixel into physical address
- Link merger merges the 4 independent data streams of one mupix into one data stream

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# Hit Sorting and Custerfinding

- In each frame from MuPix only one hit per column can be processed
- Hits in "lower" rows are preferred
- Hits are not sorted by time
- Need to sorted by time to simplify cluster search and tracking
- Clusters occure due to charge sharing of neighbouring pixels from single hit
- Need to be identified and treated as single hit for tracking (weighted by charge)

# Complete Readout Chain

For the LMD prototype at CoSy
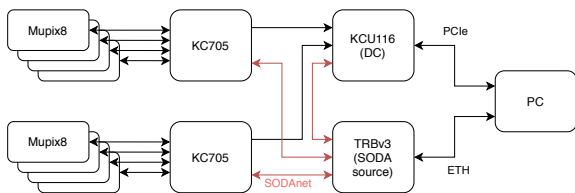


- Two Kintex7 Eval boards (KC705) reading out 8 MuPix sensors each
- Kintex Ultrascale+ Eval board (KCU116) as data concentrator
- TRBv3 as SODA source
- Data from Kintex7 to Kintex US+ via optical links (Aurora8b10b)
- From Kintex US+ to PC via PCIe (DMA IP from Xilinx)

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# To Do List for the Protopye DAQ

- Some parts of our firmware still missing (hit sorting, cluster finder)
  Can be done offline
- SODA needs to be integrated in our DAQ
  SODAnet endpoint code for KC705 provided by P. Schakel (KVI)
- FMC adapter board to connect MuPix sensors to KC705 with 2nd SFP connector
- Configuration of MuPix chip via KC705 has to be tested
- Communication with PC via DMA/PCIe needs to designed and tested

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