ToASt ASIC development update

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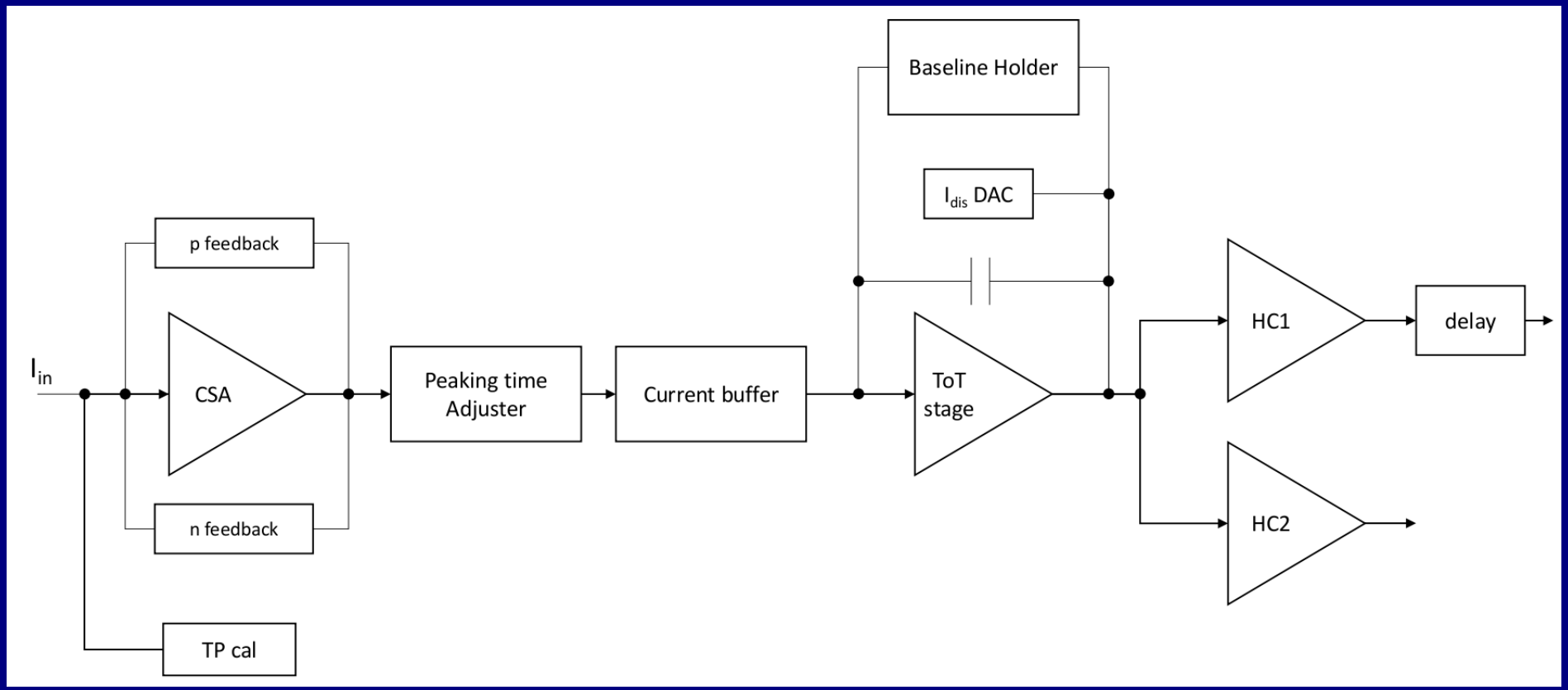
Specifications

Specification	Min	Max	Unit
Input capacitance	2	17	pF
Max rate per strip		40	kHz
Input charge	1	40	fC
Noise		1500	e^-
Preamp peaking time	50	$\geq$ 100	ns
Channels per chip	64		
Reference clock		160	MHz
Charge resolution	8		bits
Time resolution (pk-pk)		6.25	ns
Time resolution (r.m.s.)		1.8	ns
Power consumption		256	mW
Chip dimensions	4.2 $\times$ 3.5		mm^2
Pads position	On two sides only		

ToASt analog FE

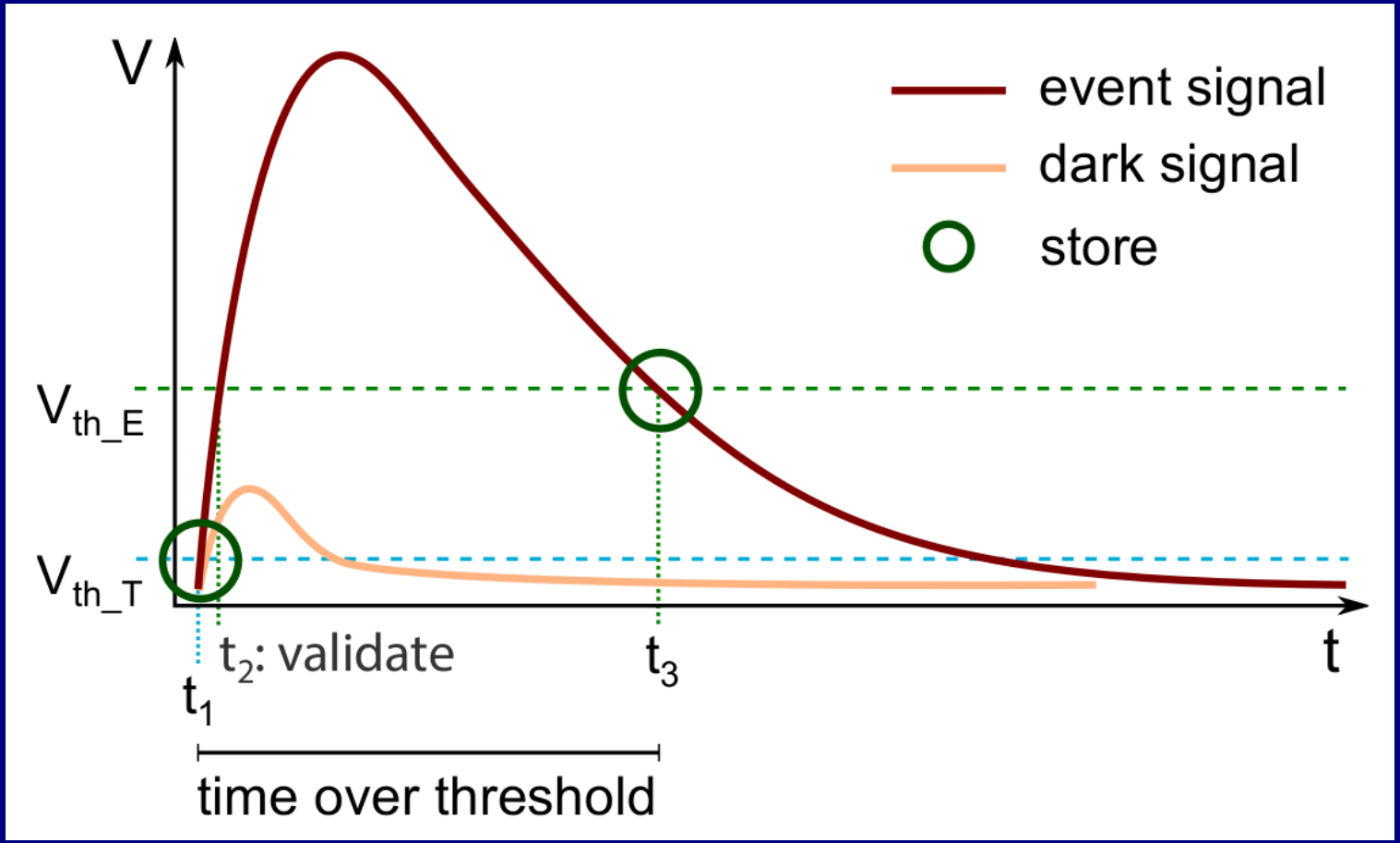


- Polarity 0 : n-type strip detector
- Polarity 1 : p-type strip detector

Front-end architecture

- *Preamplifier*: first amplification of signals coming from n- and p-type strips
- *Peaking Time Adjuster*: increase signals peaking time and combine two polarities
- *Current Buffer*: main charge amplification
- *ToT Stage*: constant discharge current to ensure the linearity of the ToT measurement
- *Hysteresis Comparator*: events discrimination with hysteresis (2 discriminators for each channel)

Double threshold logic

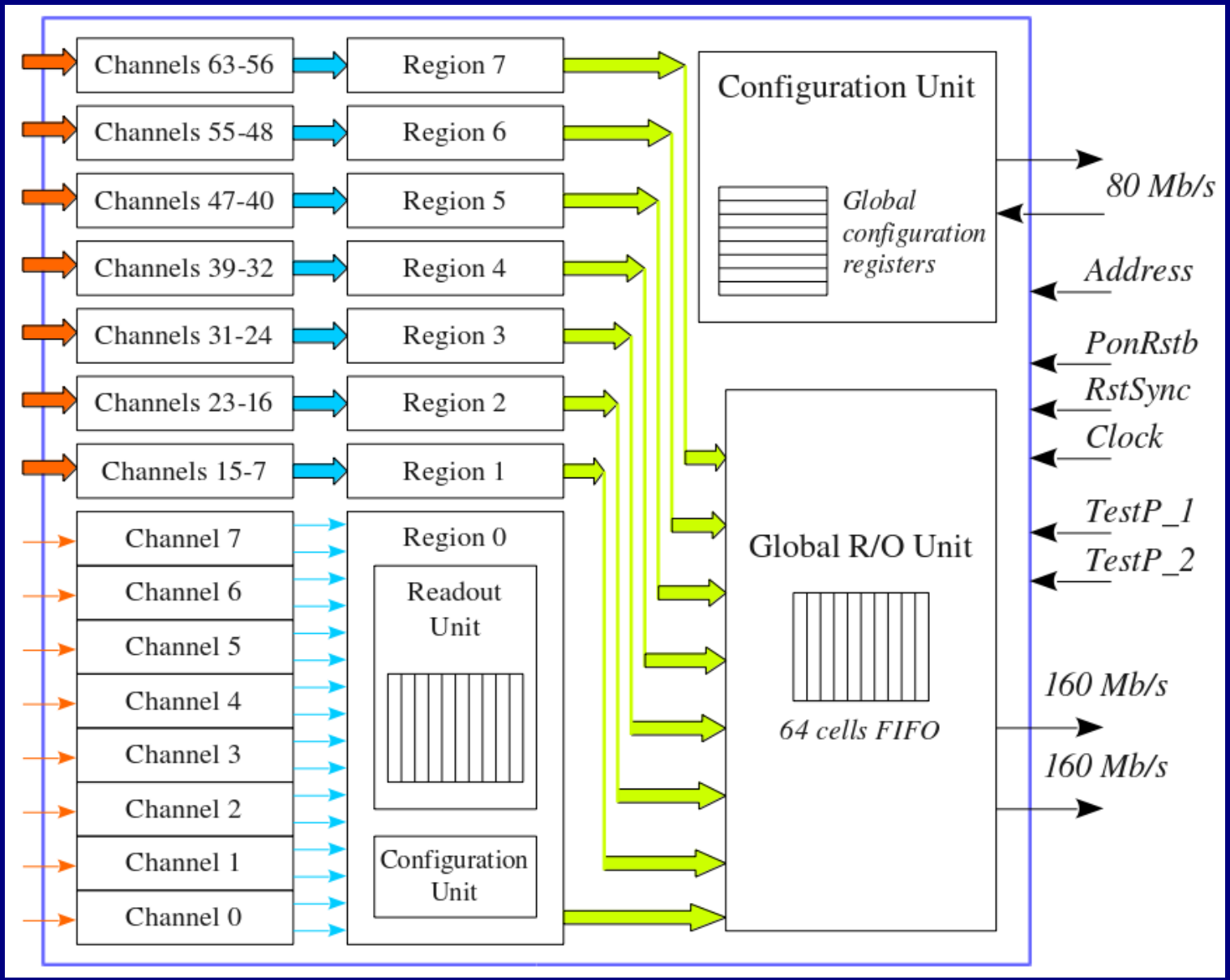


- Leading edge time measured on time threshold *(to minimize jitter)*
- Event acquired only if crosses the energy threhsold *(to minimize noise events)*

ToASt main characteristics

- 64 input channels
- Time of Arrival (ToA) and Time over Threshold (ToT) measurements
- Master clock frequency : 160 MHz
- Region : groups of 8 channels with local FIFO
- Second level FIFO buffering for the 8 regions
- Two output serial links at 160 Mb/s
- Serial configuration protocol at 80 Mb/s
- SEU protection for registers and FSM
- CMOS 0.11 μm technology

ToASt architecture



ToASt pinout *(preliminary)*

Pin name	Direction	Description
in[63:0]	In	Analog inputs
pon_rst	In	Power on asynchronous reset
SyncReset	Rx	Synchronous reset
ChipAddr[6:0]	In	Chip address
TestPulse	In	Digital test pulse
CfgRx	Rx	Configuration receiver
CfgTx	Tx	Configuration transmitter
TxOut_0	Tx	Data serial output 0
TxOut_1	Tx	Data serial output 1

Output data format

- Data output in 32 bits words over 160 Mb/s serial links
- It can be configured to use 1 or 2 links

Packet type	Header *2 bits*	Data *30 bits*
Data	01	Region[2:0] Channel[2:0] Le[11:0] Te[11:0]
Header	00	11 ChipId[6:0] Reserved[12:0] FrameN[7:0]
Trailer	11	00 DataCnt[11:0] CRC[15:0]
Sync	10	01 1001 0110 0110 1001 1001 0110 0110

Control unit

- Serial link at 1/2 of the master clock frequency
- Input : 16 bits command
- Output : 16 bits data
- Address :
  - a_B : broadcast address
  - $a_6 a_5 a_4 a_3 a_2 a_1 a_0$: chip address
- 14 12-bits Global Control Registers (GCR)
- 64×2 12-bits Channel Control Registers (CCR)

Control data format - 1

Function	**Data** 4 bits	**Op code** 12 bits
Chip Select	1101	$01a_B a_6 a_5 a_4 a_3 a_2 a_1 a_0 00$
Chip Deselect	0000	00xx xxxx xxxx
Register select (channel)	0100	$0000 r_2 r_1 r_0 0 c_2 c_1 c_0 a_0$
Register select (region)	0100	$0000 r_2 r_1 r_0 1 a_3 a_2 a_1 a_0$
Register select (global)	0100	$00010 a_6 a_5 a_4 a_3 a_2 a_1 a_0$
Register write	0101	$d_{11} d_{10} d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0$
Register read	0110	0000 0000 0000
No operation	1111	0000 0000 0000
Reserved for config output	1000	$d_{11} d_{10} d_9 d_8 d_7 d_6 d_5 d_4 d_3 d_2 d_1 d_0$

Control data format - 2

The addresses are interpreted as follows :

- GCR write : $\mathrm{d_{11}d_{10}d_9d_8d_7d_6d_5d_4d_3d_2d_1d_0}$ is the 12 bit data to be written in the register
- Region and channel select : $\mathrm{r_2r_1r_0}$ is the region address
- Channel select : $\mathrm{c_2c_1c_0}$ is the channel address
- Channel select : $\mathrm{a_0}$ selects DAC_If register (0) or DAC_th registers (1)
- Channel write : if DAC_If is selected, $\mathrm{d_4d_3d_2d_1d_0}$ is written in the DAC_If channel register. if DAC_th is selected, $\mathrm{d_9d_8d_7d_6d_5}$ is written in the DAC_thE register and $\mathrm{d_4d_3d_2d_1d_0}$ is written in the DAC_thT register.

The received command is re-sent out from the serial output.
Important note : after a read command the configuration unit is not ready to accept another command until the read output word has been sent out. Idle codes have to be inserted to avoid the reset of the link.

Control registers

- Channel registers :
  - Channel mask
  - Calibration enable
  - Time and energy threshold DACs for fine tuning (5 bits)
  - ToT discharge current calibration DAC (5 bits)
- Global registers :
  - GCR0 : global settings :
    - Detector polarity, leading edge only and single threshold modes
    - Drivers enable
    - Frame and time stamp counters control
  - GCR1 : region enable
  - GCR2-13 : global DAC controls for :
    - FE bias
    - Global threshold setting
    - Global ToT discharge current setting

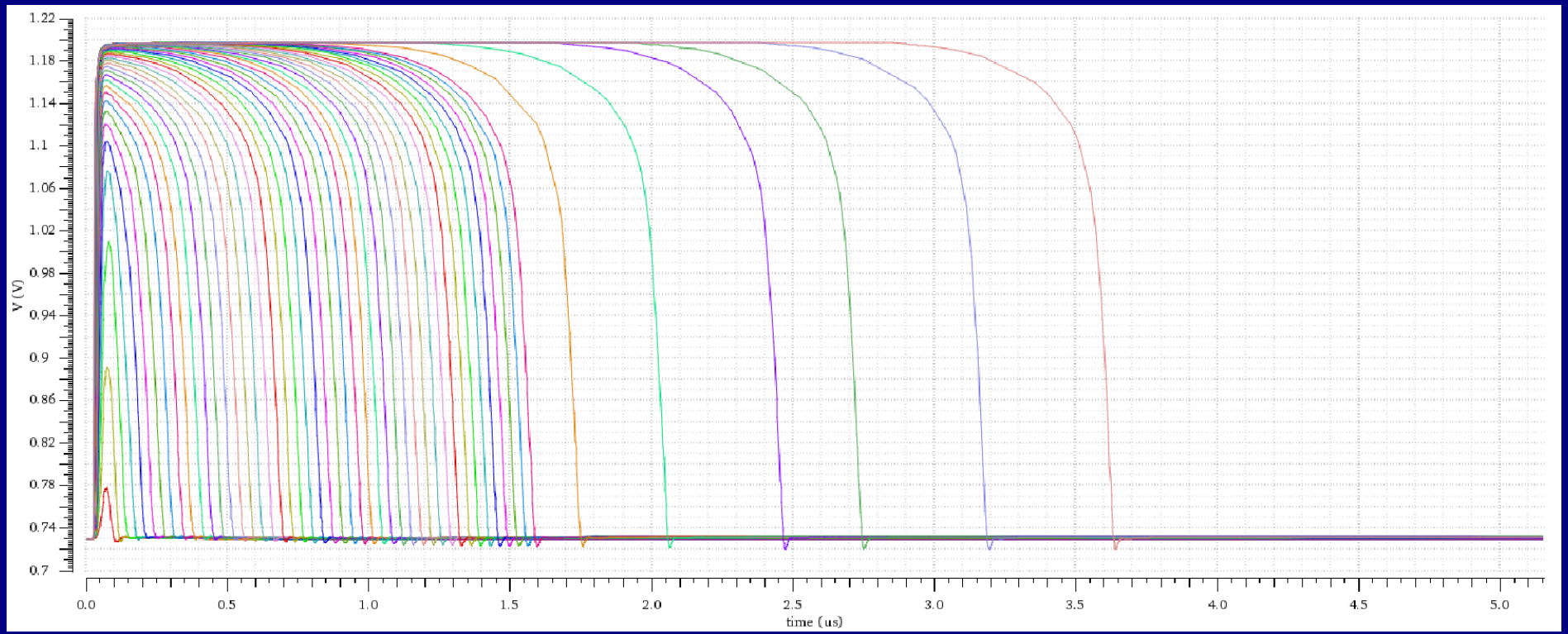
Reset management

- Asynchronous power-on reset : for start-up only
- Synchronous, pulse lenght encoded reset :
  - 1 clock cycle reset pulse : ignored
  - 2 clock cycles reset pulse : a time stamp reset is generated
  - 3 clock cycle reset pulse : ignored
  - n$\geq$4 clock cycles reset pulse : both global and time stamp reset are generated.

Analogue front-end status

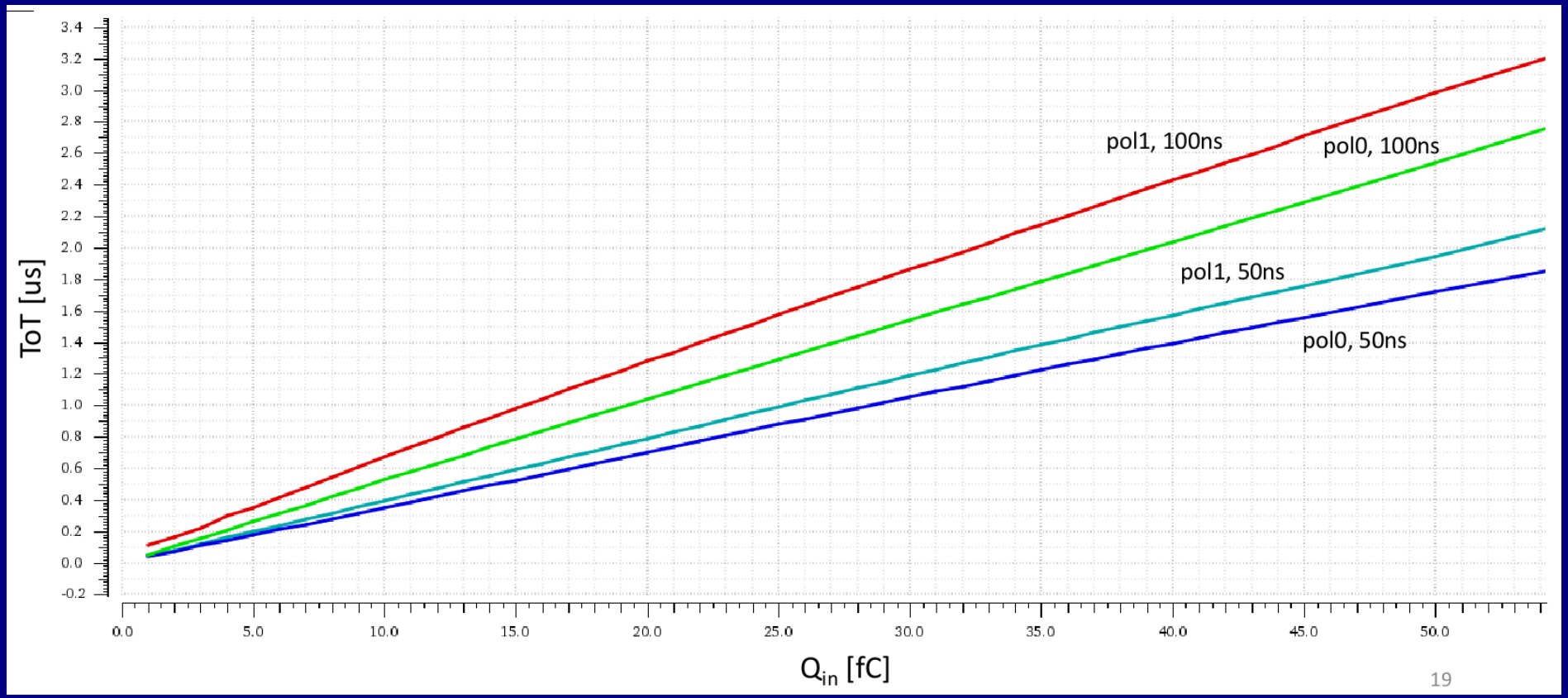
- Significantly larger modification required with respect to original plans
- Power distribution requires significant improvement :
  - Cell level : power lines moved to upper layers
  - Chip level : replace ME7 with ME8 on vertical power distribution for minimum resistance
  - Pad level : test only power pads on top and bottom.
- Full review of analog chain ongoing :
  - FE bias bug correction and internal DAC control added
  - Improvement of the performances at low charges
  - Review of the peaking time requirements w.r.t. the FE modifications
  - Replacement of the differential comparator with a single-ended one
  - Two test pulse capacitors :
    - Small cap for fine ToT characterization at low charges
    - Large cap for coarse ToT characterization at full range

Example of simulations : Vout vs charge



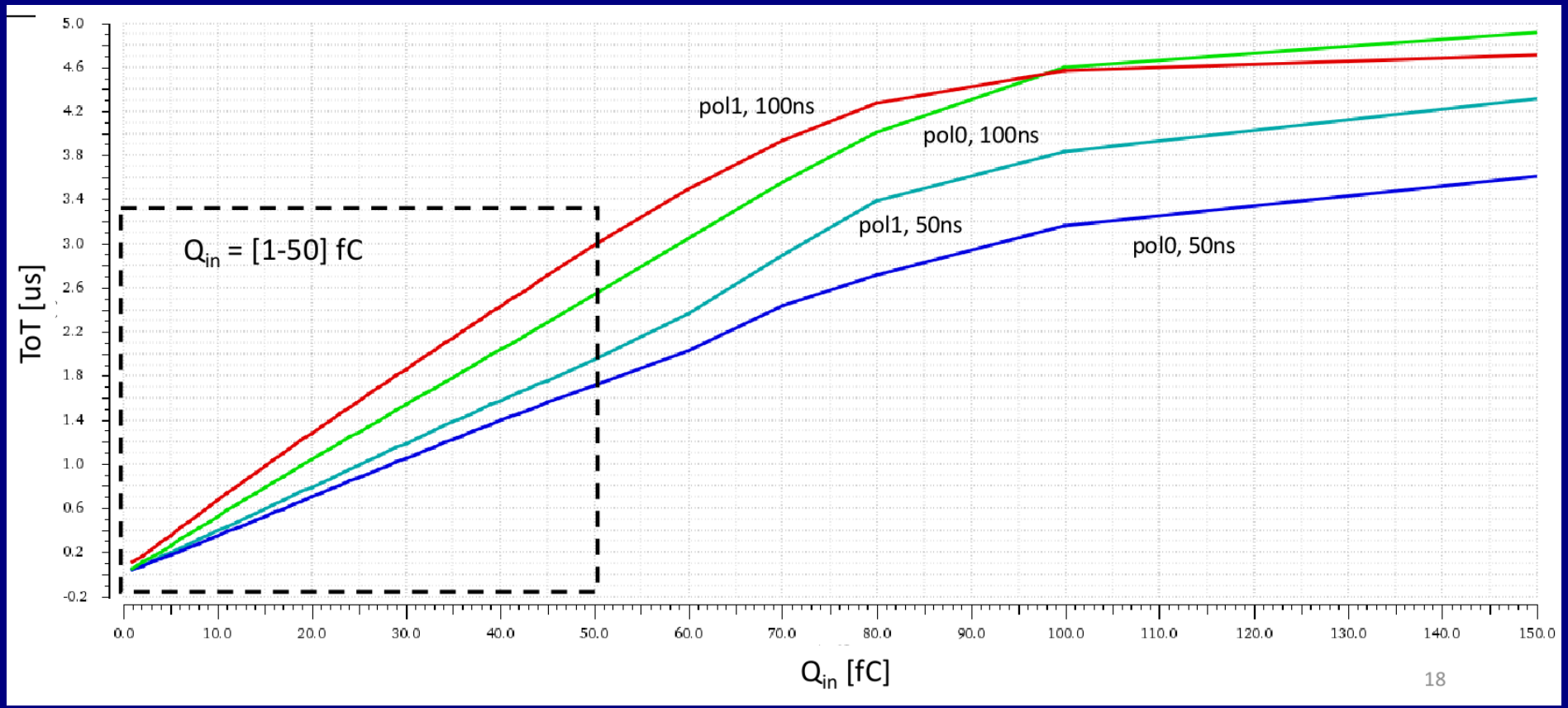
- Q_{IN} = [1-45] fC + (50, 60, 70, 80, 100, 150) fC
- Peaking time 50 ns
- Polarity 0

ToT vs charge (range [1÷60 fC)



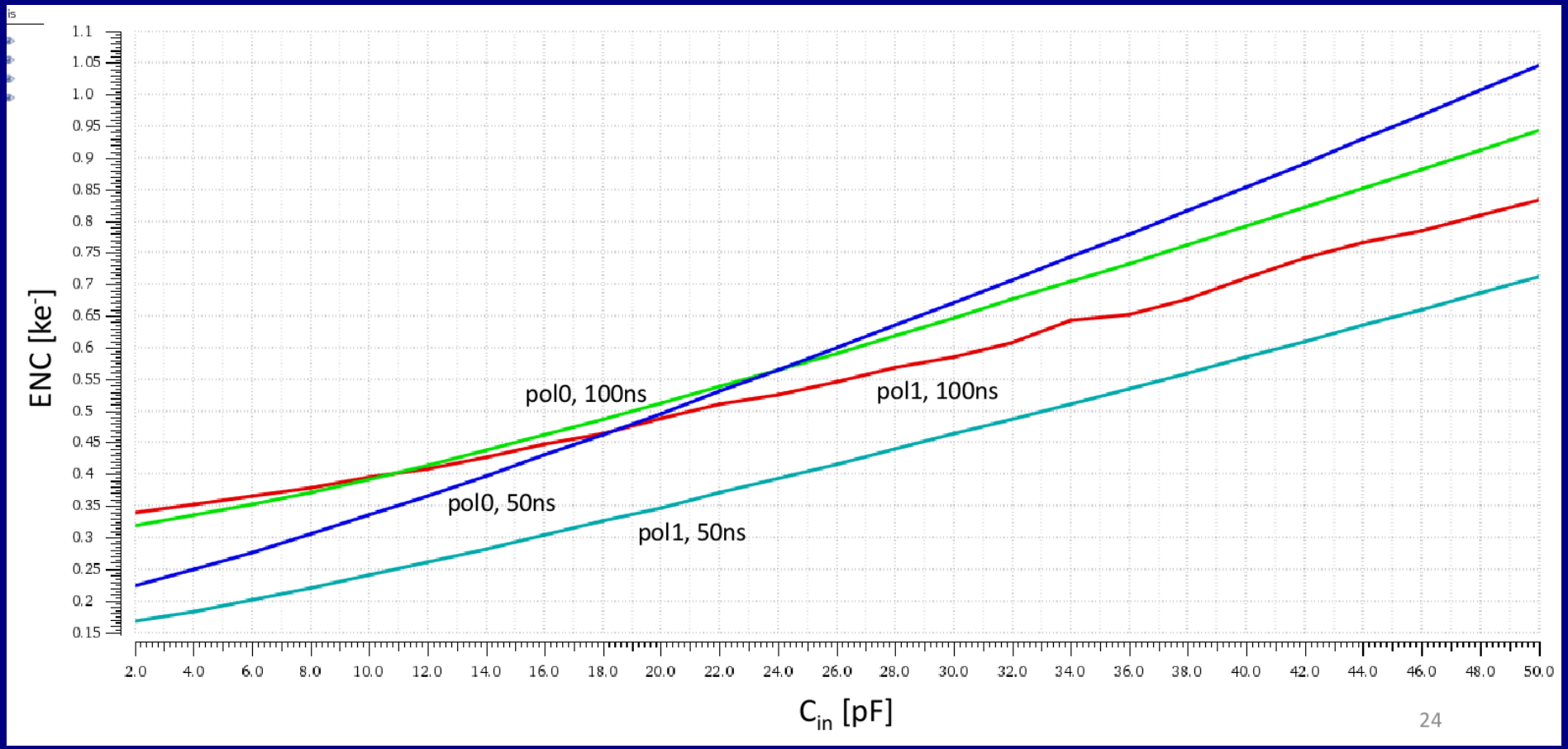
- ToT still linear despite FE saturation

ToT vs charge (up to 150 fC)



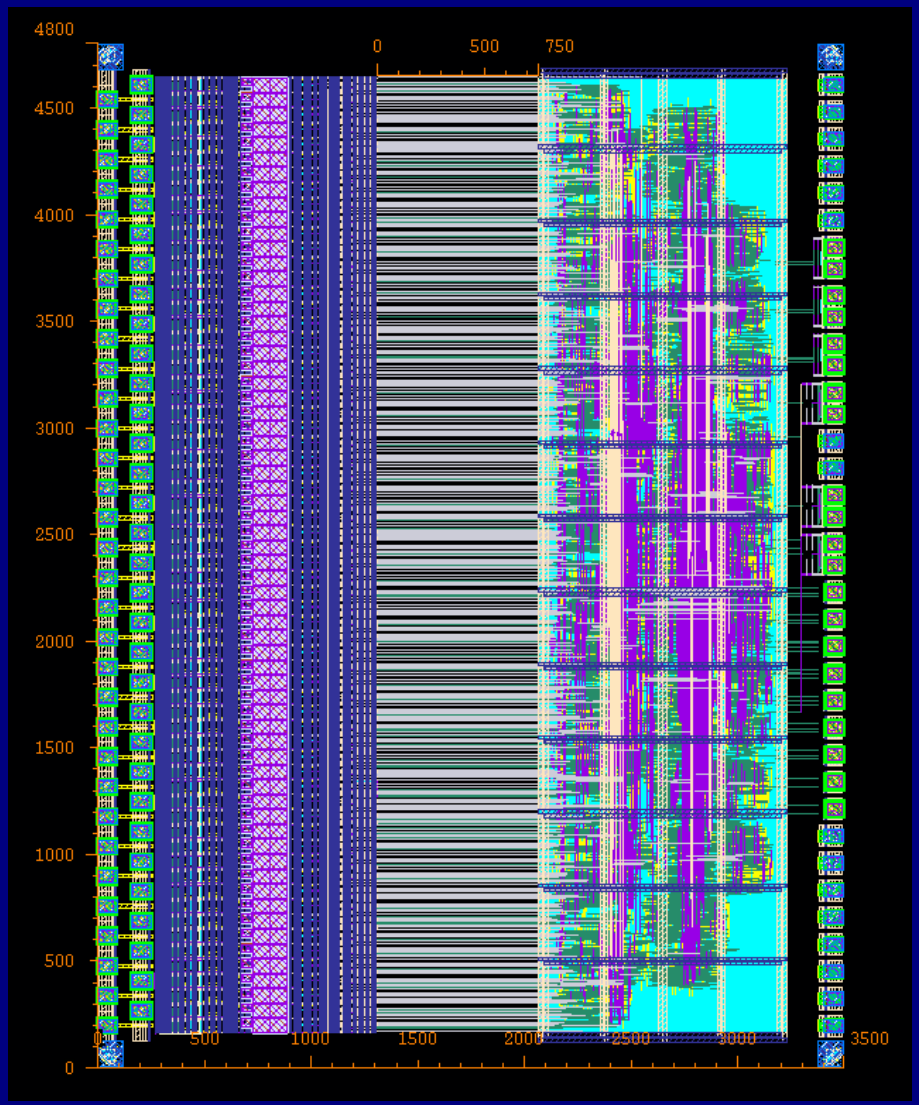
- ToT saturation
- FE not stuck by very large charges

Example of simulations : ENC vs charge



- With longer peaking times, both signal and noise are reduced
- No significant advantage for the elettronics *(not necessarly true for the detector)*

First ToASt layout



- Digital-on-top design flow
- Same size as PASTA
- PASTA analog layout (ToASt analog layout not yet available)
- ToAST digital layout
- Some space available for FE improvement

Summary

- Development for the PANDA MVD strip detector :
  - 64 channel ASIC
  - Configurable for both input signal polarities.
  - Time of Arrival measurement with system clock resolution
  - Charge measurement via Time over Threshold
  - Local FIFOs for data de-randomization
  - 2×160 Mb/s serial outputs
- BE design : signoff and final verifications ongoing
- FE design : optimization ongoing

Spare slides

Channel Control Registers

Register	Bits	Function
0	11:8	*Reserved for future use*
0	7	Channel mask
0	6	Delay enable
0	5	Calibration enable
0	4:0	ToT discharge current calibration DAC
1	11:10	*Reserved for future use*
1	9:5	Energy threshold calibration DAC
1	4:0	Time threshold calibration DAC

Global Control Registers 0-1 - *preliminary assignment*

GCR0 bit assignment	
Bit	**Function**
11	*Reserved for future use*
10	detector polarity
9	leading edge-only mode
8	single threshold mode
7	*Reserved for future use*
6	Frame counter reset
5	Tx 1 enable
4	Tx 0 enable
3:2	*Reserved for future use*
1	Time stamp counter Gray mode
0	Time stamp counter enable

GCR1 bit assignment	
Bit	**Function**
11:8	*Reserved for future use*
7	Region 7 disable
6	Region 6 disable
5	Region 5 disable
4	Region 4 disable
3	Region 3 disable
2	Region 2 disable
1	Region 1 disable
0	Region 0 disable

Global Control Registers 2-7 - *preliminary assignment*

Register	Bit	Function	Default
GCR2	11:10	*Not used*	00
GCR2	9:5	CSA Ibias	01101
GCR2	4:0	CSA source followers Ibias	10111
GCR3	11:10	*Not used*	00
GCR3	9:5	Preamp feedback pMOS Ibias	01110
GCR3	4:0	Preamp feedback nMOS Ibias	01110
GCR4	11:10	*Not used*	00
GCR4	9:5	Preamp Ishift	10001
GCR4	4:0	PTA Ibuf	10101
GCR5	11:10	*Not used*	00
GCR5	9:5	PTA pMOS Ibias	01110
GCR5	4:0	PTA nMOS Ibias	01110
GCR6	11:10	*Not used*	00
GCR6	9:5	CB Ibias 1	01110
GCR6	4:0	CB Ibias 2	10101
GCR7	11:10	*Not used*	00
GCR7	9:5	CB Vbias	01010
GCR7	4:0	ToT Ibias	01110

Global Control Registers 8-13 - *preliminary assignment*

Register	Bit	Function	Default
GCR8	11:10	*Not used*	00
GCR8	9:5	BLR Ibias	11110
GCR8	4:0	BLR Vcas	10110
GCR9	11:10	*Not used*	00
GCR9	9:5	HC Ibias 1	01000
GCR9	4:0	HC Ibias 2	01110
GCR10	11	*Not used*	00
GCR10	10:6	HC Ibias 3	01000
GCR10	5:0	Baseline Vbias	011111
GCR11	11:8	*Not used*	0000
GCR11	7:4	HC DAC threshold bias +	1111
GCR11	3:0	HC DAC threshold bias -	1001
GCR12	11:10	*Not used*	00
GCR12	9:5	ToT Ifb DAC Ilsb	01101
GCR12	4:0	ToT Ifb DAC Imin	10101
GCR13	11:6	*Not used*	00
GCR13	5:0	Ib calibration	000000