Status of PASTTREC ASIC tests

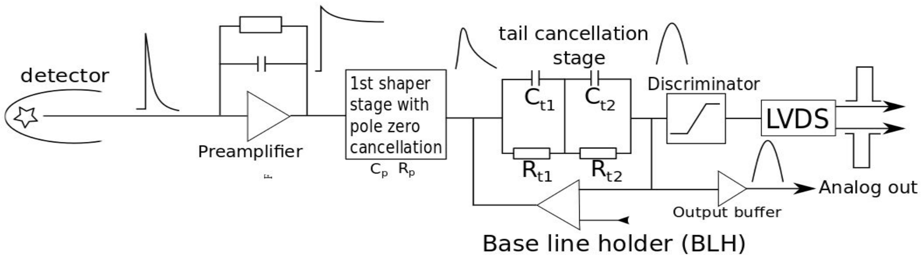
A. Malige
akshay.malige@doctoral.uj.edu.pl

PANDA Collaboration meeting
June 2020

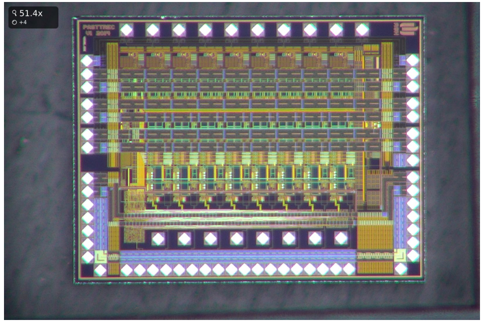
23 - 06 - 2020

Front-end electronics

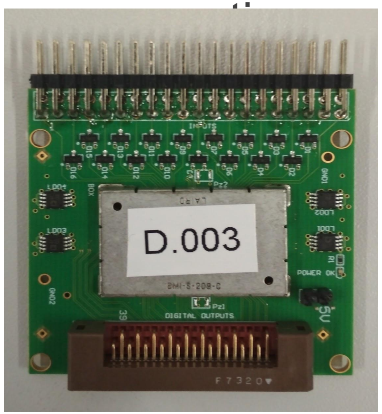
- ➢ The FEE card contains two 8-channel PASTTREC chips (D.Przyborowski et al.,JINST_013P_0516. (2016))



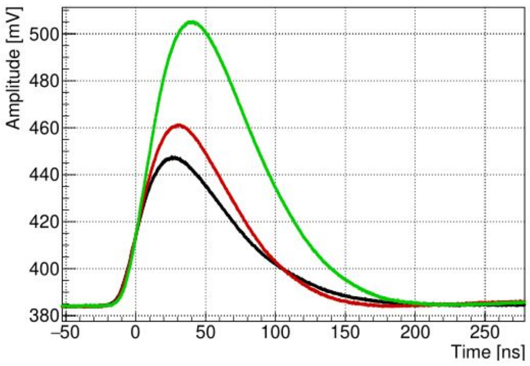
Schematic representation of the front end electronics functions with a concepts of signal shaping with analog circuitry.



- ➢ Signal shaping, ion-tail cancellation using CR-RC , discriminator for signal



Waveform



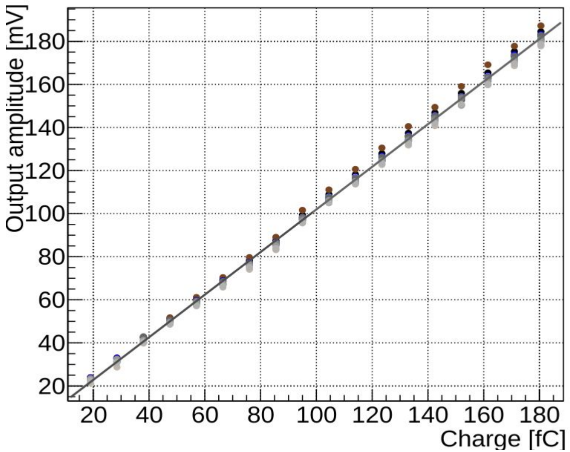
Settings

black: $TC_{C1} = 10.5pF$, $TC_{R1} = 27k\Omega$, $TC_{C2} = 0.9pF$, $TC_{R2} = 20k\Omega$;
red: $TC_{C1} = 6pF$, $TC_{R1} = 23k\Omega$, $TC_{C2} = 0.6pF$, $TC_{R2} = 11k\Omega$;
green: $TC_{C1} = 16.5pF$, $TC_{R1} = 11k\Omega$, $TC_{C2} = 0.9pF$, $TC_{R2} = 5k\Omega$;

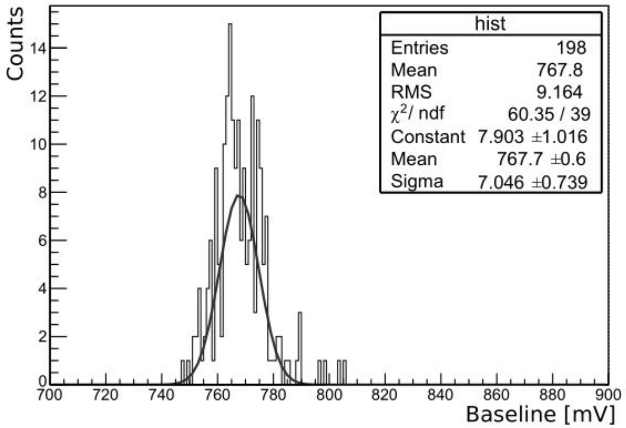
Analogue output for 3 optimal TC settings found for the preamplifier gain K=1 mV/fC, peaking time 20ns,

Goals

- Align baselines to set common disc.threshold (treat all the channels equally)
- Lower noise = lower operational discr.threshold, high time resolution, low operating voltage, slower aging effect (i.e < 6 mV @ Gain 1mV/fC)
- High gain uniformity, baseline position uniformity



Amplitudes of 16 output signals versus input charge for the same ASIC configuration with S.Dev < 1.3%

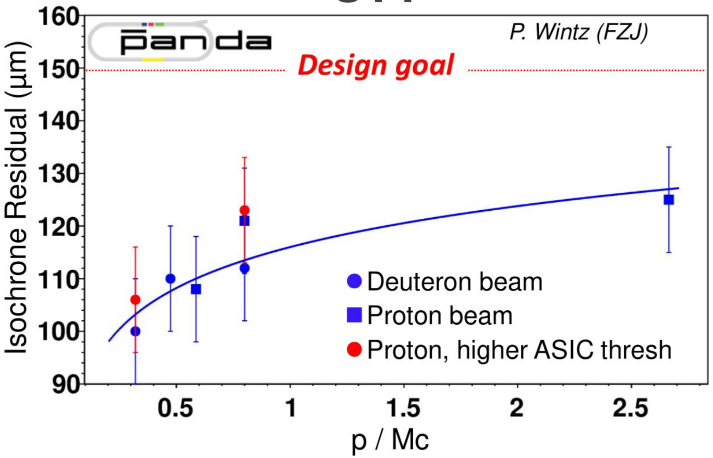


Distribution of the baseline levels accumulated from 198 channels

Design goals

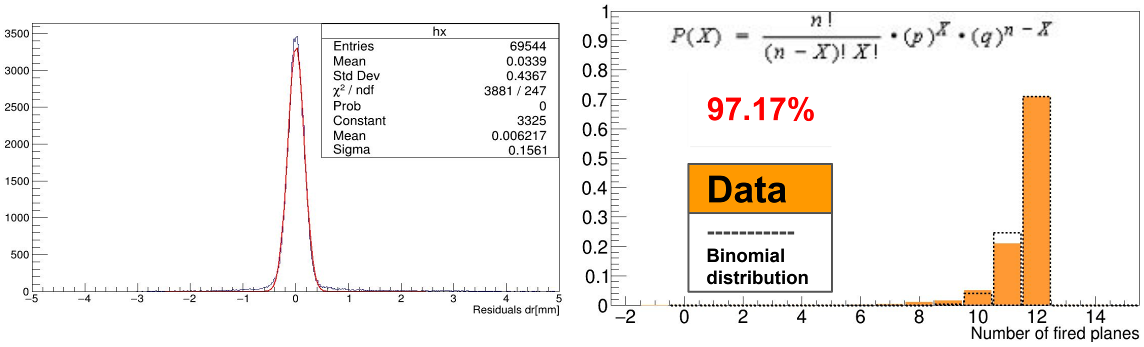
- ➢ Tracking resolution of ~156 um at gain 1mV/fC, 6 mV discr.threshold and Tp 20 ns
- ➢ Results from STT and FT from in beam measurements 2016 / 19
- ➢ PASTTREC – ASIC for STT / FT design goal reached

STT



HV 1800V, Tp 35 ns, Gain 1.8 mV/fC
Spatial resolution as a function of βγ
Courtesy : P.Wintz

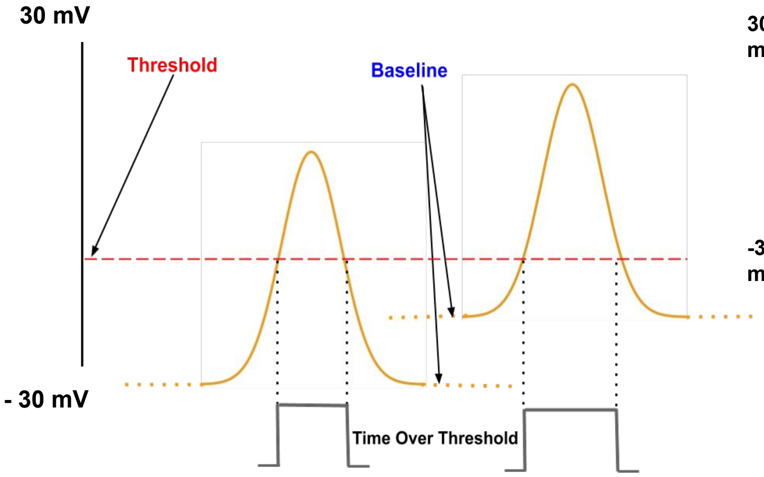
FT

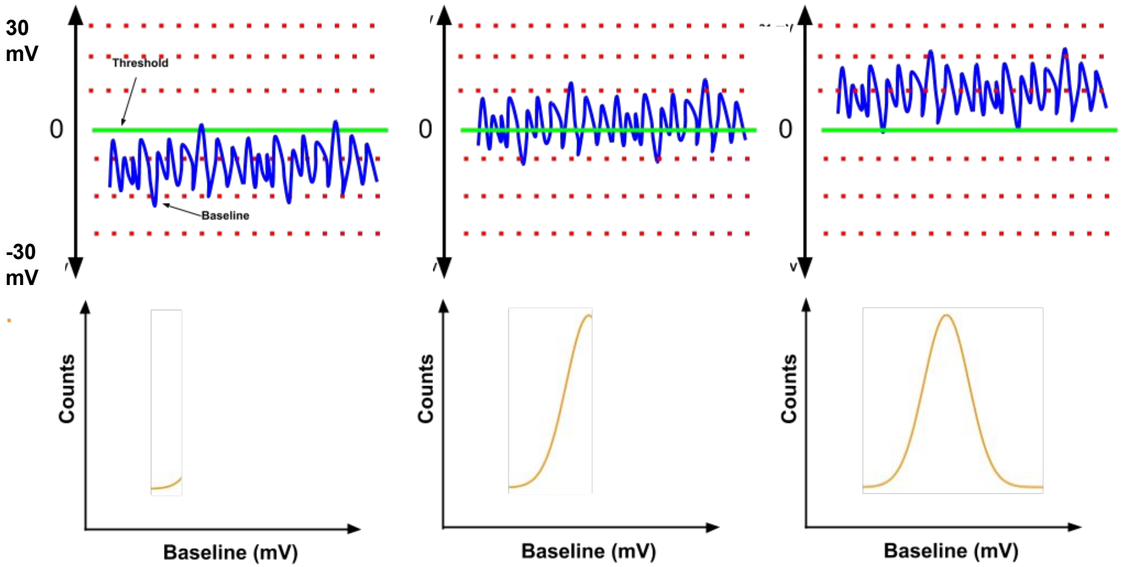


HV 1750, Th 6 mV, Tp 20 ns, GM 90:10
Left: Spatial resolution calculated for tracks in 4 straight layers (0 deg)
Right: Efficiency of the detector for 6 layers when the 1st and the 8th layer is hit.

Baseline Alignment procedure

- Baseline adjustment - 30 mV to + 30 mV (1 LSB = 2 mV)
- Automatic baseline alignment technique developed



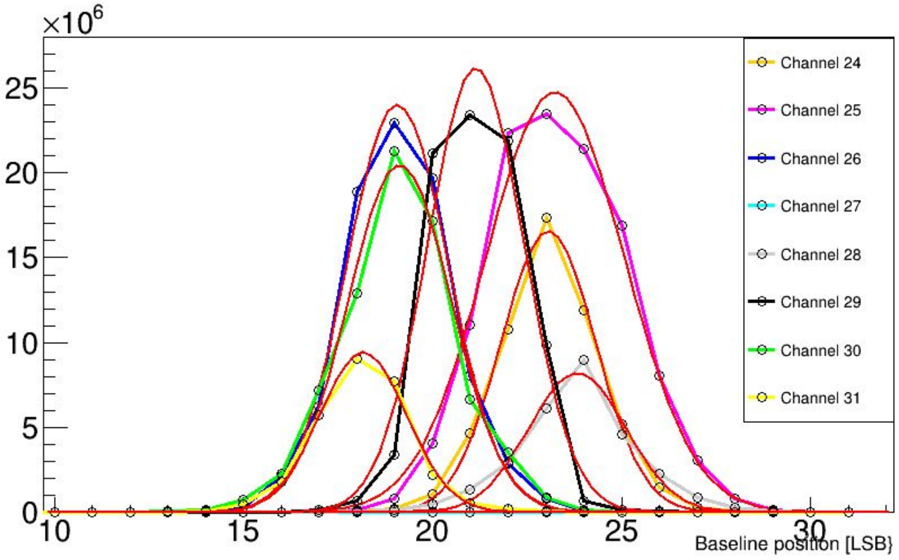


Baseline Alignment procedure

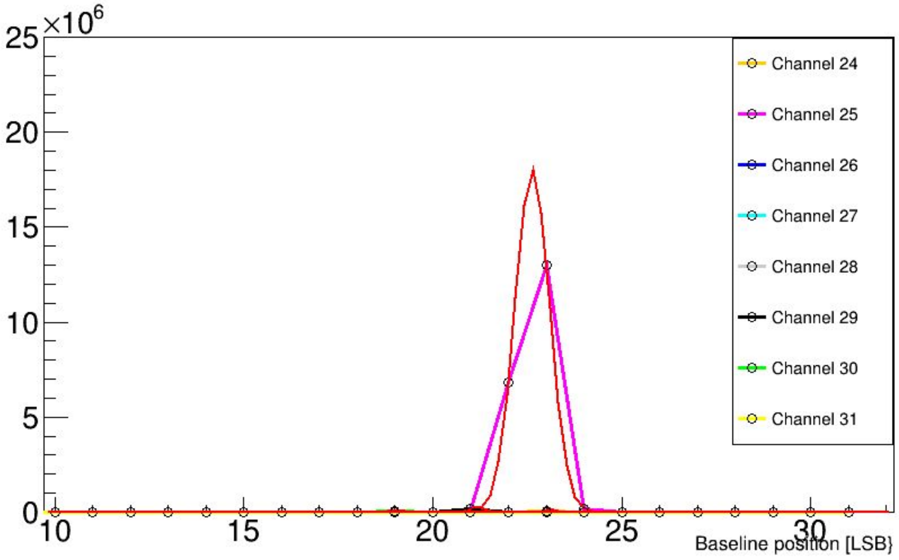
- ➢ Baseline adjustment - 30 mV to + 30 mV (1 LSB = 2 mV)
- ➢ Automatic baseline alignment technique developed

Count profile from a noise scan of 1 asic @ gain 4mV/fC and gaussian fit
(before baseline alignment)

Connected to detector module

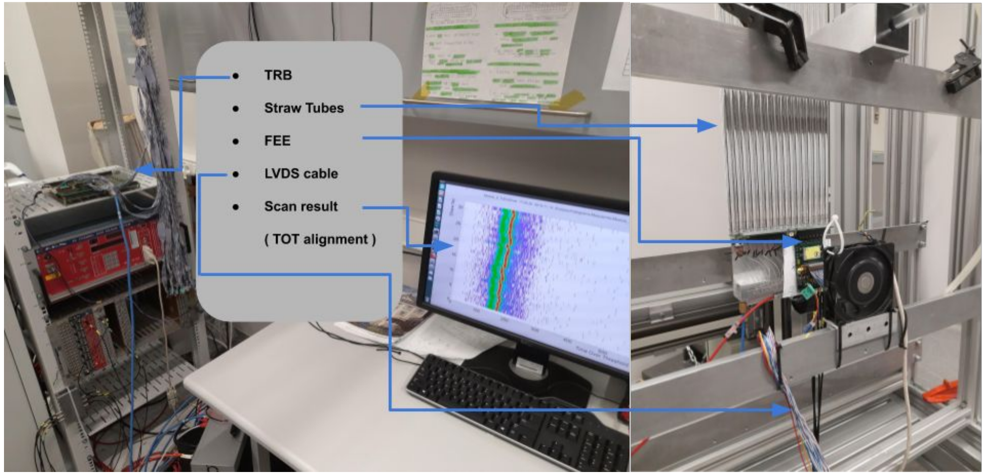


Disconnected from detector module



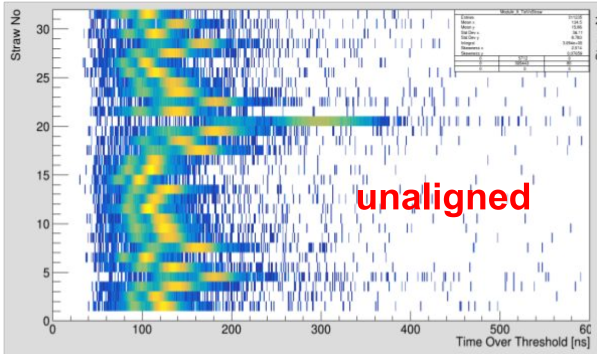
Tests of the ASICS

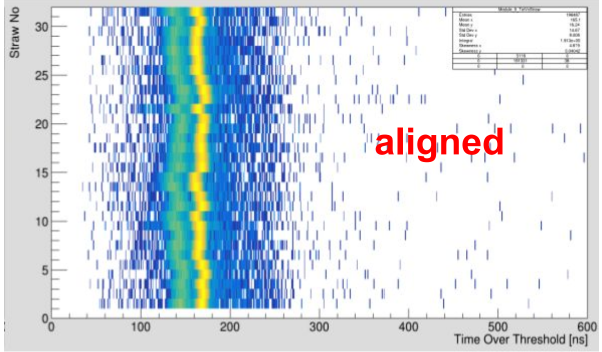
- ➢ Scan made for 1 channel at a time
- ➢ Connected to det.module
- ➢ Noise width determined from gaussian fit over count profiles
- ➢ S-Curve measurement using a pulse generator



- ★ **Two settings :** Gain **4mV/fC**, Peaking time 15ns & 20 ns
- ★ **Software :** Written in Python 3, uses TRBnet interface to communicate with ASICs
- ★ **Repository** : https://github.com/HADES-Cracovia/pasttrectools

Tests of the ASICS





- ➢ Scan made for 1 channel at a time
- ➢ Connected to det.module
- ➢ Noise width determined from gaussian fit over count profiles
- ➢ S-Curve measurement using a pulse generator

★ **Two settings :** Gain **4mV/fC**, Peaking time 15ns & 20 ns

★ **Software :** Written in Python 3, uses TRBnet interface to communicate with ASICs

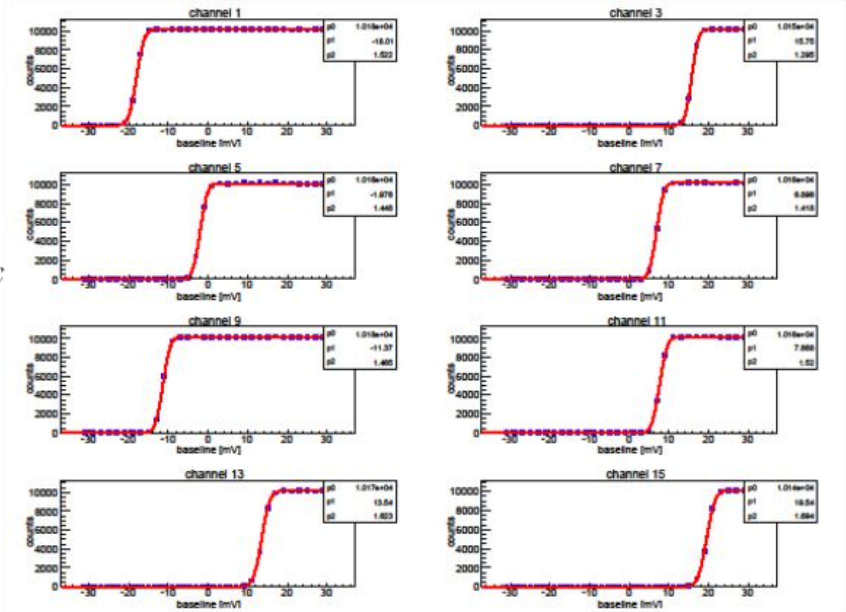
★ **Repository** : https://github.com/HADES-Cracovia/pasttrectools

Noise width calculation (8 channels)

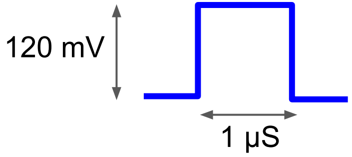
➢ Counts @ FEE output measured as a function of baseline level

Fit function

$$S(x') = A \int_{-\infty}^{x'} \frac{1}{\sigma\sqrt{2\pi}} e^{-\frac{1}{2}\left(\frac{x-u}{\sigma}\right)^2} dx$$



Pulse generator



Comparison of σ

Tp 20 ns

Channel No	1	3	5	7	9	11	13	15
Sigma (gaus) mV	1.24	1.06	0.99	1.01	1.08	1.20	1.49	1.56
Sigma (S-curve) mV	1.52	1.30	1.45	1.42	1.47	1.52	1.62	1.69

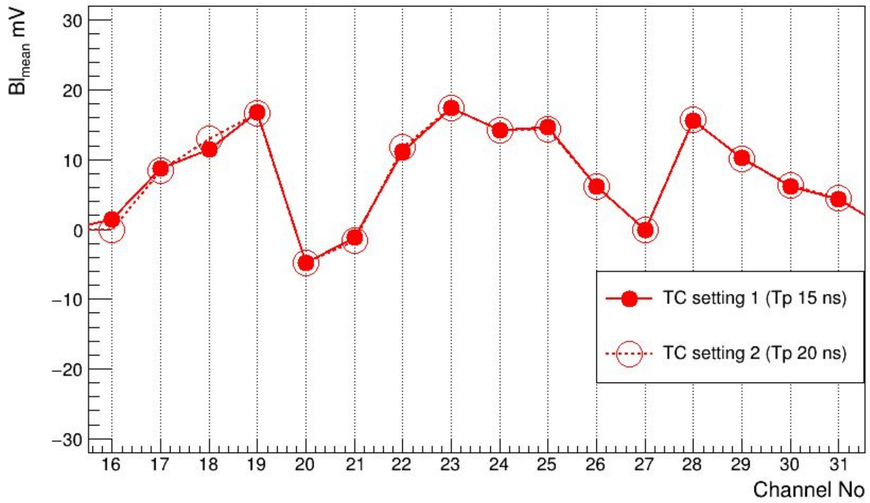
New packed asics

Mean baseline position

B_i – baseline for bin i (i = 1..32)
C_i – counts registered for baseline B_i
$B_{imV} = (B_i * 2) - 32$ // from LSB to mV , baseline values go from -32 to 32 mV

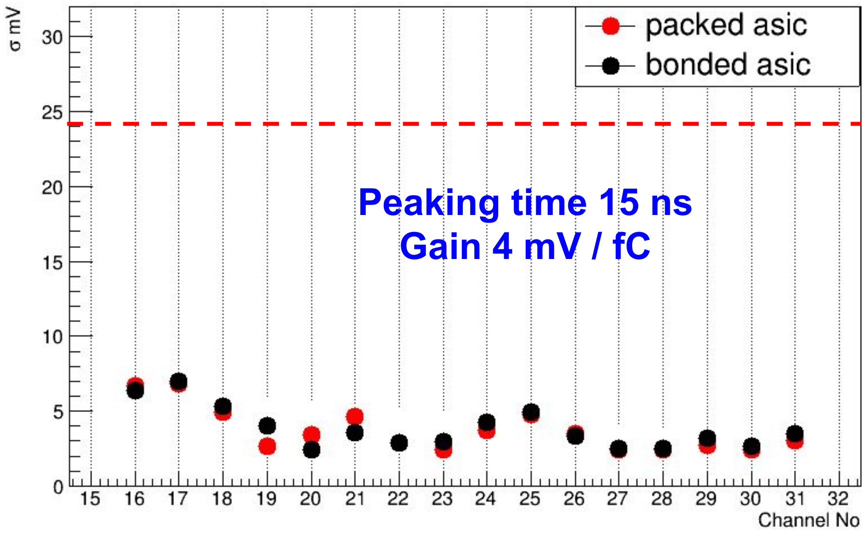
Bl mean = $\frac{\Sigma B_{imV}.C_i}{\Sigma C_i}$

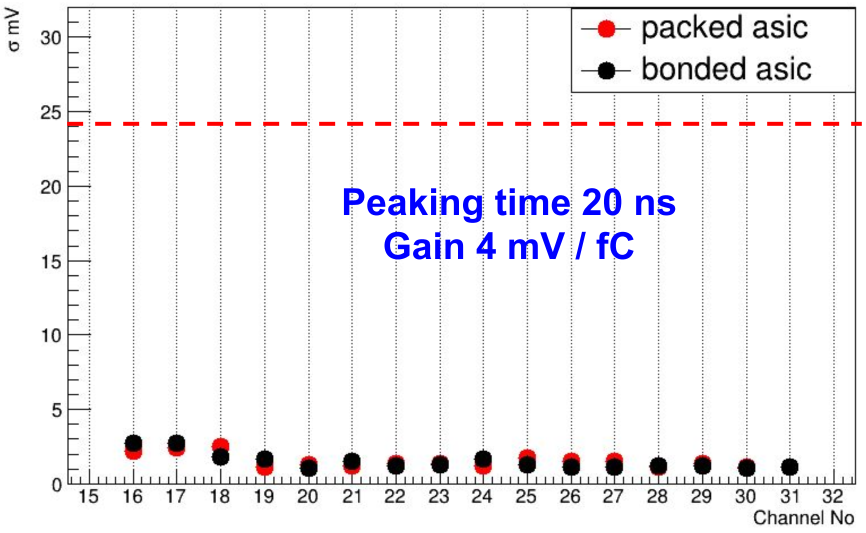
➢ Stable baseline position irrespective of TC setting.



Comparison of bonded and packed asics

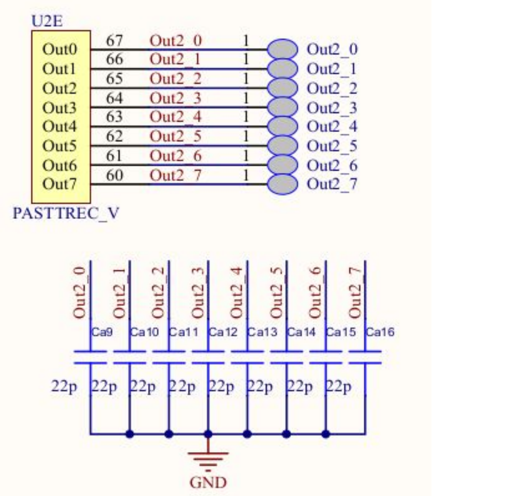
- **σ** < 3 mV @ Tp 20 ns gain 4mV /fC (**@ Gain 1 mV/fC < 1 mV**)
- Discr.threshold of 24mV ~8 sigma above noise (eq.to 6mV for gain 1mV/fC)
- Allows to lower the detector operating voltage to 1700 V
- No significant difference between the packed and bonded asics (preliminary)

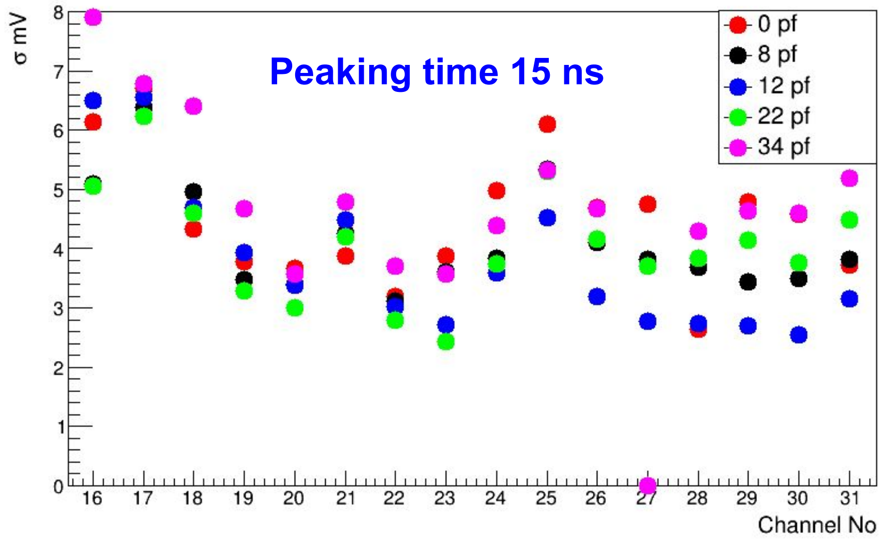


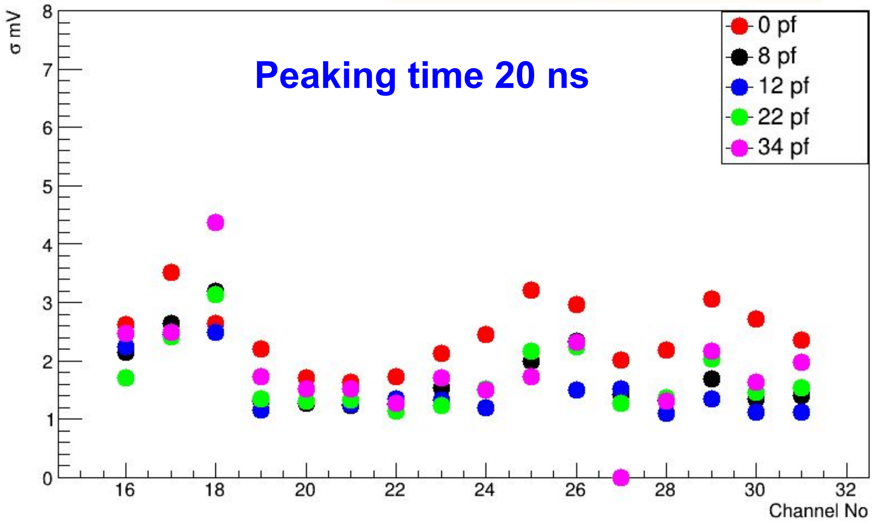


Tests with output load capacitance

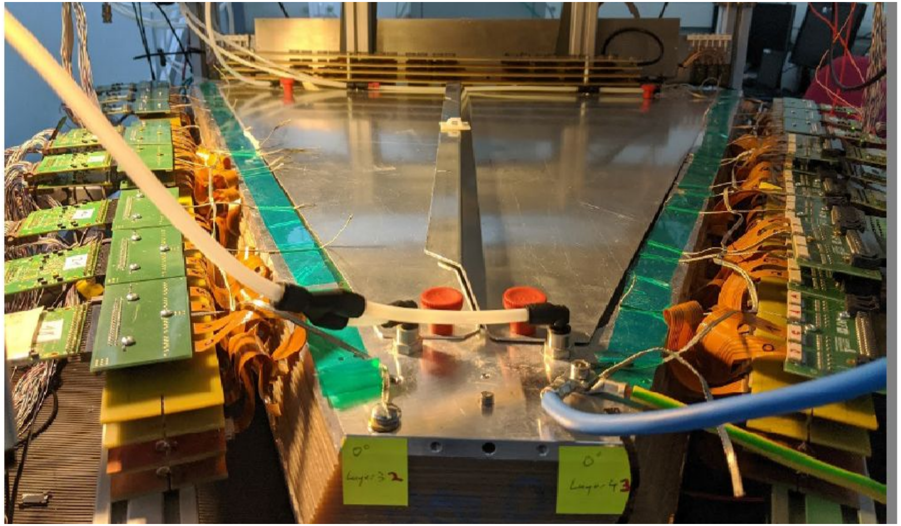
- ➢ PASTTREC needs additional load capacitance on analog output for stability
- ➢ Boards (one FEE) connected to the same module
- ➢ 12 - 22 pF suitable for packed asics



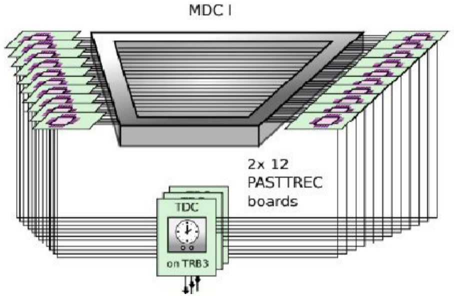


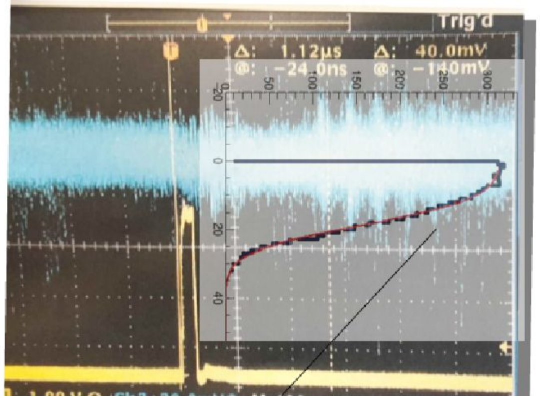


MDC (HADES) chambers @ GSI



- Rectangular cells (5x5 to 14x10) mm^2
- Wire of different lengths(13-75 cm ~10pF/m)
- Use same noise scanning software and ASIC settings (gain 4 mV/fC, 15 ns rise time)



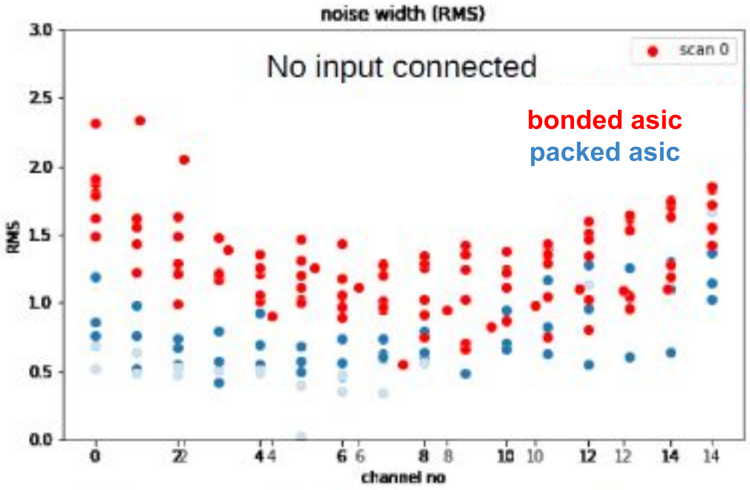


Quantify noise:

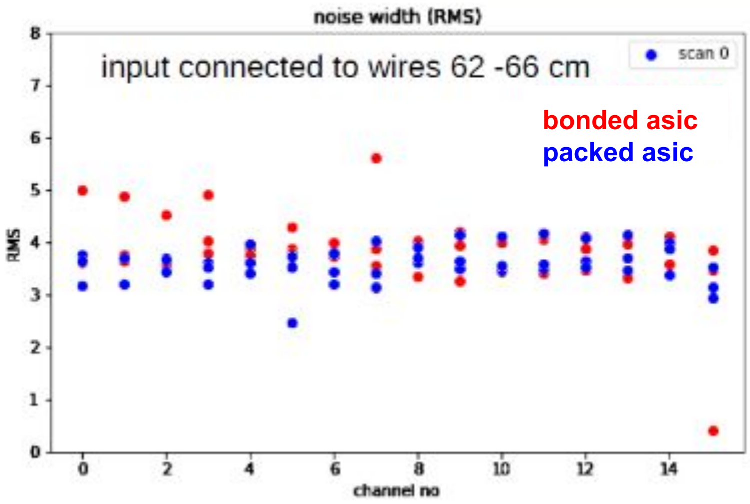
- **MDC HV off → no gas amplification**
- **baseline calibrated**
- **detect count rate by scanning threshold (analog to S-curve)**
  → gives a measure for amplitude distribution of noise per channel
- **Fit width and turning point of distribution**
  → threshold at turning point is interpreted as average measure of the noise amplitude
- **Different types of noise in different channels observed**
  → various distributions:

Noise comparison

- Gain 4 mV/fC , Tp 15 ns
- RMS of baseline/threshold in units of DAC-LSB = 2 mV
- Similar RMS for bonded and packed asics
- MDC typical threshold 30 (60 mV)



Input connected to MDC adapter board only
(for power supply)



Connected to Driftchamber wires 62 -66 cm
long (FPC 32-35)

Summary

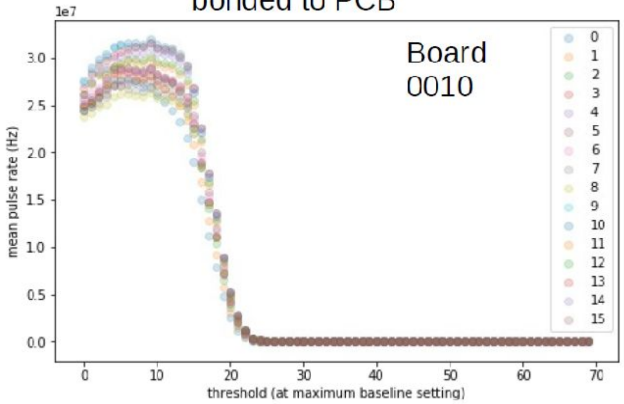
- No significant difference in the asic types (packed - bonded)
- Automatic baseline tuning is a faster and accurate technique.
- Baseline position does not depend on FEE settings
- σ < 1 mV/fC in FT FEE's, hence discr.threshold 6 mV is a safe option
- Dependence of FEE noise on detector module to be further studied

Thank you

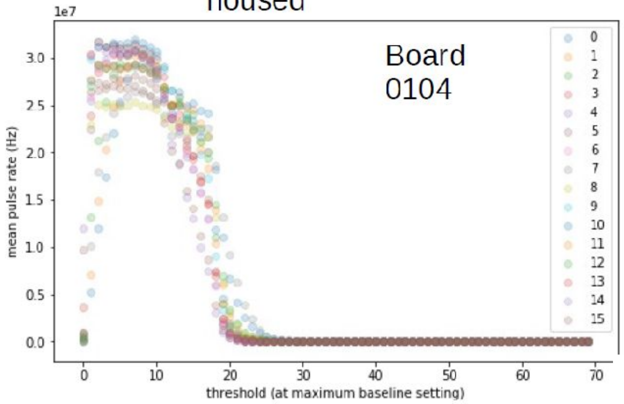
Noise comparison bonded / housed ASICS

- Connected to Driftchamber wires 62 -66 cm long (FPC 32-35)
- Gain = 2, peaking time = 15 ns

bonded to PCB

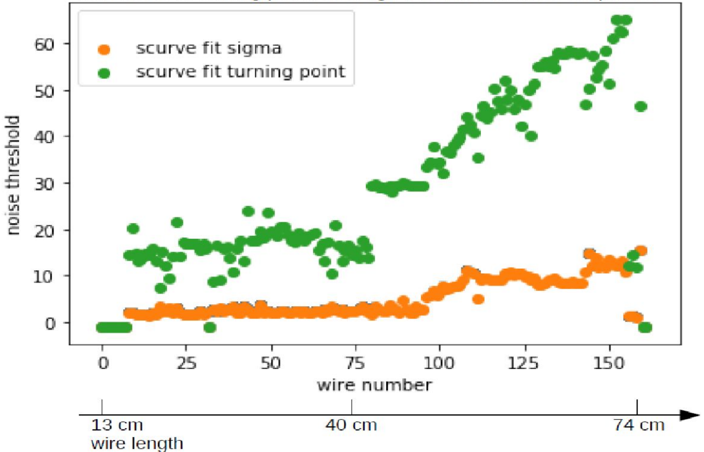


housed



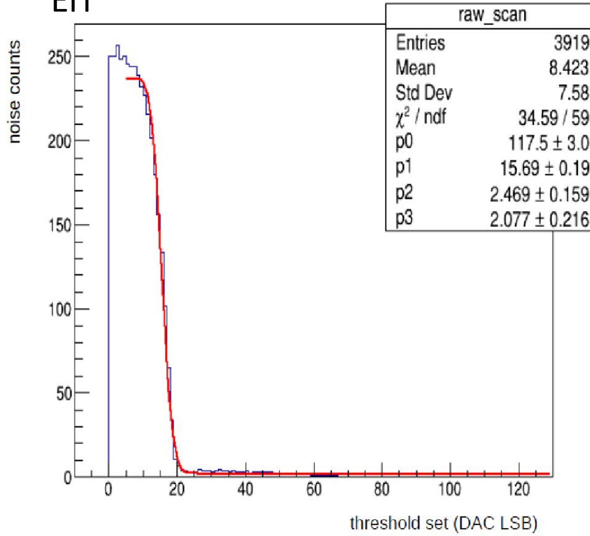
- Baseline line aligned
- Typical threshold 30 (60 mV)

Threshold at turning point: average measure of noise amplitude

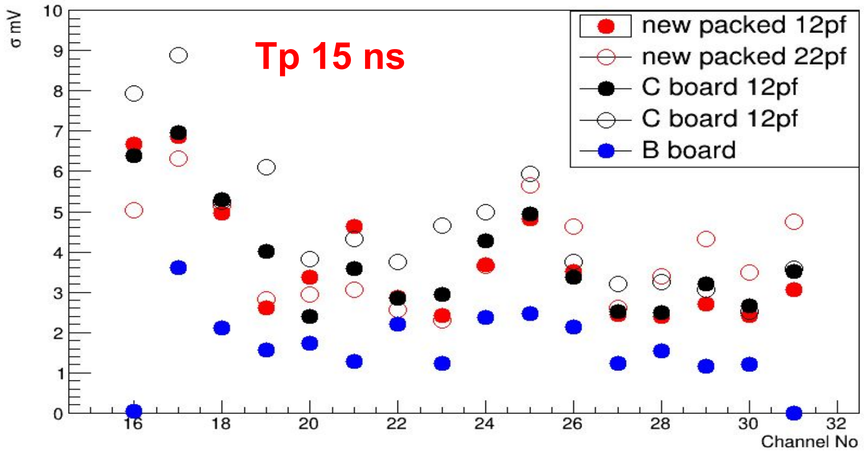


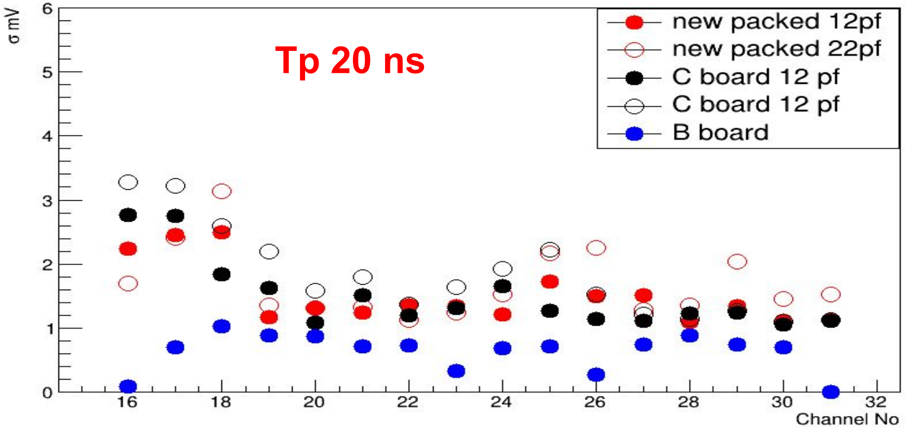

```
0010 average(16chan) noise thresh:
mean =  8.933  +-  0.813   |  RMS  =  4.971  +-  0.296
```

Example of fit for one wire with Erf

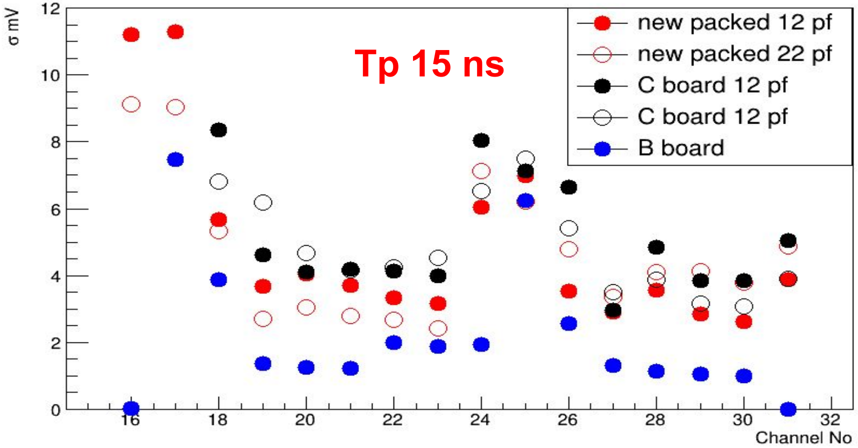


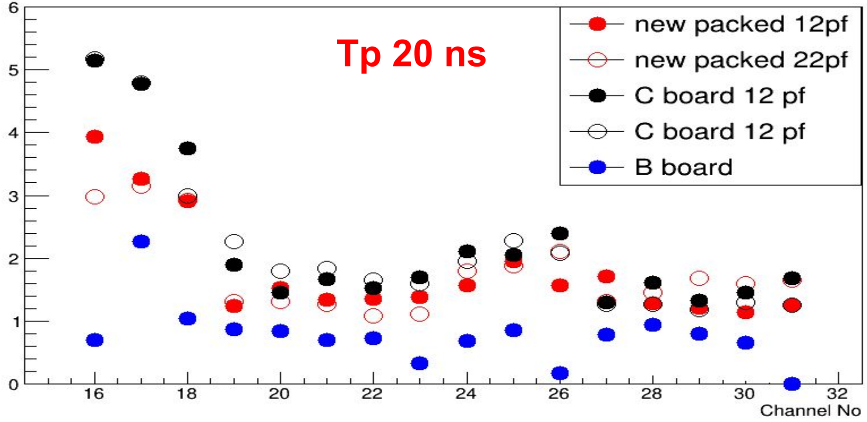
Module 0



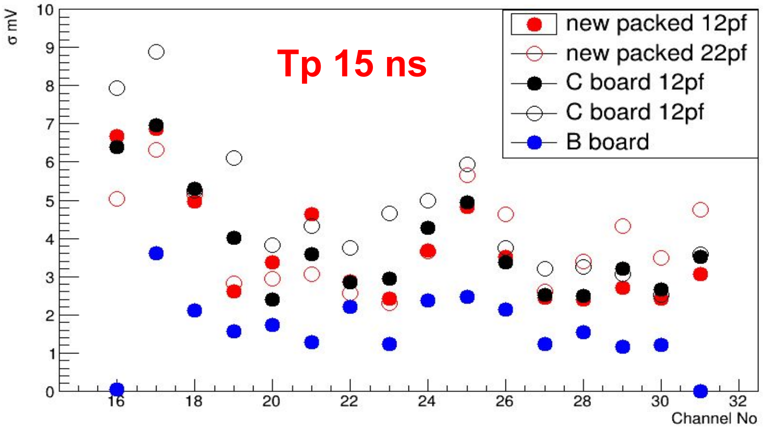


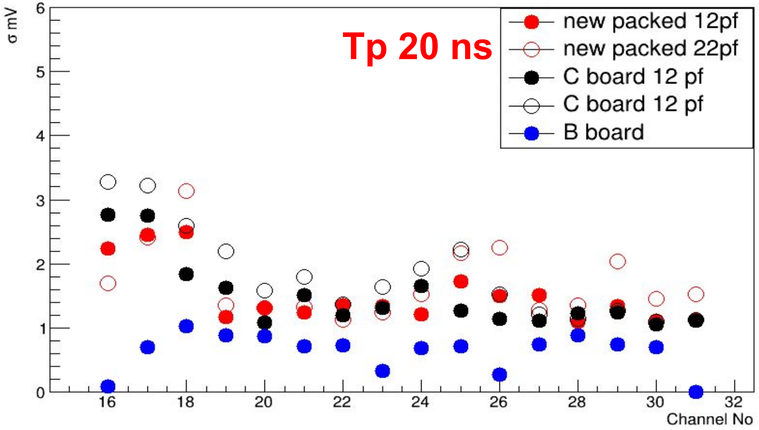
Module 1





Module 0_a





Module 0_b