# Pixel Detector

Sezione di Torino

# MVD silicon pixel detector : readout architecture and ASIC developments

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# MVD

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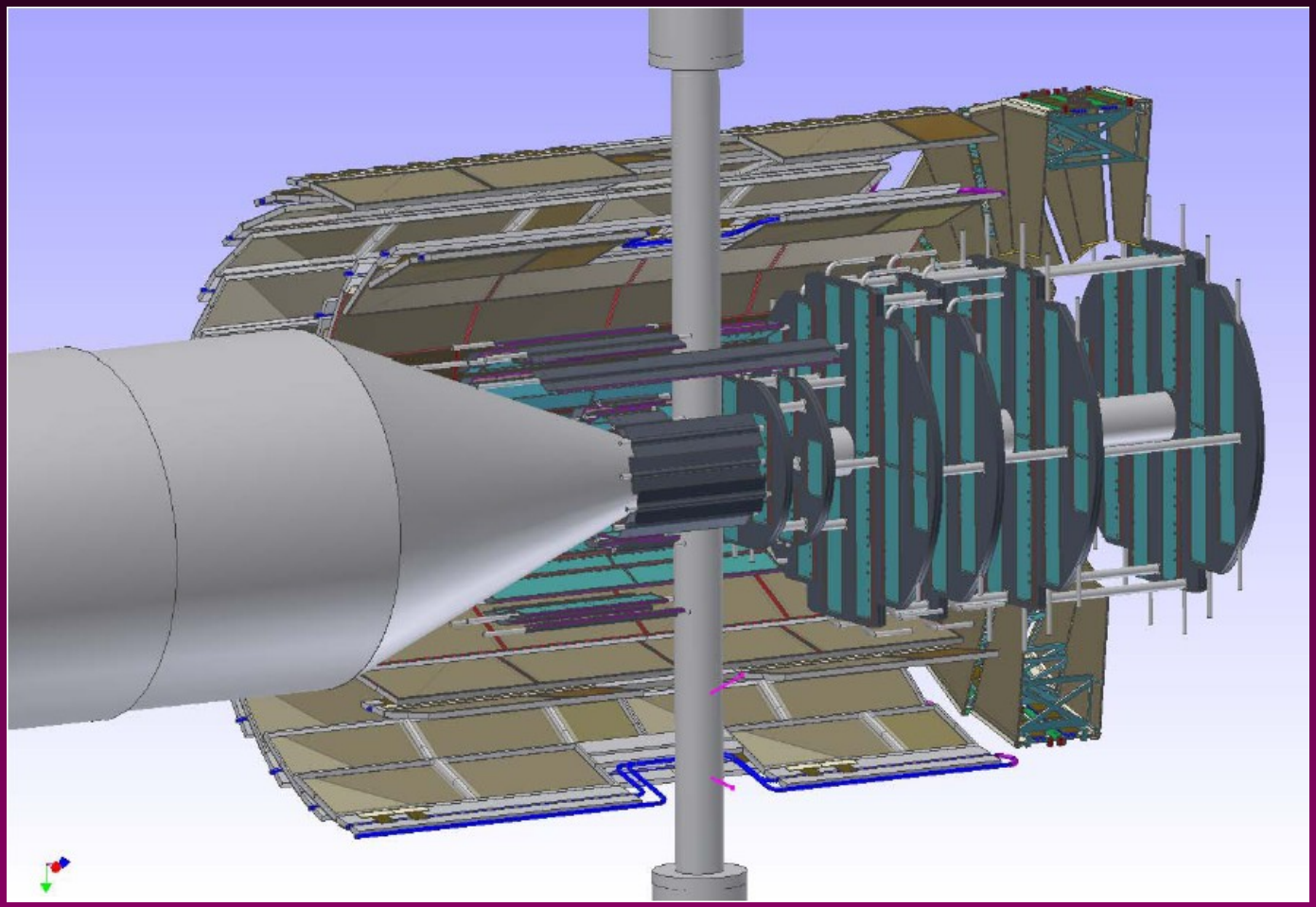

- Barrel :

  Layer 1 : radius 28 mm, SPDs

  Layer 2 : radius 53 mm, SPDs

  Layer 3 : radius 92 mm, SSDs

  Layer 4 : radius 120 mm, SSDs

- Forward :

  Disks 1-2 : radius 37.5 mm, SPDs

  Disks 3-4 : radius 75 mm, SPDs

  Disks 5-6 : radius 130 mm, SPDs + SSDs

# Pixel specifications

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| | |
|---|---|
| Pixel size | 100 × 100 $\mu m^2$ |
| Chip active area | 11.4 × 11.6 $mm^2$ (116 rows, 110 cols) |
| dE/dx measurement | ToT, 12 bits dynamic range |
| Max input charge | 50 fC |
| Noise floor | <32 aC (200 $e^-$) |
| Clock frequency | 156.25 MHz |
| Time resolution | 6.4 ns ( 1.85 ns *r.m.s.* ) |
| Power consumption | < 500 $mW/cm^2$ |
| Max event rate | $6.1 \cdot 10^6$ hits/($cm^2 \cdot s$) |
| Total ionizing dose | < 100 kGy |

# Data rates

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| antiproton- | proton | Ar | Au |
|---|---|---|---|
| Average flux [hits/cm$^2$·s]<br>Disk number | 8.24·10$^5$<br>Disk 6 | 3.30·10$^5$<br>Disk 5 | 9.47·10$^4$<br>Disk 4 |
| Average flux [hits/cm$^2$·s]<br>Barrel 1 - stave | | 2.55·10$^5$<br>stave 3 | 1.03·10$^5$<br>stave 13 |
| Average flux [hits/cm$^2$·s]<br>Barrel 2 - stave | | 2.55·10$^5$<br>stave 19 | 2.54·10$^4$<br>stave 25 |
| Max flux [hits/cm$^2$·s]<br>[hits/(readout chips·s)] | 6.1·10$^6$<br>~8.1·10$^6$ | 6.8·10$^5$<br>~9·10$^5$ | 1.65·10$^4$<br>~2.18·10$^4$ |

p : 2.0·10$^{32}$
Ar : 2.4·10$^{31}$
Au : 2.2·10$^{30}$

annh. rate 2·10$^7$ @ 15 GeV/c

# Module concept

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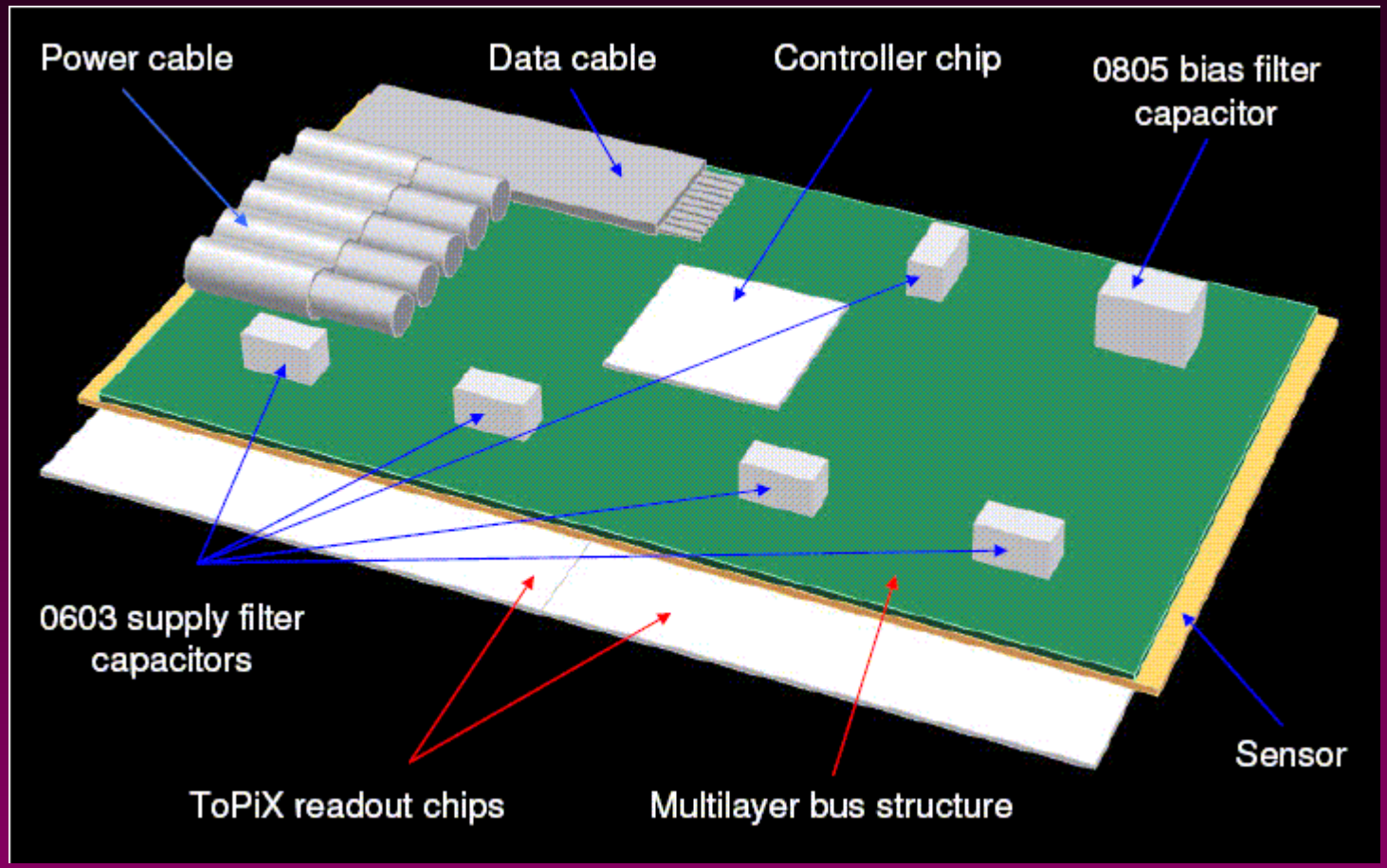

# Module options

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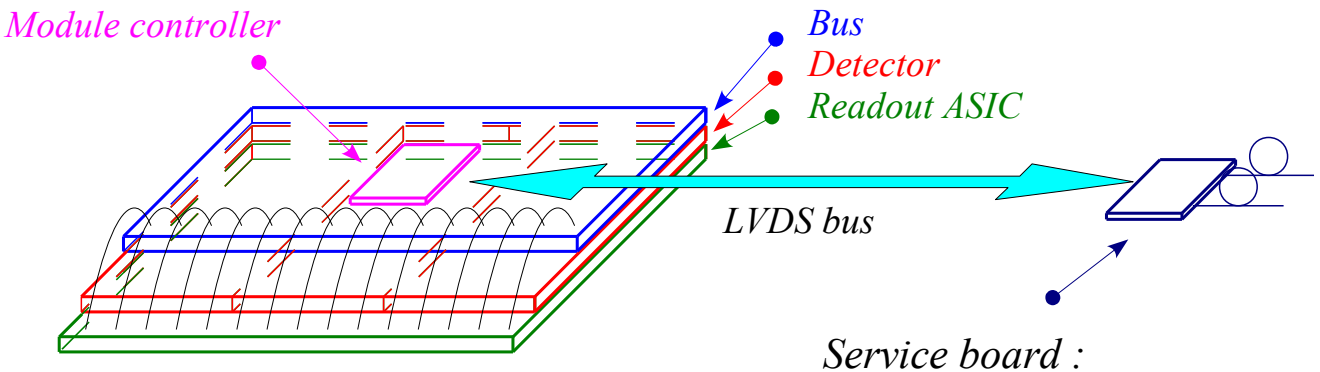
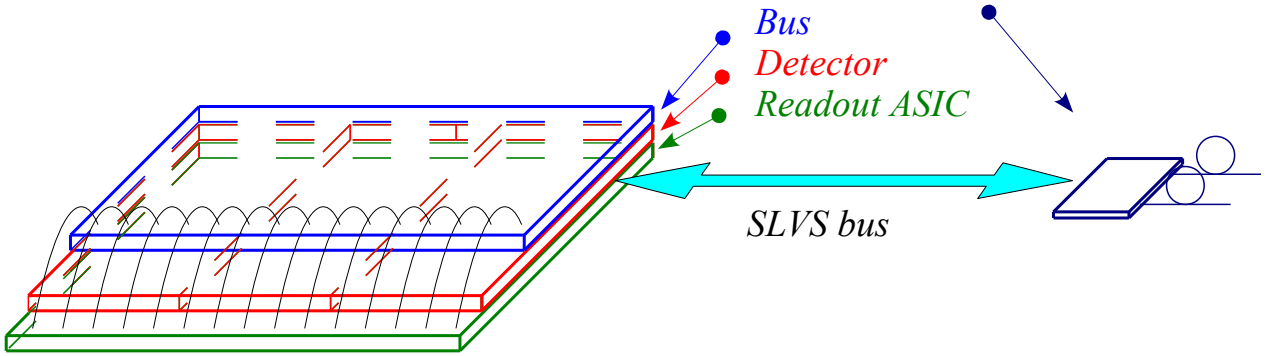



Option 1




Option 2

# Options pro/cons

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- Option 1
  - ☺ reduced number of cables
  - ☺ simpler ToPiX control logic
  - ☺ better management of data rate increase
  - ☹ requires an extra chip
- Option 2
  - ☺ no need of an extra chip
  - ☺ interface already under development at CERN
  - ☹ more cables

# ToPiX ASIC

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- Custom development for the PANDA MVD
- Provides spatial and time coordinates plus energy resolution measurement ( via ToT )
- Compatible either with p-type or n-type detectors
- Self triggered architecture
- Each event has a 12 bits time reference
- Data corresponding to a 12 bits counter cycle (26.21 μs ) are packed in a frame, with an 8 bits frame counter ( 6.71 ms cycle )
- *Possible modification : counter cycle stopped at 3000 (19.2 μs, i.e. 8 bursts) - 8 bits frame counter cycle ~4.9 ms (8 super-bursts)*

# Pixel cell

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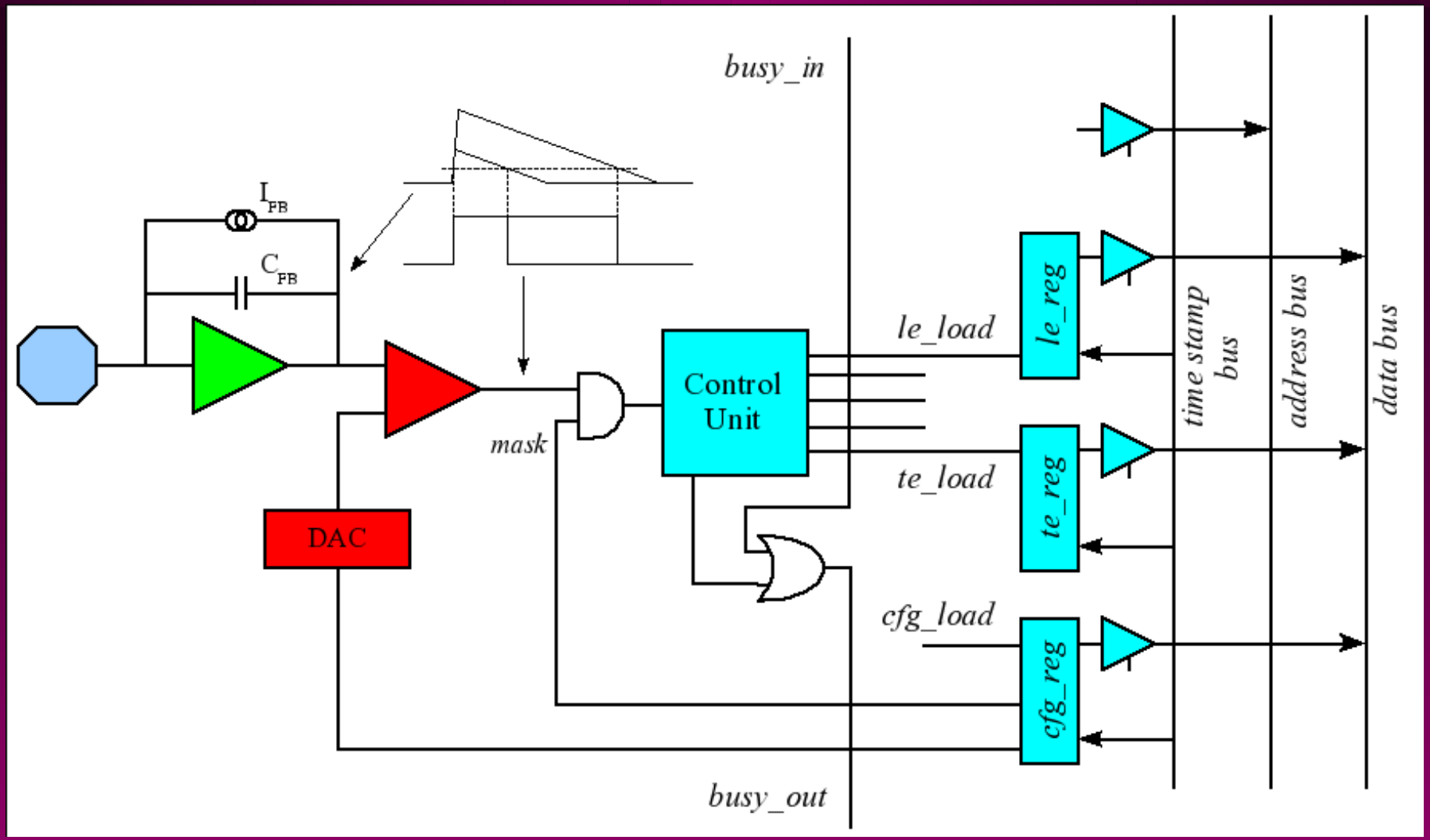

# ToPiX block diagram

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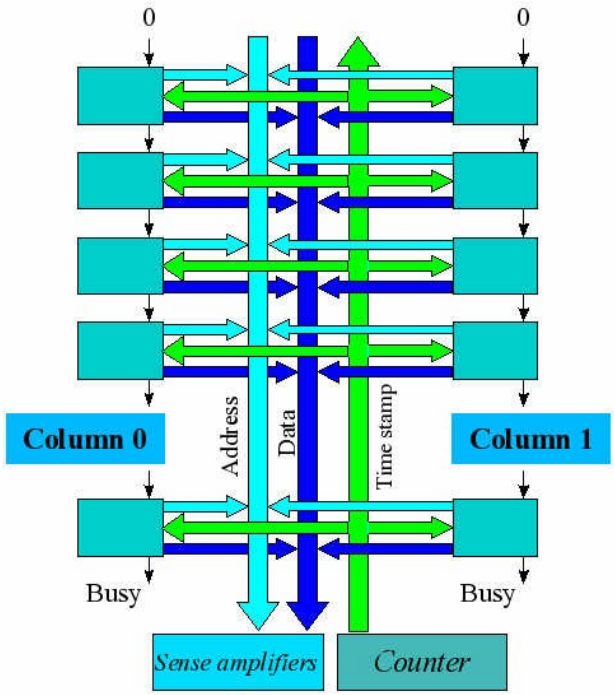


116 pixels/column
110 columns
50 bits/event
8.1 MHits/s
~400 Mb/s max output rate

# Data format

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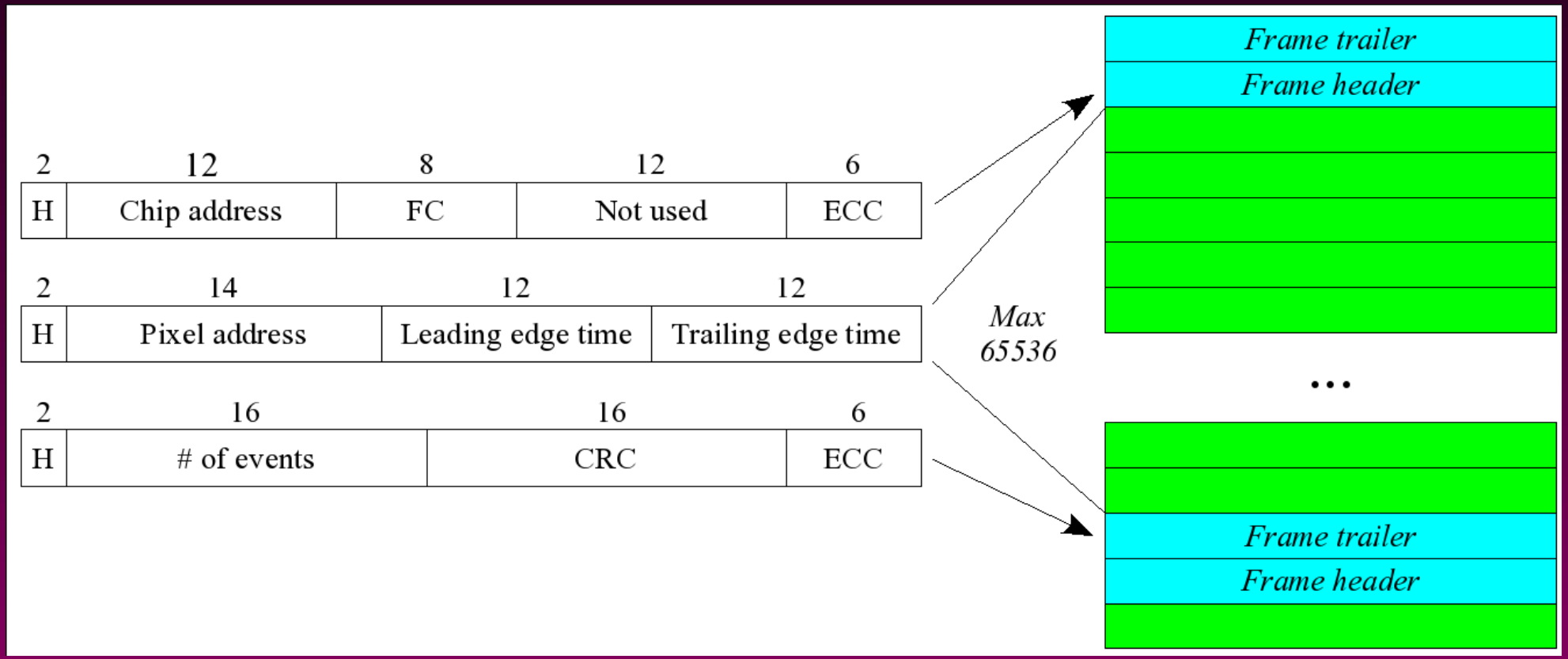
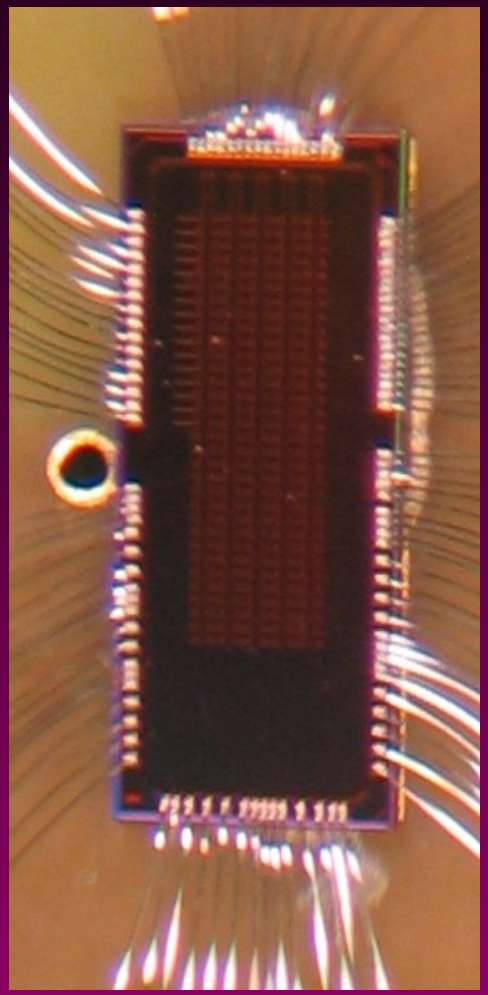


# ToPiX v2

Sezione di Torino



- Full pixel cell ( analogue + digital )
- Two folded columns with 128 cells
- Two columns with 32 cells
- 5x2 $mm^2$ die area
- CMOS 0.13 μm LM technology
- Dice-based SEU resistant FFs
- Tests :
  - → test bench
  - → with a sensor and a radiation source
  - → TID and SEU

# ToPiX v3

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- Under design
- 5x4 $mm^2$ die area
- CMOS 0.13 μm DM technology
  - LM → 6 thin, 2 thick metal layers
  - DM → 3 thin, 2 thick, 3 RF metal layers
- Triple redundancy-based SEU protection
- End of column logic
- 312.5 Mb/s serial output
- Pads for bump bonding

# Topix3 stability with $C_f$ = 12fF

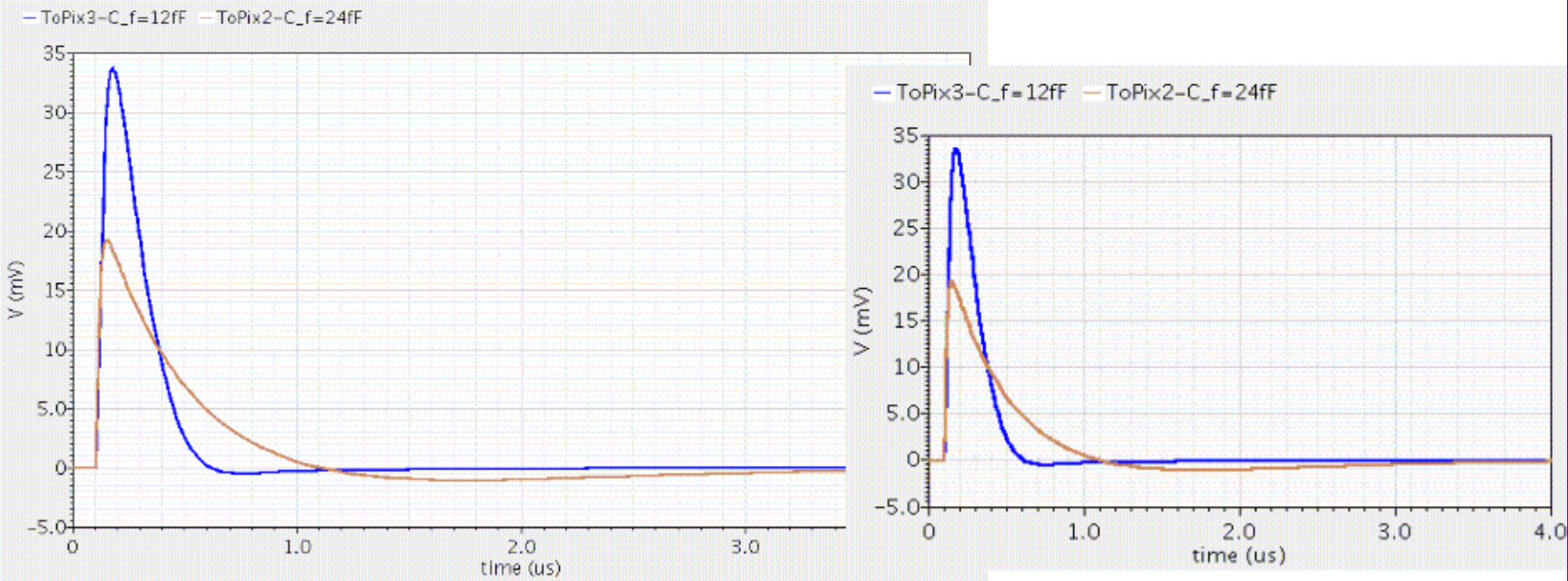
Reduction of the offset in the charge measurement.

The offset in the charge measurement is caused by the channel-to-channel baseline variation:

$$\Delta Q_{offset} = \frac{\Delta V_{var}}{CSA_{gain}} = \Delta V_{var} C_f$$

The ToPix2 value of $C_f$ is 24fF and was chosen as a compromise between gain and stability of the loop.

The number and size of the transistors in the feedback path have been carefully optimized to allow a reduction of the feedback capacitance to 12fC.

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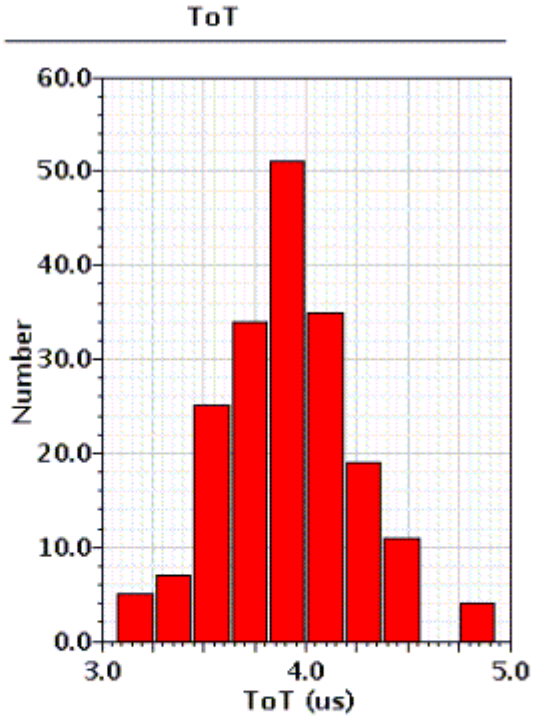
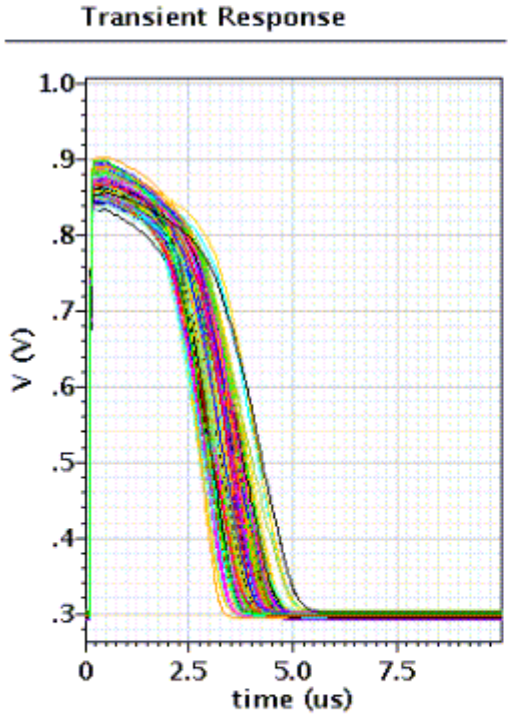
# Monte Carlo simulation for mismatch and process variation (ToPix3)

The mismatch effects have been minimized achieving a ToT channel-to-channel variation σToT/ToT of 10%.

Number of simulations = 200
$Q_{in} = 20fC$
Mean = $3.908\mu s$
Standard deviation = $319ns$




Baseline variation
$\Delta V_{var} \approx 10mV$

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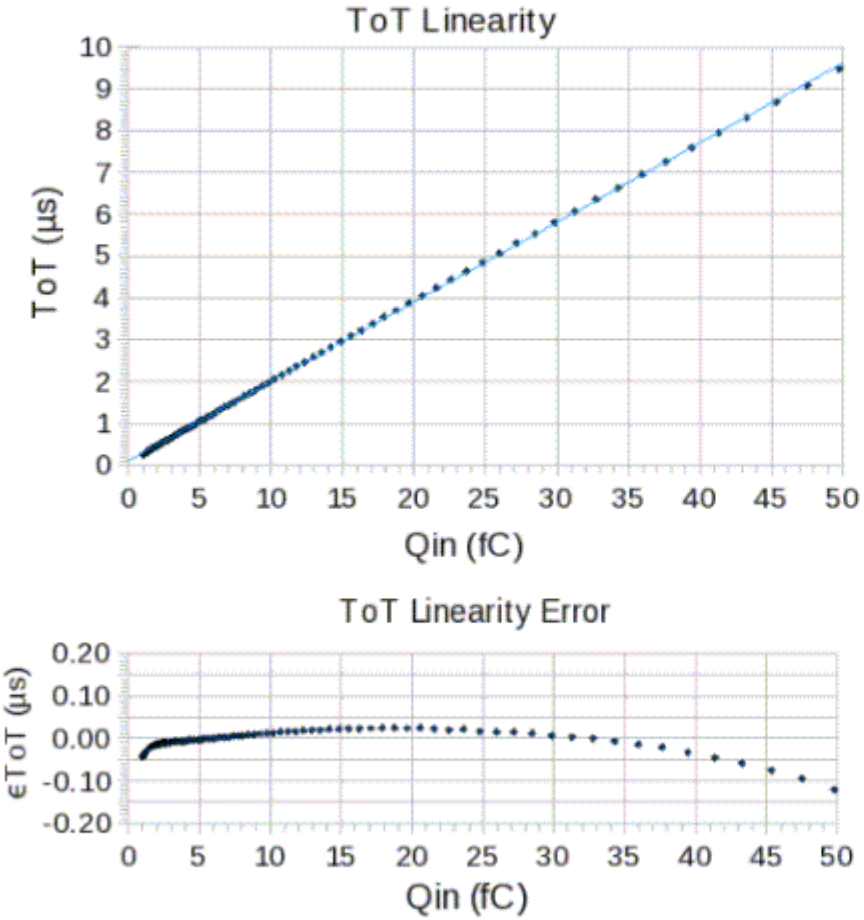
# ToT vs Qin linearity up to 50fC




$$ToT[Q_{in}] = 191\,\frac{ns}{fC}\cdot Q_{in} + 97fC$$

| | |
|---|---|
| Analog Gain | ~70mV/fC |
| Dynamic Range | 50 fC |
| Equivalent Noise Charge | 200 $e^-$ rms |
| Leakage | Up to 50nA |
| σToT/ToT | 10% |
| Baseline variation | ±10mV |
| Input signal polarity | Selectable |
| Discharging current | 5nA |

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# Pixel layout - 1

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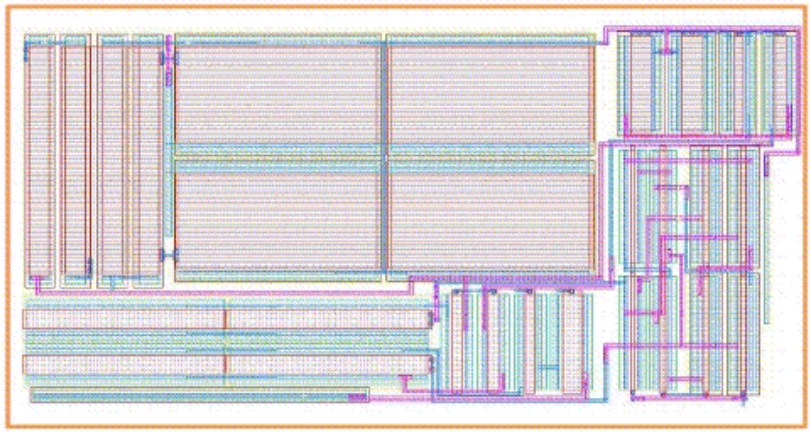
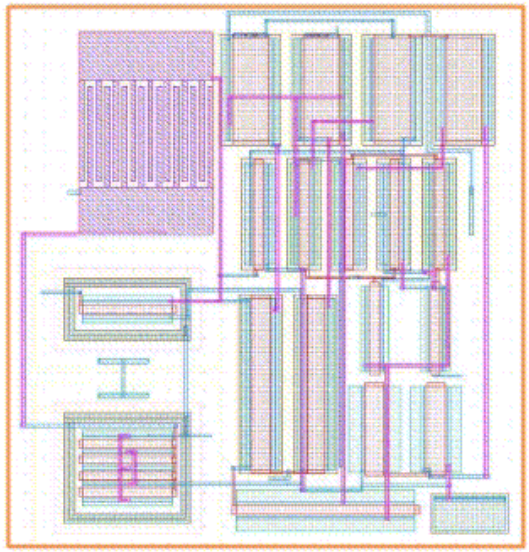
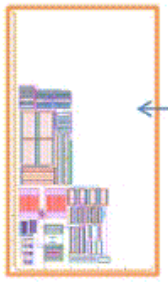
Filter stage: 40µm x 20µm (50% of area of the previous)



Preamplifier 35µm x 30µm



Analog Cell 100µm x 50µm (-30%)



To be designed

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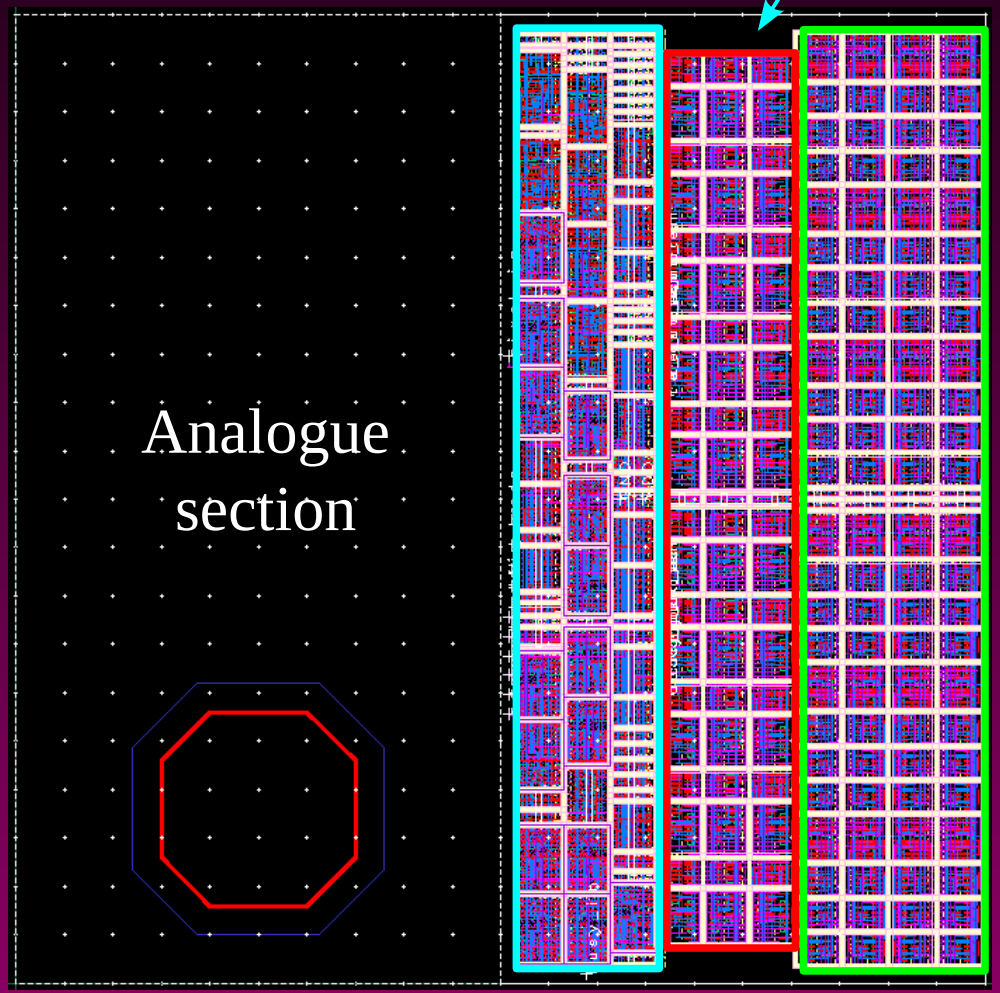
# Pixel layout - 2

Sezione di Torino



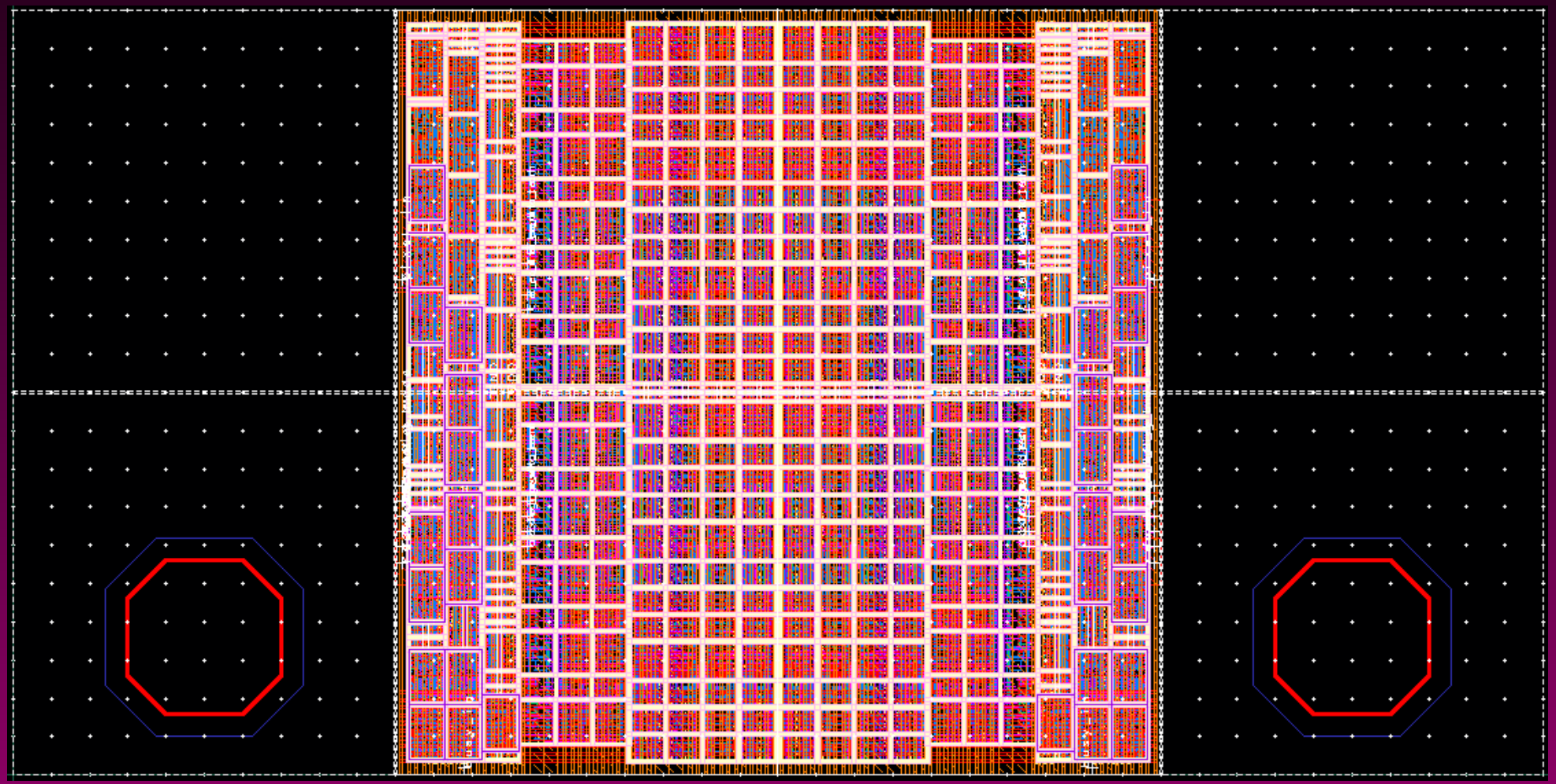

Configuration register ( TR with correction) - 9 bits

Leading and trailing edge registers (TR w/o correction) – 12 bits

Control logic ( TR FF )

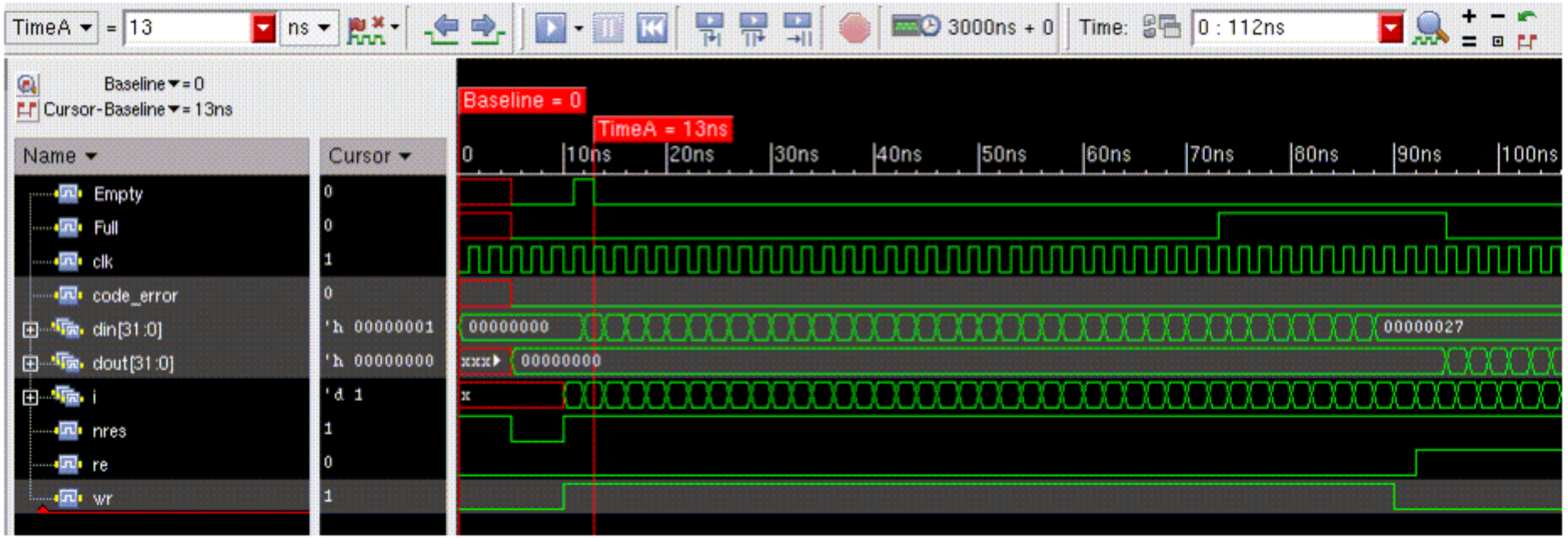
# Double pixel

Sezione di Torino



32x32 FIFO:

1. Hamming code encoder/decoder for single error correction (SEC)
2. Triple Module Redundancy registers for FIFO control logic;
3. Triple Module Redundancy Flip-Flops for counters;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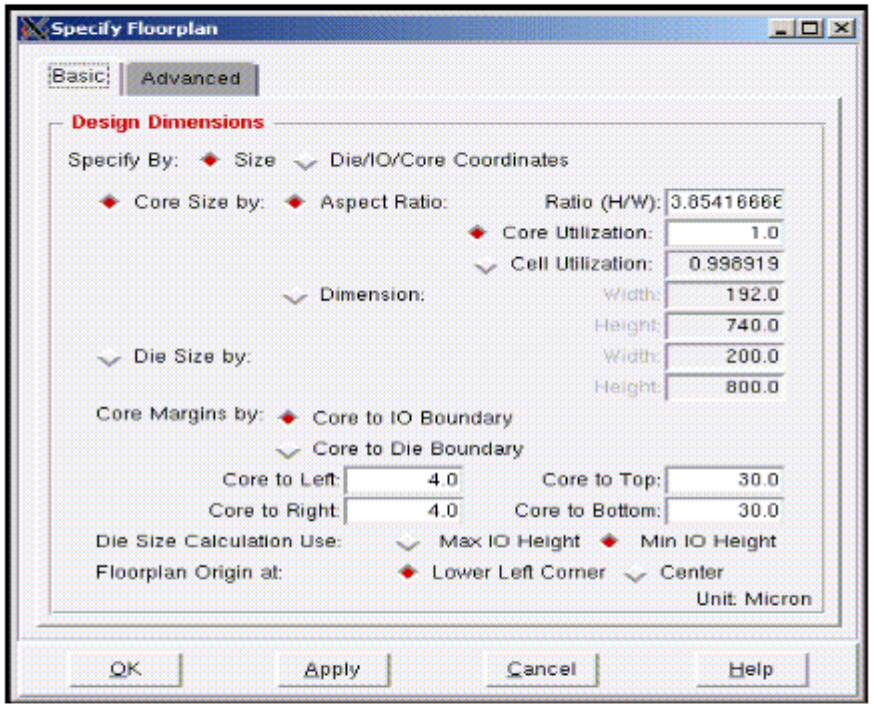
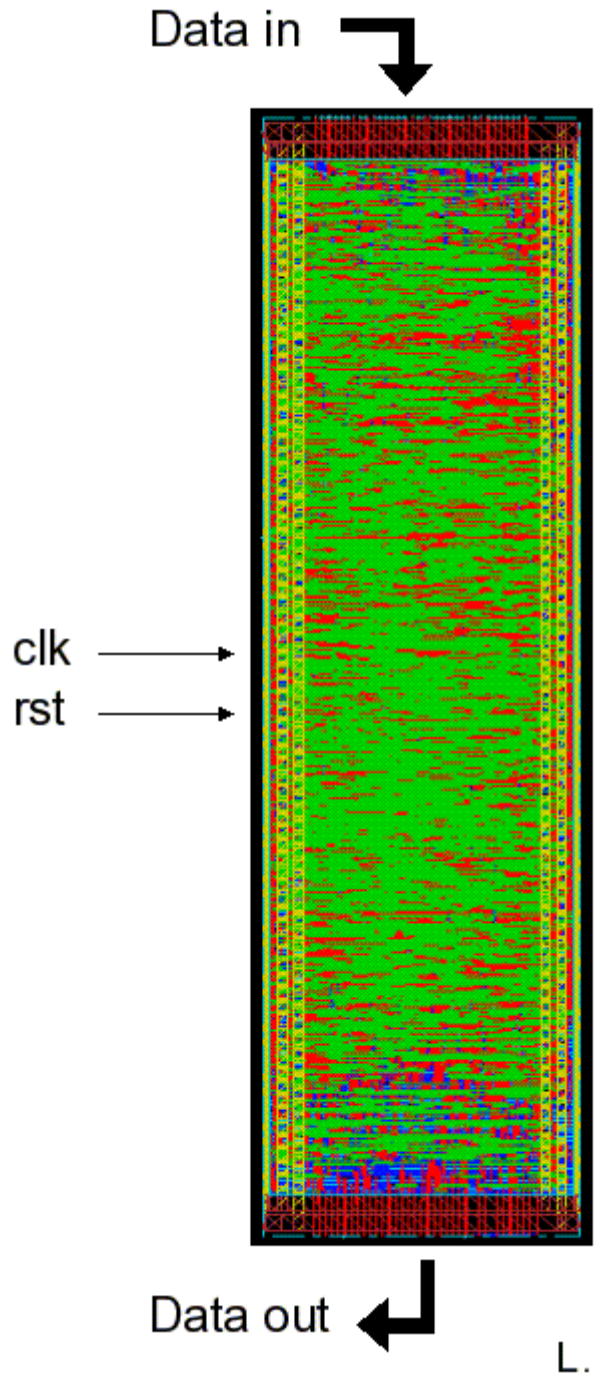
Routing layers = 5




Density: 72.964%

**average power: 14.570 mW**
**average switching: 12.580e mW**
**average leakage power: 1.9895 mW**
**worst IR drop average analysis: 3.4679 mV**

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# Floorplan

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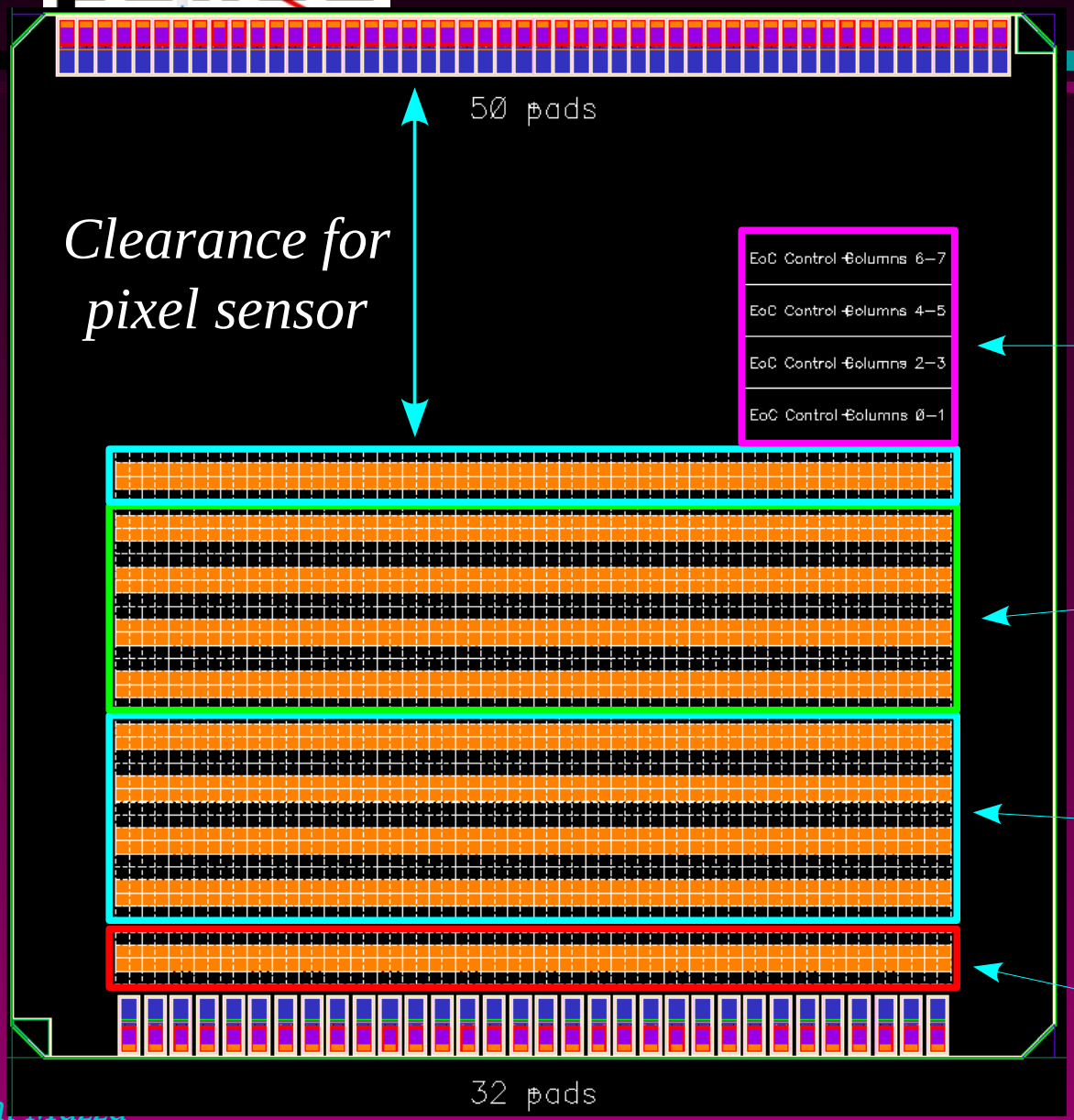


End of column FIFOs

32×2 pixel column

128×2 pixel column

128×2 pixel column

32×2 pixel column *or*
32 channels strips r/o

# Design status

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- Analogue pixel circuitry modification completed, layout design ongoing.
- Digital pixel section layout well advanced.
- HDL system simulation re-started.
- 160 MHz column drivers and receivers test ok *( NA62 GtkTo )*.
- Hamming protected FIFO layout completed.
- End of column control logic design started.
- Slow control interface design to be started.
- E-link interface under test at CERN.

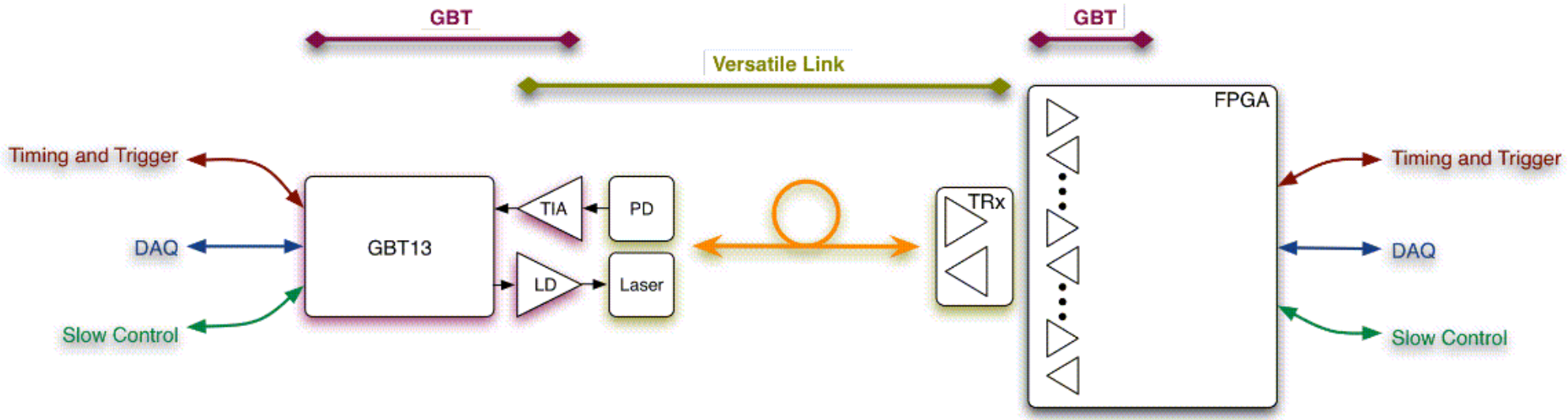
# Radiation Hard Optical Link Architecture

*Defined in the "DG White Paper"*

- *"Work Package 3-1"*
  - Objective:
    - Development of an high speed bidirectional radiation hard optical link
  - Deliverable:
    - Tested and qualified radiation hard optical link
  - Duration:
    - 4 years (2008 – 2011)

***Radiation Hard Optical Link:***

- *Versatile link project:*
  - Opto-electronics
  - Radiation hardness
  - Functionality testing
  - Packaging
- *GBT project:*
  - ASIC design
  - Verification
  - Functionality testing
  - Packaging




**On-Detector**
Custom Electronics & Packaging
Radiation Hard

**Off-Detector**
Commercial Off-The-Shelf (COTS)
Custom Protocol

# Project Schedule

- *2008*
  - Design and prototyping of performance critical building blocks:
    - GBTIA, GBLD, Serializer, De-Serializer, Phase Shifter
  - First tests of optoelectronics components
    - SEU tests on PIN receivers
  - Proceed with the link specification meetings
  - General link specification
- *2009*
  - Design/prototype/test of basic serializer/de-serializer (GBT-SERDES) chip
    - GBT-SERDES ("Tape-out" 9th of November)
  - Design/prototype/test of optoelectronics packaging
    - GBTIA + PIN on TO CAN
- *2010*
  - GBLD re-spin
  - GBT-SERDES testing ← !
  - Detailed link specification document
  - Full prototype of optoelectronics packaging
  - Prototype of "complete" GBTX chip } ?
- *2011*
  - Extensive test and qualification of full link prototypes
  - System demonstrator (s) with use of full link
  - Schedule of the final production version is strongly dependent on the evolution of the LHC upgrade schedule

# PANDA DAQ

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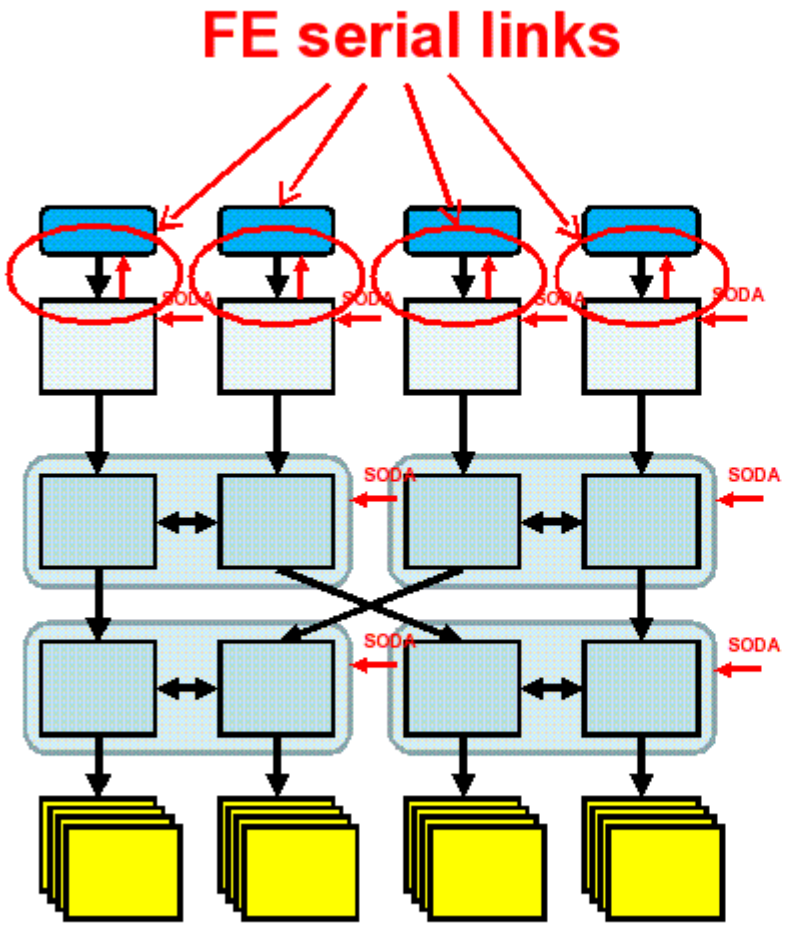


DAQ :

Beam structure : 2 us burst + 400 ns pause

Super burst : 256 bursts → 614.4 μs

Data block corresponds to one burst

Superblock corresponds to 614.4 μs beam

DAQ builds super bursts by Round Robin algorithm

200 GB/s sustained data rate

# Multiplexer

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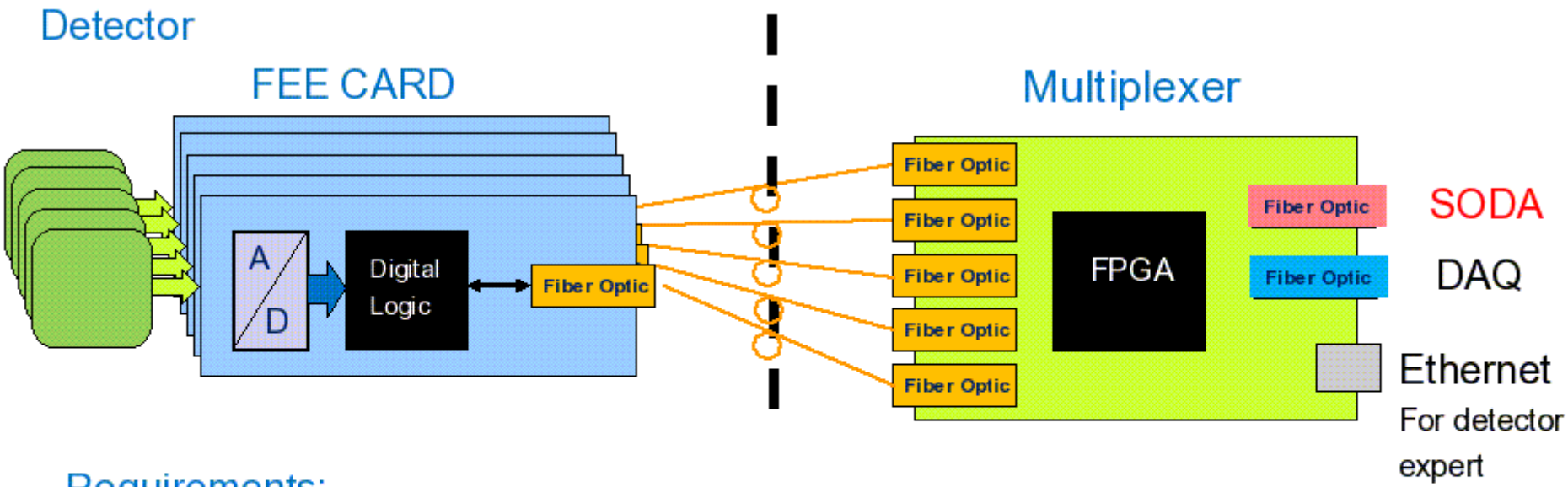


Requirements:

FEE interface functionality:

- SODA commands
- DATA transmission
- Slow control

Speed: 1.5-4.5Gb/s

Some detectors require radiation tolerant components

Hardware solution: FPGA with SerDes

# FPGA usage

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## Resource usage

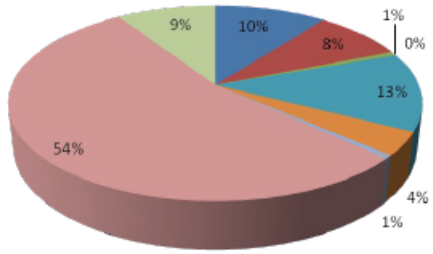
- Implementing several channels leads to an important usage of logic cells resources

| Max usable/available nb of channel | Altera Stratix II GX | Logic cells usage in % |
|---|---|---|
| 8/8 | EP2SGX30D | 92% |
| 12/12 | EP2SGX60D | 78% |
| 16/16 | EP2SGX90E | 69% |
| 20/20 | EP2SGX130G | 59% |
| 24/24 | | |

| Max usable/available nb of channel | Xilinx Virtex 5 | Logic cells usage in % |
|---|---|---|
| 3/8 | XC5VFX30T | 87% |
| | | |
| 10/16 | XC5VFX100T | 93% |
| 13/20 | XC5VFX130T | 94% |
| 20/24 | XC5VFX200T | 96% |

This table gives only ressource usage in terms of logic cells but other ressources are used such as DSP blocks or RAM.
Differences between Altera and Xilinx logic cells usage can be explained by the different policies they adopt in term of ratio between number of logic cells and number of transceivers.

- The Reed Solomon decoder takes most of the resources




Resource usage (in ALMs*) by entity for one full channel implemented on Stratix II GX

ALM: Adaptative Logic Module (contains 2LUTs and 2 registers)

# Conclusions

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- ToPiX :
  - Pixel cell design well advanced, complete layout will be finalized in the summer
  - HDL system simulations restarted
  - End of column design ongoing
    - ➔ *On track for the November submission (up to now...)*
- Data transmission :
  - E-link interface for the current prototype
  - GBT tests ongoing at CERN
- Future steps :
  - ToPiX version 3 submission and tests
  - ToPiX v3 – detector and ToPiX v3 – GBT tests
  - GBT-FPGA customization for PANDA ( interface with SODA and DAQ )