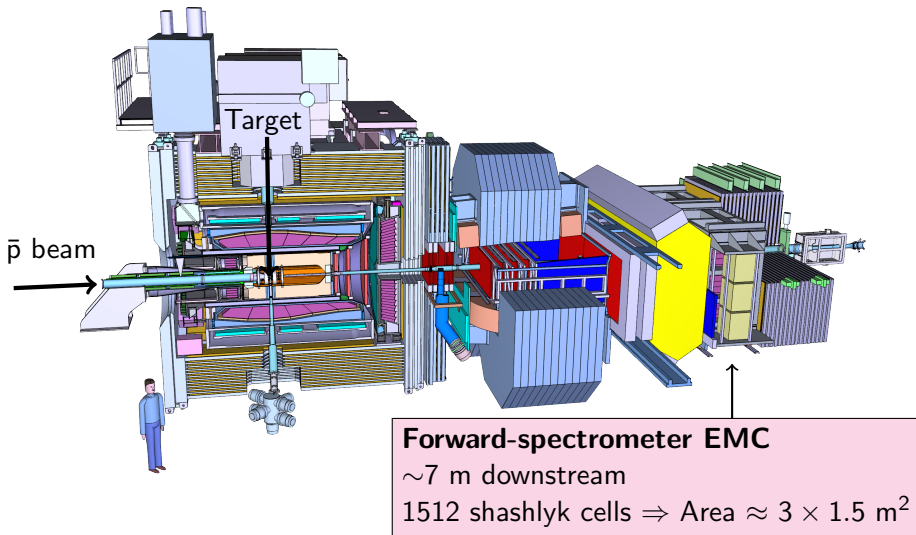


# FPGA-based algorithms for feature extraction in the PANDA shashlyk calorimeter



Markus Preston, Per-Erik Tegnér

# Location of the shashlyk calorimeter



# Front-end digitiser module

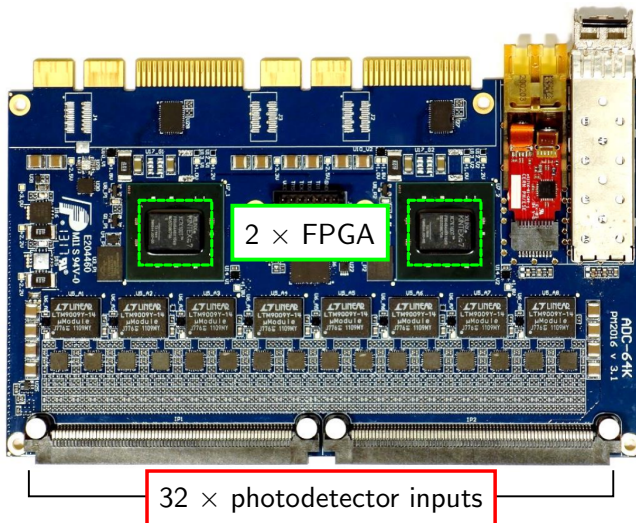


Figure courtesy of Pawel Marciniewski, Uppsala University.

# Front-end digitiser module

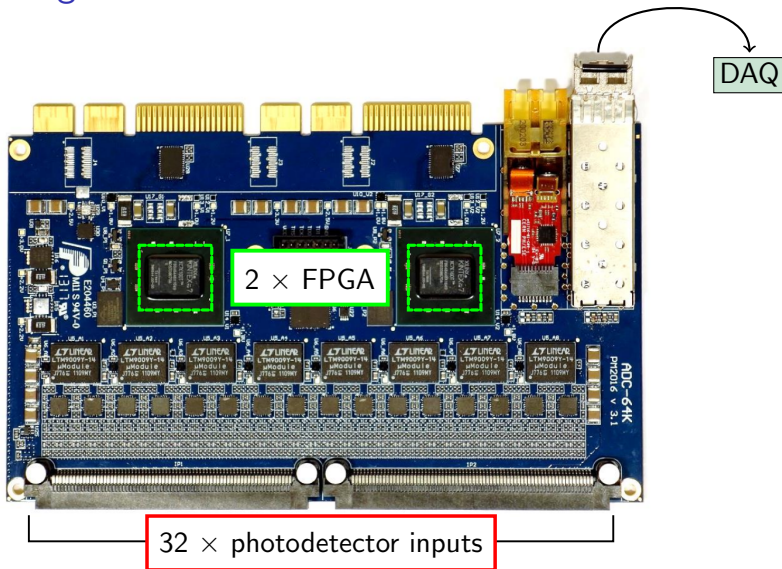


Figure courtesy of Pawel Marciniewski, Uppsala University.

# Tasks of the front-end digitiser

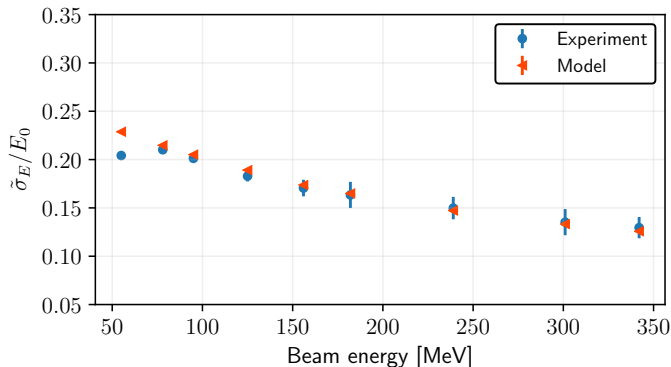
- ▶ PANDA DAQ scheme  $\Rightarrow$  real-time “feature extraction” in FPGAs.

# Tasks of the front-end digitiser

- ▶ PANDA DAQ scheme  $\Rightarrow$  real-time “feature extraction” in FPGAs.
  1. Identify signals
  2. Extract pulse-height information.
  3. Extract timing information.
  4. Recover/reconstruct pile-up pulses.
  5. Transmit only these extracted features.
- ▶ Aim of our work: Develop an FPGA triggering/feature extraction algorithm for these tasks.

## Model development

- ▶ Detailed Geant4-based Monte Carlo model of detector (shower profile, time constants, attenuation, PMT response, electronic noise)
- ▶ Model has been validated against testbeam data (pulse height and time resolution).



# New feature-extraction method

## Basic considerations

- ▶ May first consider “reference” option:
  - ▶ Waveform maximum  $\Rightarrow$  pulse height distribution
  - ▶ (Digital) CFD  $\Rightarrow$  timing distribution
  - ▶ Pile-up rejection



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- ▶ Can one do better?
  - ▶ Methods based on “Optimal Filter” (OF) are well known in high-energy physics.
  - ▶ Finite impulse response (FIR) filter  $\Rightarrow$  pulse amplitude and time.
  - ▶ Assume fixed pulse shape.
  - ▶ Equivalent to  $\chi^2$  fit of known pulse shape to data.

# New feature-extraction method

## Adapting the OF

- ▶ Two main issues with using an OF in PANDA:
  - ▶ No bunch-crossing information from accelerator  $\Rightarrow$  phase between data and sampling clock not known.
  - ▶ No pile-up reconstruction.

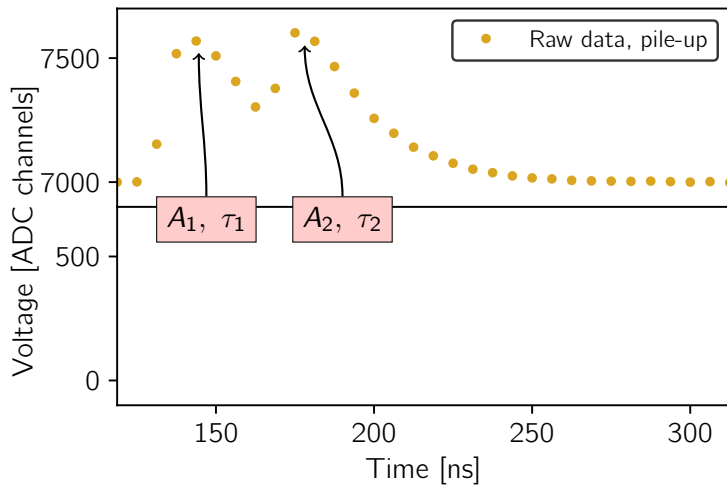
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## Adapting the OF

- ▶ Two main issues with using an OF in PANDA:
  - ▶ No bunch-crossing information from accelerator  $\Rightarrow$  phase between data and sampling clock not known.
  - ▶ No pile-up reconstruction.
- ▶ To solve this, we propose:
  1. Only include initial part of pulse (rising edge + maximum) in OF “fit”  $\Rightarrow$  no contamination from pile-up.
  2. Store several assumed pulse shapes, for different signal/clock phases.
  3. Analyse incoming data with digital CFD  $\Rightarrow$  estimate phase.
  4. “Fit” correct assumed pulse shape  $\Rightarrow$  amplitude + more accurate timing.

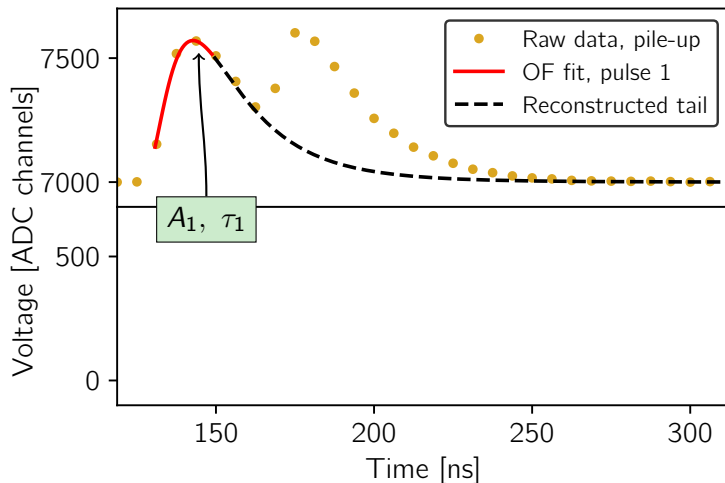
# New feature-extraction method

Modified OF



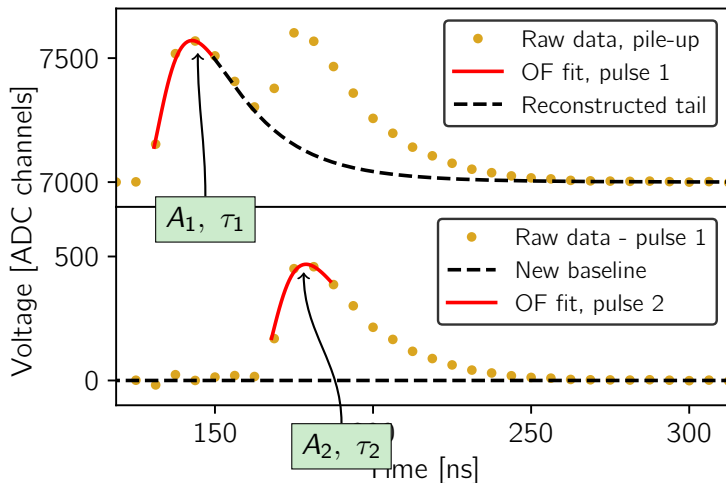
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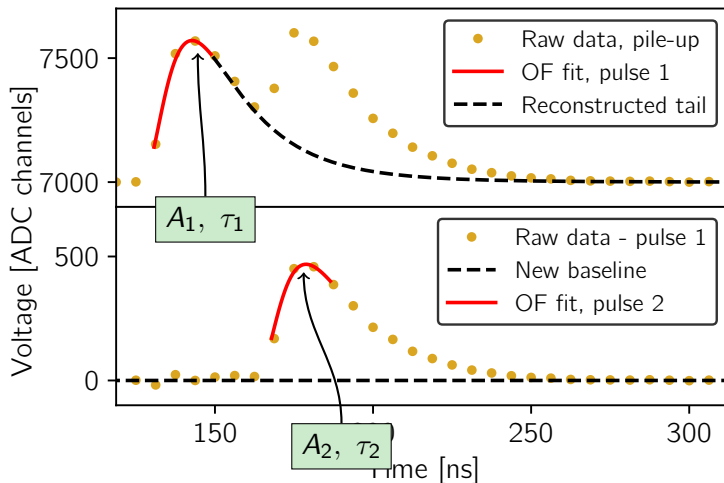
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Modified OF

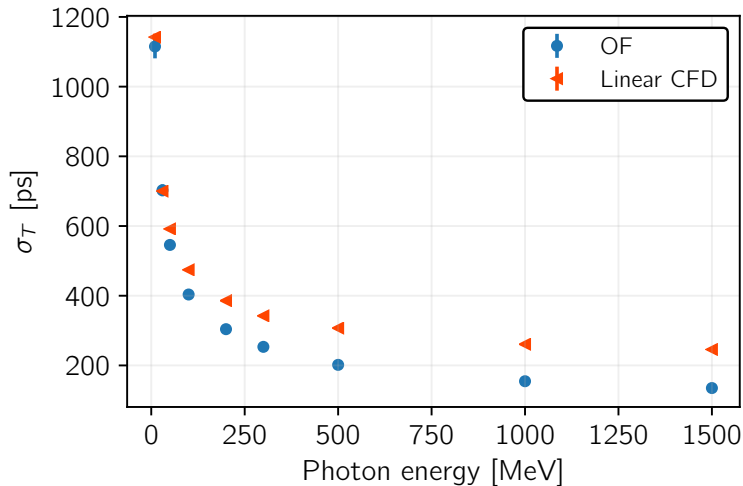


Model-generated data + VHDL implementation  $\Rightarrow$  evaluate method



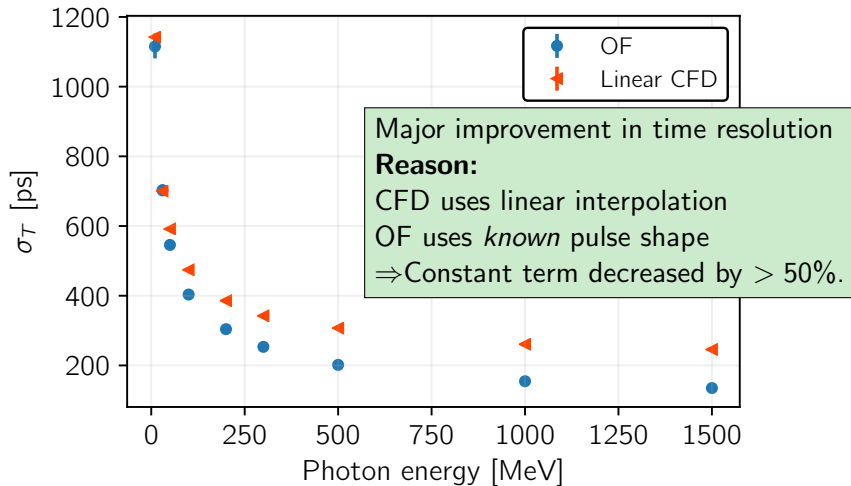
# New feature-extraction method

Time resolution — isolated pulse



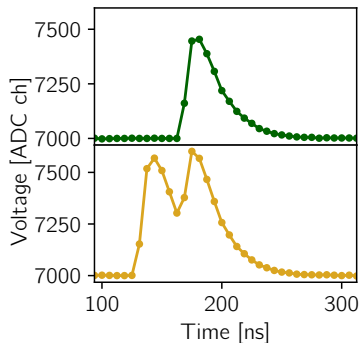
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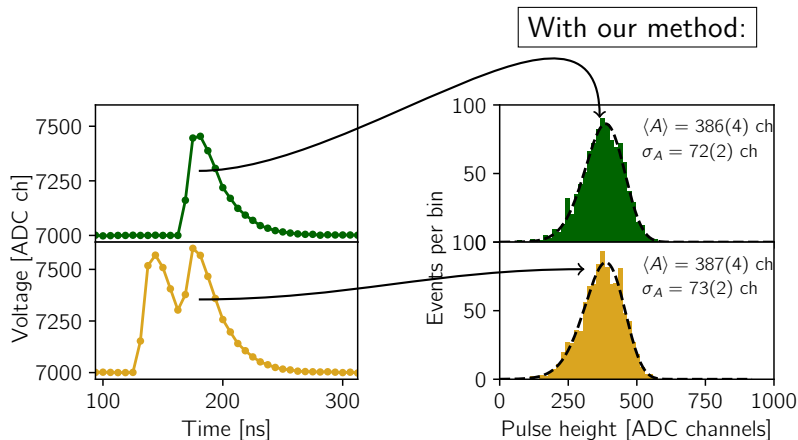
## Resolution under pile-up conditions



Without pile-up reconstruction:  
Expect biased pulse-height estimate  
on second pulse.

# New feature-extraction method

Resolution under pile-up conditions



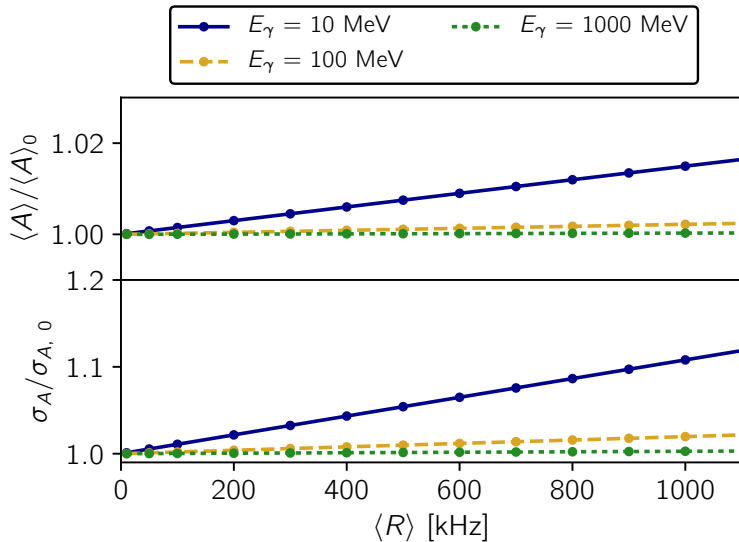
# New feature-extraction method

## Performance in the PANDA environment

1. PandaRoot Monte Carlo simulation of PANDA  $\Rightarrow$  energy deposition from “background events” in the detector.
2. Task: detect a particular photon ( $E_\gamma$ )
3. Study resolution and efficiency for different average rates  $\langle R \rangle$  in detector. Worst-case scenario:  $p_{\bar{p}} = 15 \text{ GeV}/c$ .

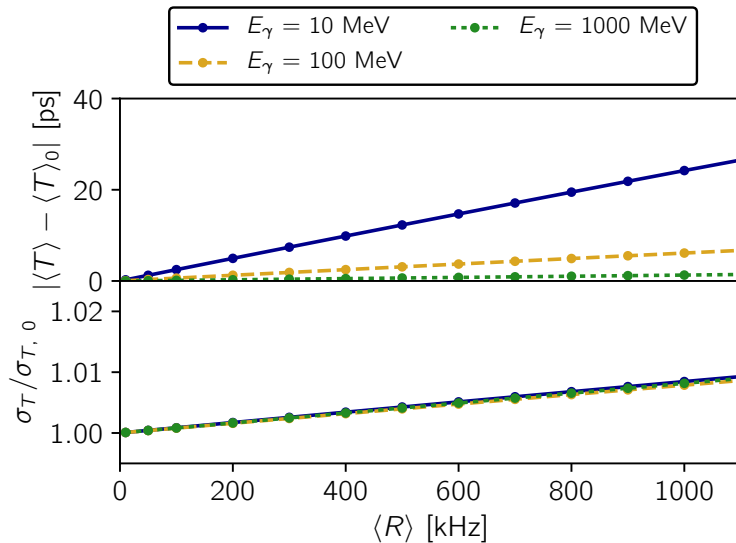
# New feature-extraction method

Pulse height resolution — pile-up pulse



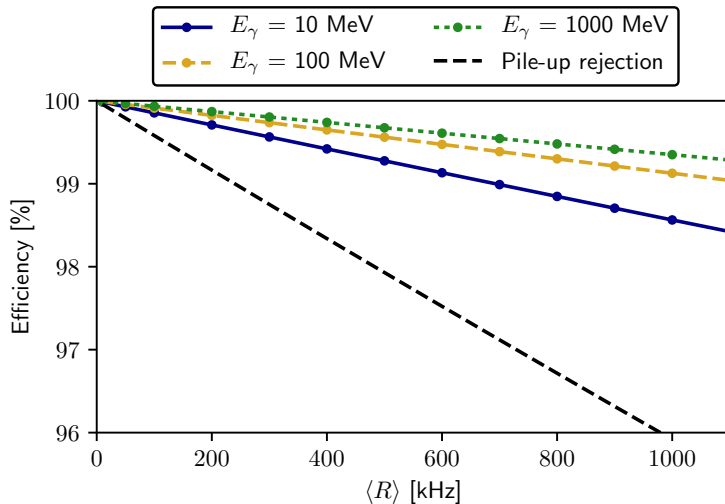
# New feature-extraction method

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# New feature-extraction method

Pulse-detection efficiency — pile-up pulse





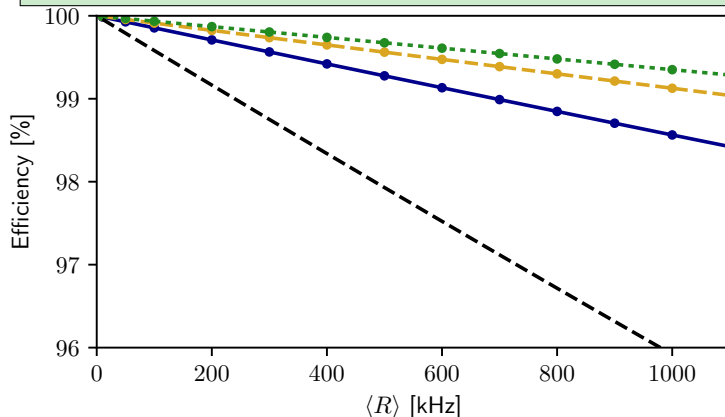
# New feature-extraction method

Pulse-detection efficiency — pile-up pulse

**Considerable improvement** (over pile-up rejection)

In PANDA: hit rates  $> 100$  kHz expected.

This method meets the requirements on pile-up reconstruction.



## Summary and outlook

- ▶ A real time method for feature extraction in the PANDA shashlyk calorimeter has been developed (digital CFD + OF).
- ▶ Implemented in VHDL simulation for use in FPGA.  
Benchmarked on model-generated signals.

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- ▶ Fulfills the PANDA requirements.
- ▶ Next steps:
  - ▶ Implement in FPGA.
  - ▶ Verify experimentally.

# Thank you for your attention!

Special thanks to the PANDA group at the University of Gießen for providing experimental data.

This work has been funded in part by the Swedish Research Council.