Report from
Panda DAQT and Frontend Workshop

Sören Lange (for the DAQT Group)

XXXIII Panda Collaboration Meeting
05/31-06/04, 2010
14-18 June 2010
Stockholm University

PANDA DAQT and FrontEnd Electronics Workshop, Rauischholzhausen Castle

14-17 April 2010 | Rauischholzhausen Castle, Germany

All talks are online:
https://indico.gsi.de/conferenceDisplay.py?confId=911

45 registered participants

- **Status of FEE**
  Rauischholzhausen and beyond
  → Plenary Talk by Igor Konorov
  Wedesday 15:45

- **Summary of the Open Discussion at Rauischholzhausen**
  Friday April 16
  → talk by S.L. in the Technical Board

- **This talk:**
  other topics on the Rauischholzhausen Workshop
  i.e. hardware and algorithms
  (non-FEE)

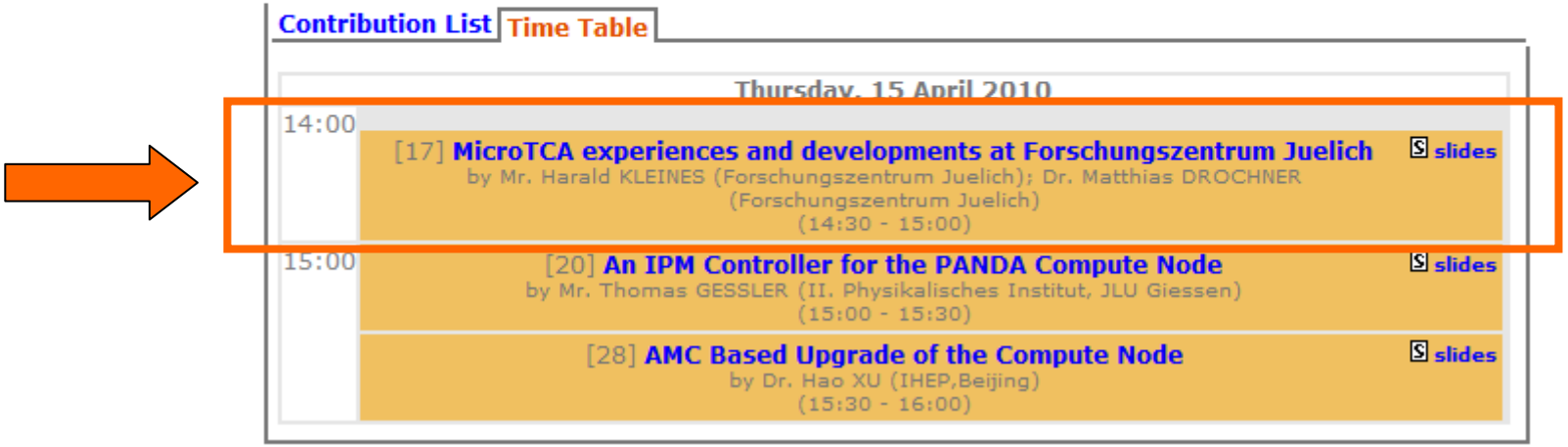
Trigger and DAQ

Hardware Developments

Trigger and Data Acquisition

Place: *Rauischholzhausen Castle, Germany*
http://www.uni-giessen.de/uni/einrichtungen/Rauischholzhausen/about.html

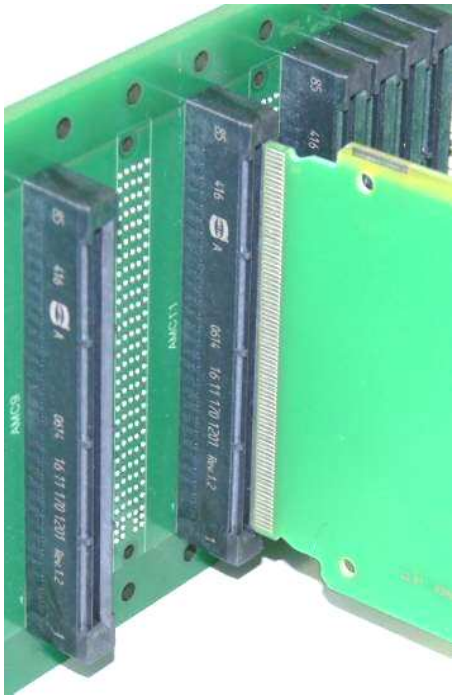
Dates: Thursday 15 April 2010 14:30



MicroTCA

Harald Kleines, Matthias Drochner, Jülich

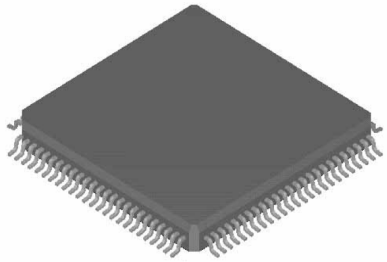
- Crate/Backplane system based on AMC
- Backplane:
  ≤12 slots, 170 pin
  - Common options:
    1000Base-BX, SATA
  - Fat pipe (x4):
    PCIe, SRIO, 10G-BASE-BX4
- But complex management analogous to ATCA
  - Module Management Controller (MMC)
  - I^2C



Development of a MicroTCA TDC Module

Harald Kleines, Matthias Drochner, Jülich

- First development: TDC Modul for STT (Straw Tube Tracker)
- **GPX ASIC** from *acam messelektronik gmh* in I-mode:
  - Well known from WASA developments
  - 8 channels
  - Bin-size: typ. 81 ps, dynamic range: 17 Bit
  - 32-fold multihit-capable,
    double pulse resolution ca. 5,5 ns
  - Peak rate: ca. 200 MHit/s
  - Continuous rate per channel: 10 MHit/s
- Change of the original plans:
  - 32 channels because of price/channel
  - Double width, compact size module
  - Self-Implementation of MMC on microcontroller



TQFP100

Status

Harald Kleines, Matthias Drochner, Jülich

- HW-Test
  - Microcontroller part works
- MMC software:
  - under development
- Still open:
  - FPGA code
- Future:
  CERN HPTDC under discussion for WASA DIRC
  → later module version with HPTDC possible

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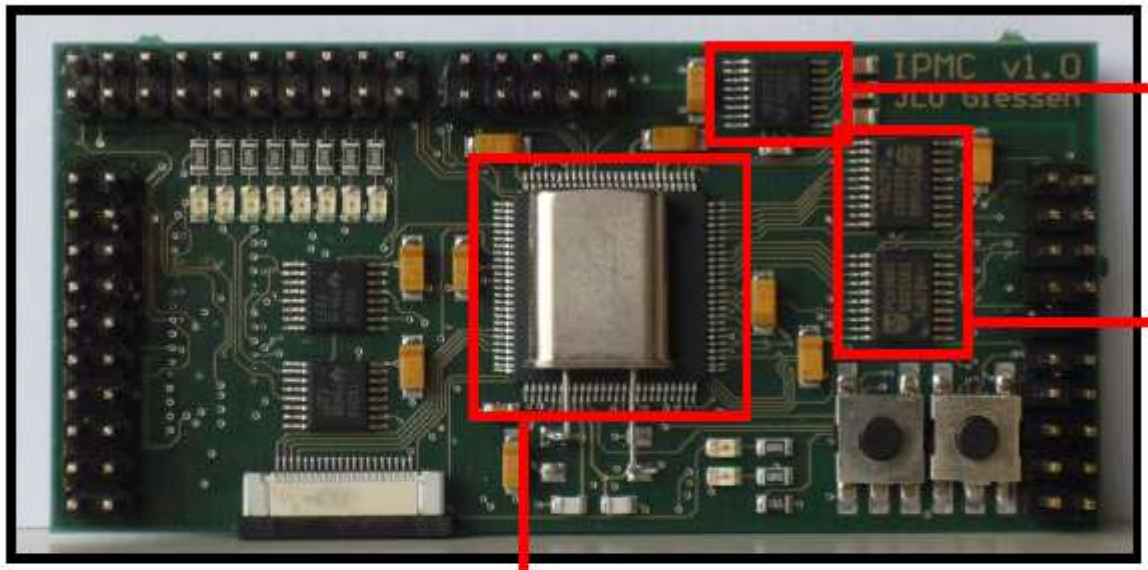
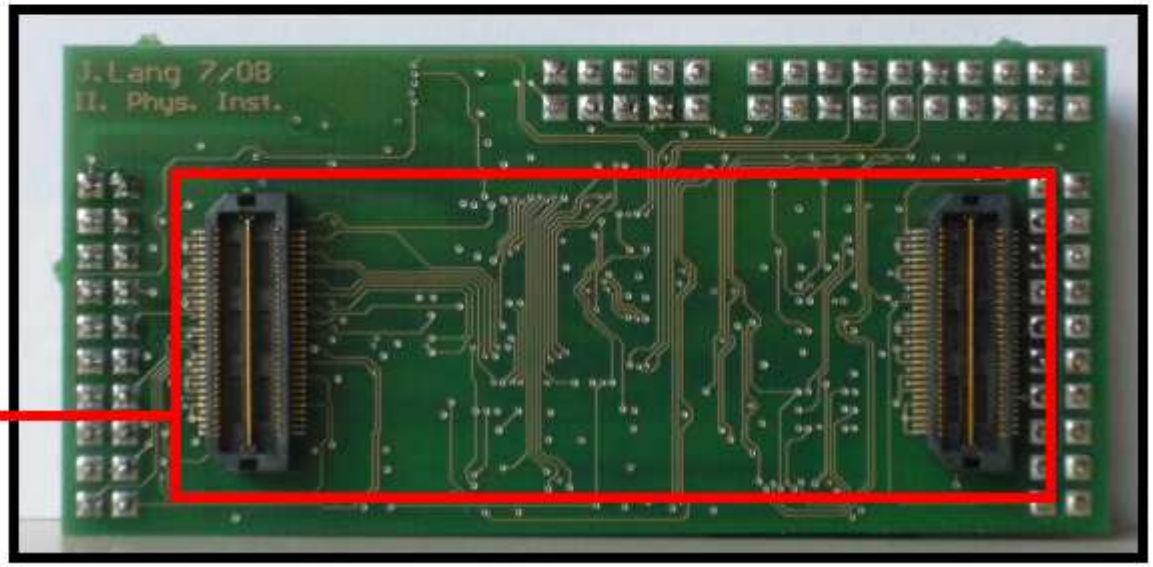
Assembled IPM Controller Prototype



UART Driver

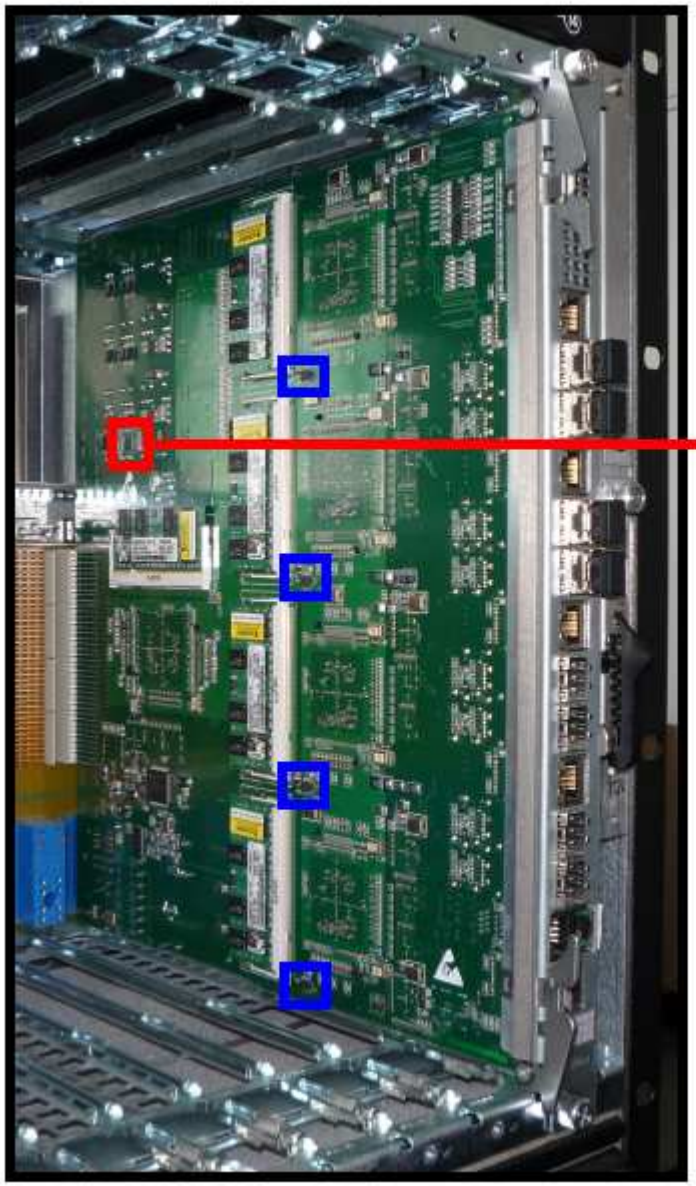
Parallel-to-I²C Controller

Microcontroller and 8MHz quartz



2 60-pin connectors

The Compute Node in the ATCA Shelf



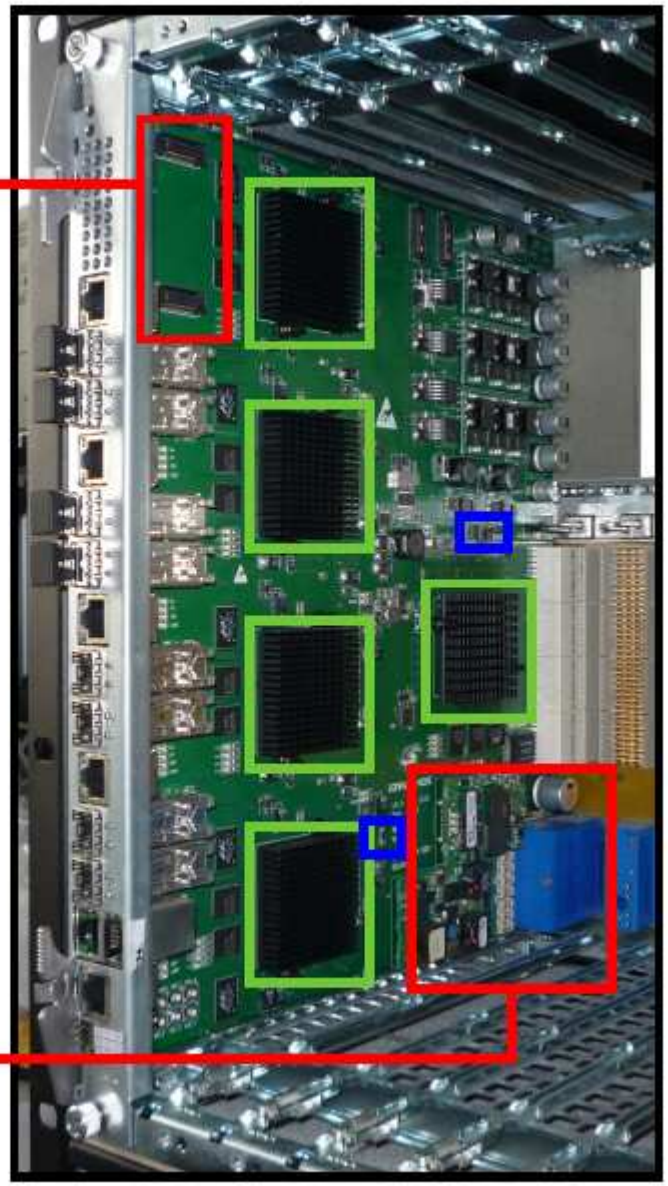
IPMC Connector

Voltage Sensor

FPGAs

Temperature Sensors

Power Supply



Status of the Firmware Development

- Firmware is being developed in C++ for the avr-gcc compiler.
- The microcontroller is programmed via a JTAG interface.
- A “command shell” was written for the PC serial interface.
- The I^2C interface controllers can be used.
- Temperature sensors on the Compute Node’s I^2C bus can be read out and programmed.

```
IPMC 1.0

ipmc>
ipmc> tmptest
Temp Sensor 1: 25 oC
Temp Sensor 2: 22 oC
Temp Sensor 3: 24 oC
Temp Sensor 4: 22 oC
Temp Sensor 5: 21 oC
Temp Sensor 6: 24 oC
Temp Sensor 7: 24 oC
Temp Sensor 8: 23 oC
Temp Sensor 9: 24 oC
ipmc>
```

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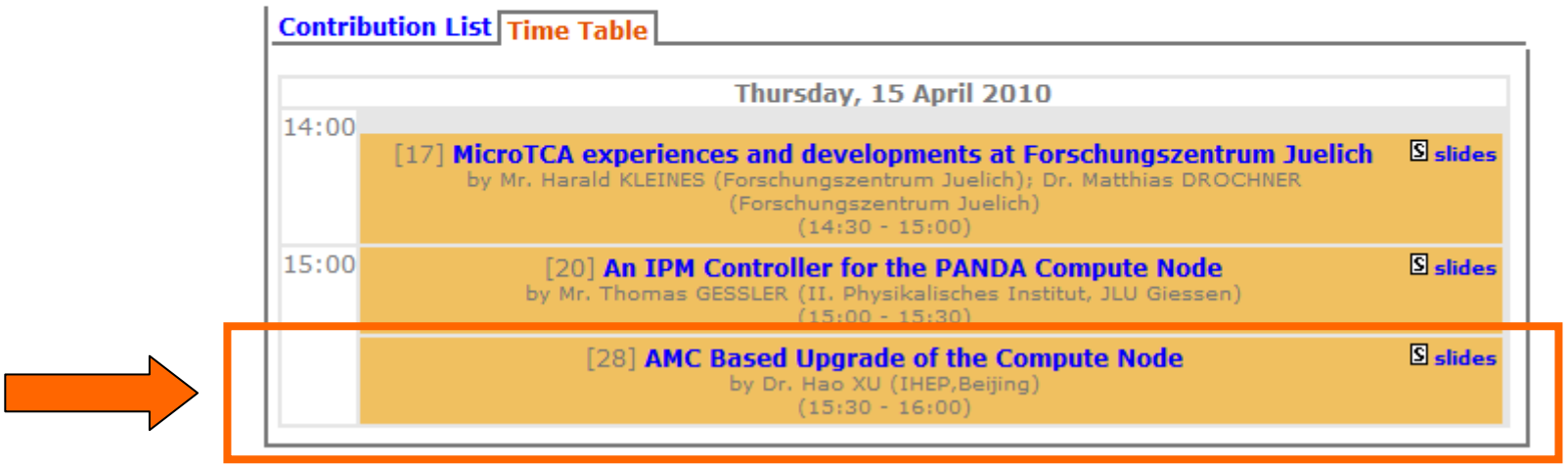
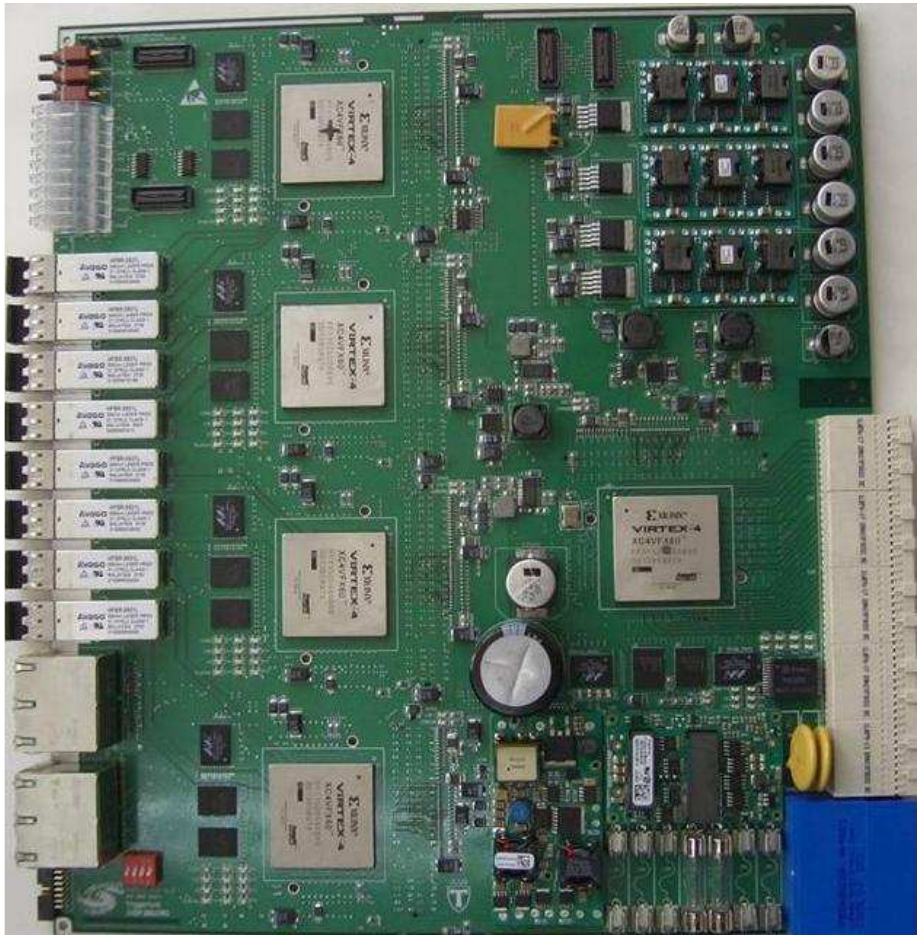
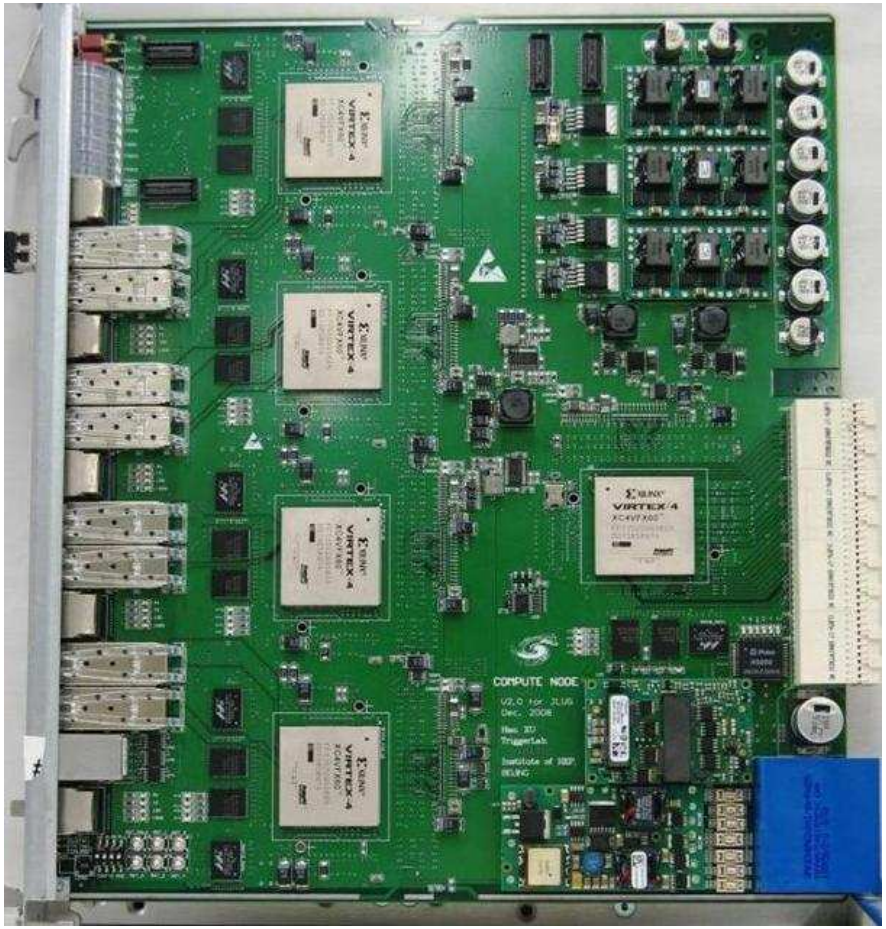




Compute Node
Version #1, 2008

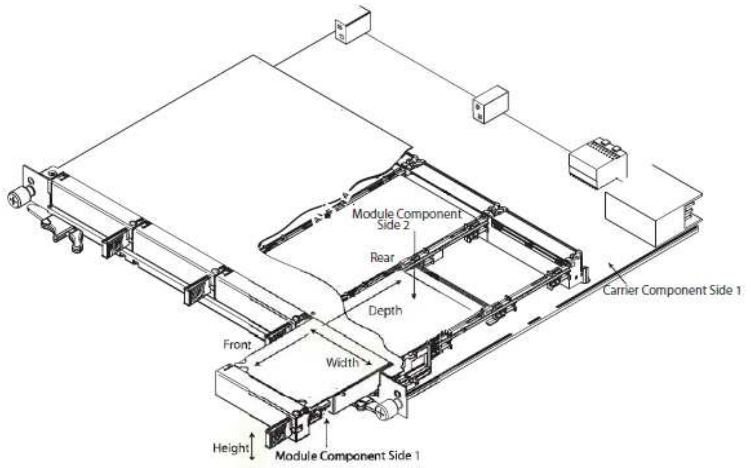


Compute Node
Version #2, 2009

New Compute Node Proposal by IHEP and Giessen

Hao Xu, IHEP
(presented by Qiang Wang, Giessen)

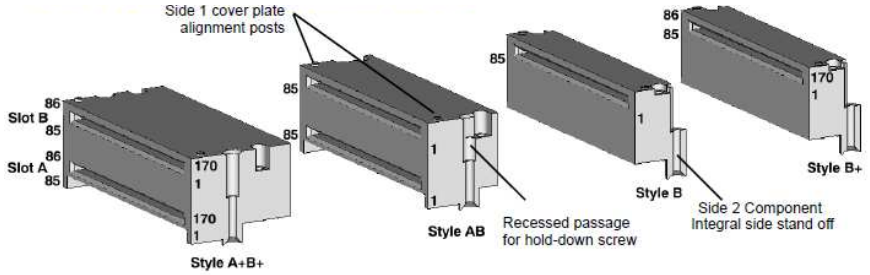
- New approach by IHEP group:
  Carrier Board w/ Advanced Mezzanine Cards
  follow AMC.0 R2.0 specification
  of PICMG
  PCI Industrial Computers Manufacturers Group
- formfactor 7.4 x 18.0 cm
- 4 add-on cards per 1 Compute Node



AdvancedMC Connector

Hao Xu, IHEP
(presented by Qiang Wang, Giessen)

- various connector mount types are available for all AMC Connector styles, B, B+, AB, and A+B+.
- fabric Interface
  - 40 signal pairs allocated to the Fabric Interface
- System Management Interface
  - 9 contacts allocated to the System Management Interface
- AMC Clock Interface
  - 5 signal pairs allocated to the AMC Clock Interface
- JTAG Test Interface
  - 5 contacts allocated to the JTAG Test Interface
- Power/ Ground
  - 8 contacts allocated to Payload Power
  - 56 contacts to allocated to Logic Ground
- 2 contacts reserved



Connector Style	Interface to AMC Module	Number of Module Slots	Number of contact positions to Carrier	Number of contact rows on Carrier	Differential pairs	General purpose contacts	Power contacts	Ground contacts
B	Basic	1	85	1	19	11	8	28
B+	Extended	1	170	2	45	16	8	56
AB	Basic	2	170	2	38	22	16	56
A+B+	Extended	2	340	4	90	32	16	112

From PICMG AMC.0 R2.0

Development of Carrier Board

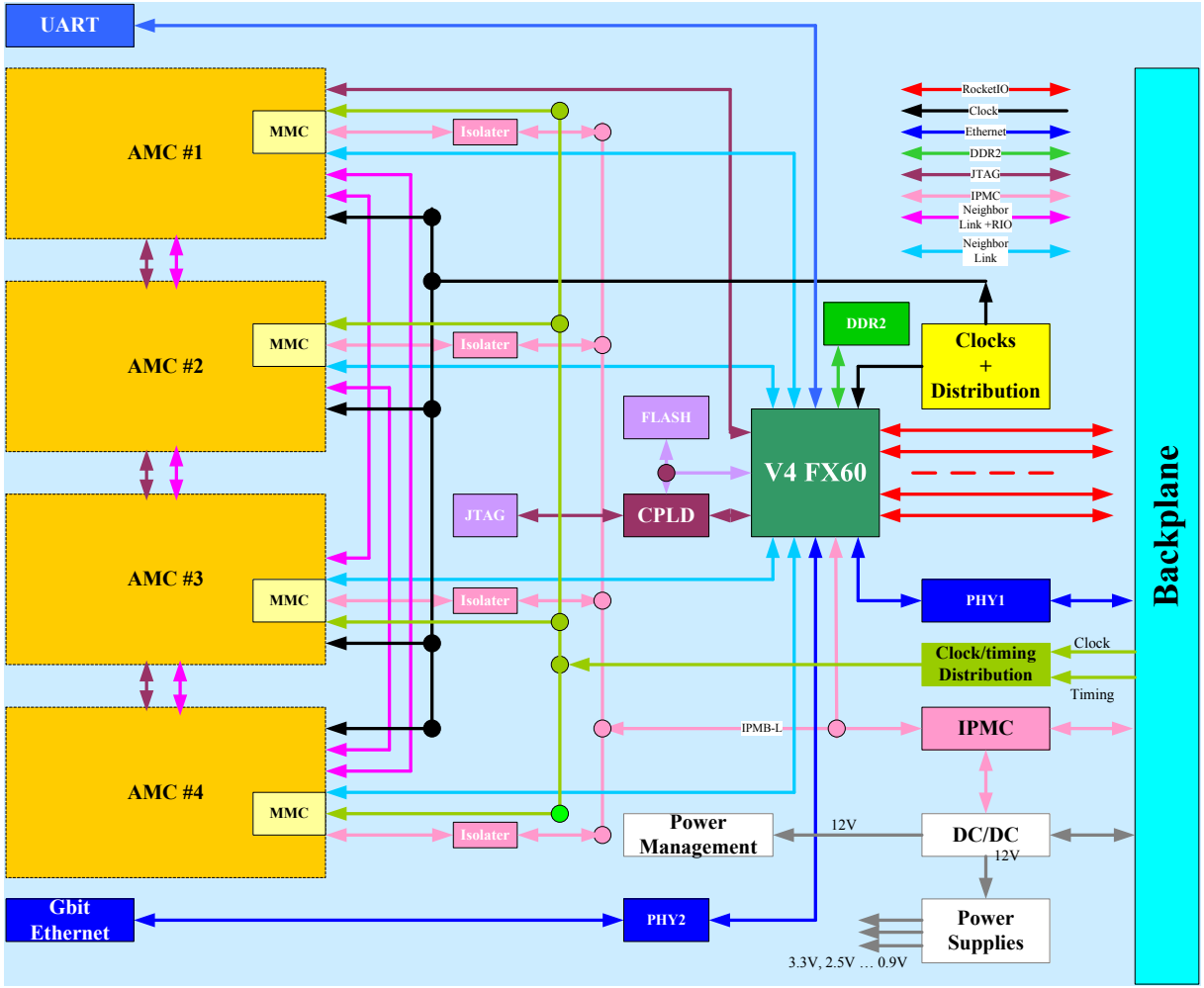
- Carrier Board with high bandwidth switch for neighbour-link
  - Virtex-4 FX60 based – functions test
    - 1 Virtex-4 FX60 FPGA
    - 2GB DDR2 SODIMM 400Mbps
    - 512Mb FLASH Memory
    - 13x RocketIOs @2Gbps to backplane
    - 2x Gbit Ethernet
    - **Schematic is ongoing, PCB will be delivered in June/July**
  - Virtex-6 based – high performance
    - 1 Virtex-6 FPGA
    - 2/ 4GB DDR3 SODIMM 800Mbps
    - 512Mb FLASH Memory
    - 13/26 RocketIOs @6.25Gbps to backplane
    - 2xGbit Ethernet

This PCB will be developed and existing in any case.

Hao Xu, IHEP
(presented by Qiang Wang, Giessen)

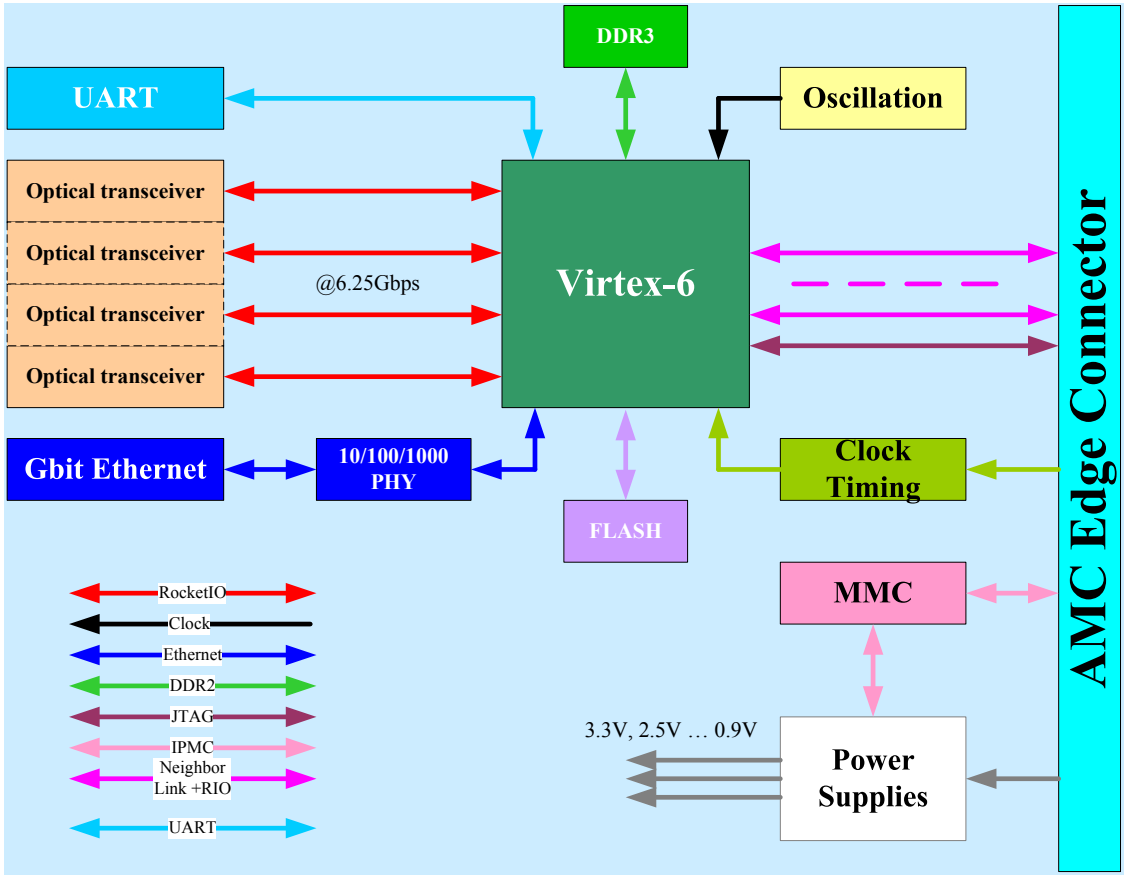
Carrier Board Rev.1

Hao Xu, IHEP
(presented by Qiang Wang, Giessen)



AMC Module 2, Virtex-6 based

Hao Xu, IHEP
(presented by Qiang Wang, Giessen)



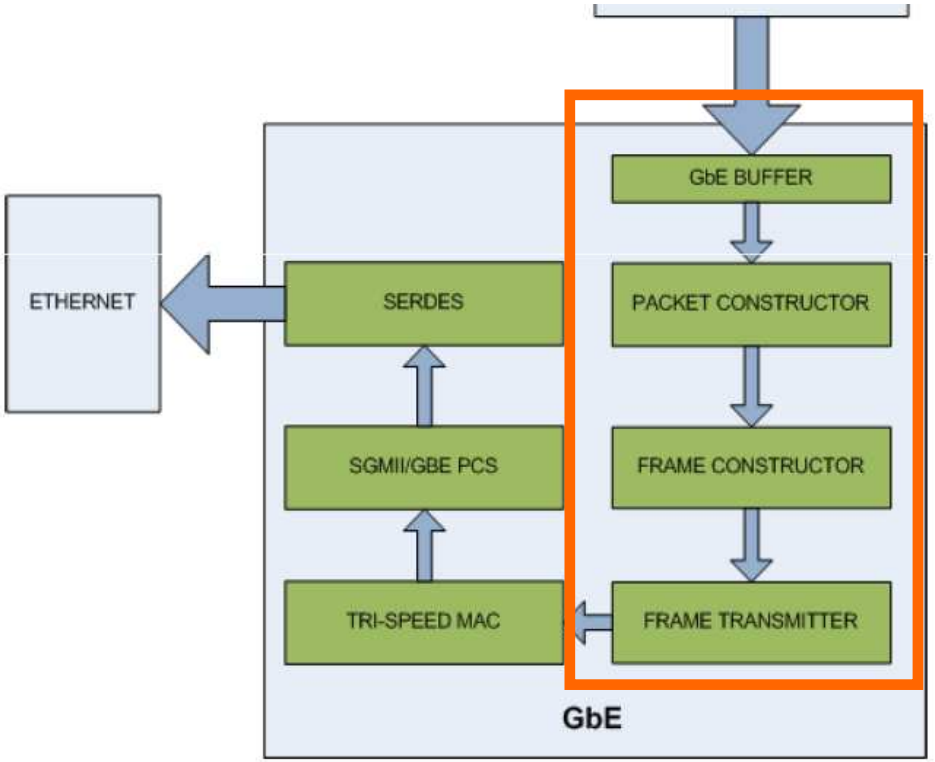
Trigger and Data Acquisition II

Place: *Rauischholzhausen Castle, Germany*
http://www.uni-giessen.de/uni/einrichtungen/Rauischholzhausen/about.html

Dates: Friday 16 April 2010 12:57

Grzegorz Korcyl - Jagiellonian University, Kraków

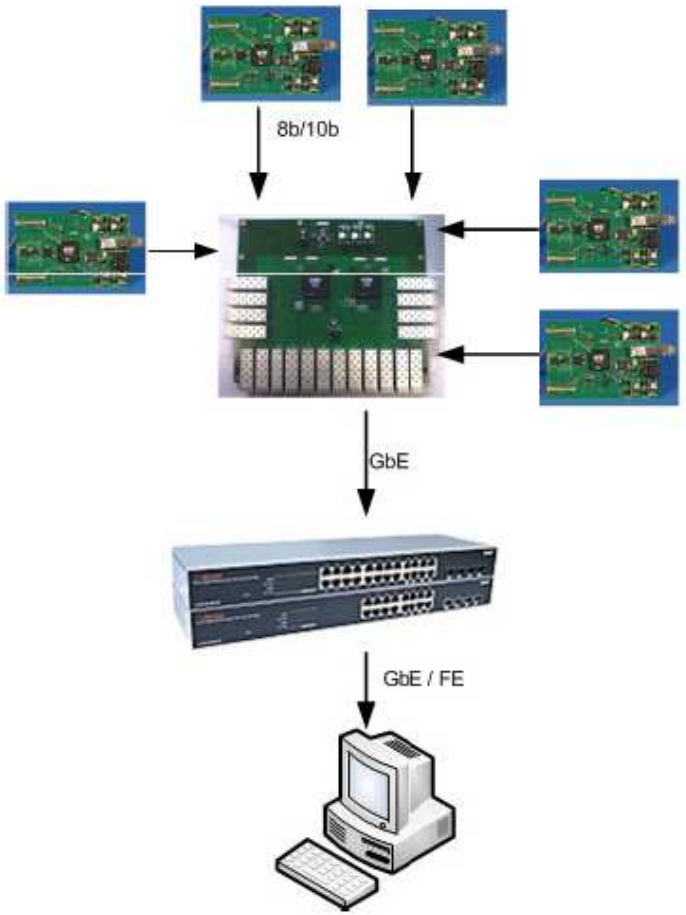
Resource	Utilization	Percentage
Slices	4256 out of 47376	8%
LUTs	5984 out of 95000	6%
Blocks RAM	76 out of 288 (~150kB)	26%



Lattice ECP2M LFE2M100E

3.b Results – setup 2

- 5x ADCM data sources
- HUBv2
- Longshine optical GbE switch
- One event builder
- Triggering by generator



Grzegorz Korcyl – PANDA TDAQ Workshop, Giessen April 2010

3.b Results – setup 2

- Packet size 38.8kB
- Accepted event rate 1.25kHz and 49MB/s throughput
- Long-lasting and stable connection

	Old DAQ	New DAQ	Factor
Bandwith to Event builder	6 MB/s	150 MB/s	25x faster
Event rate / sector	50 Hz	1.25 kHz	25x faster
Throughput / sector	1 MB/s	49 MB/s	50x faster

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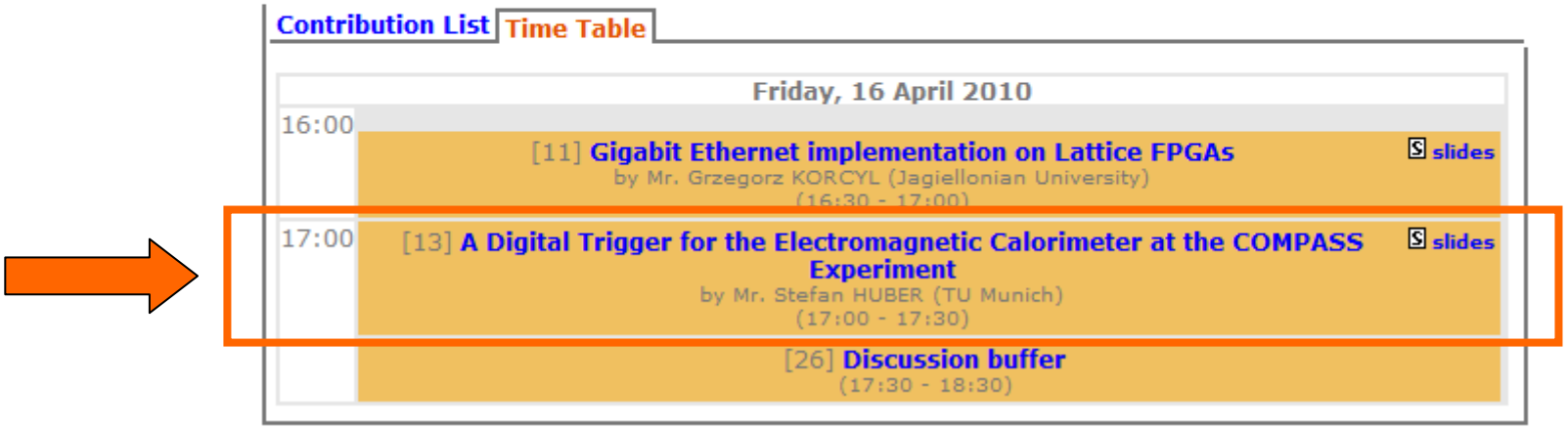


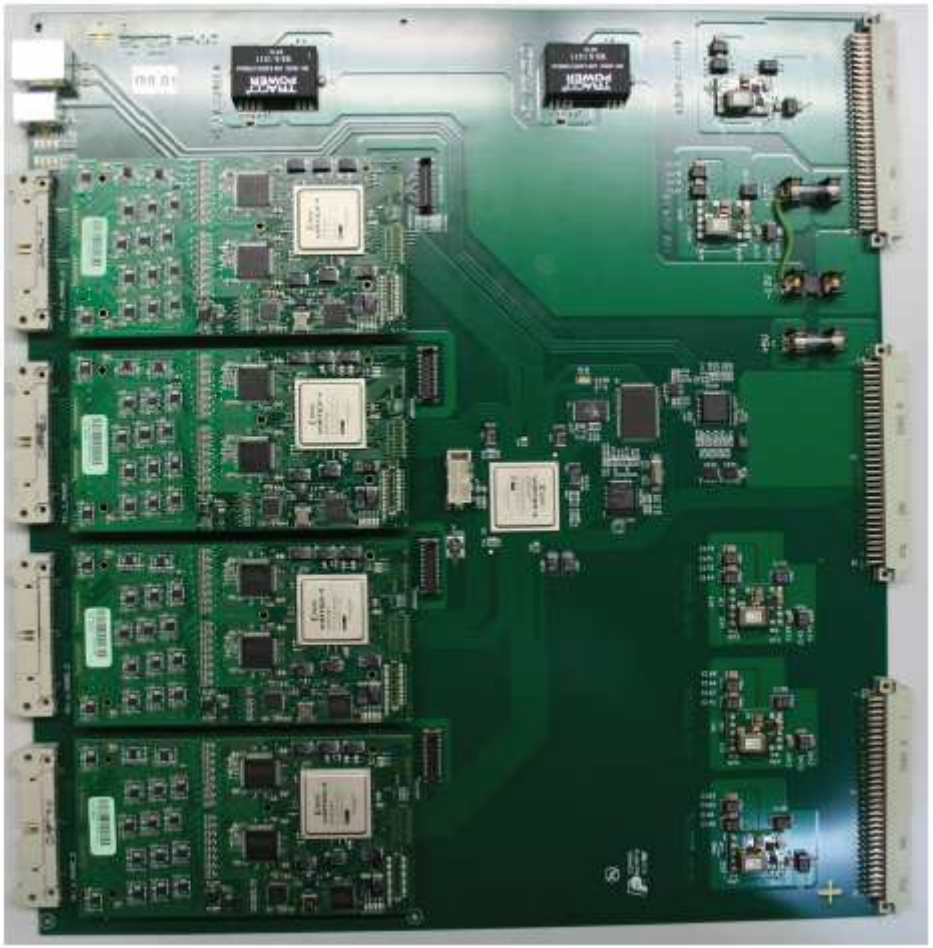
MSADC card

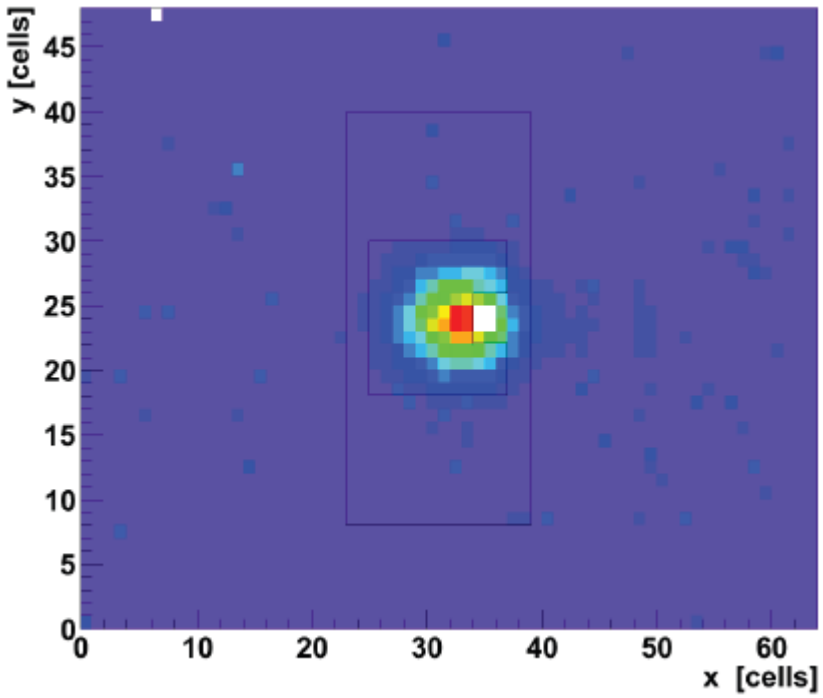
- 16 Channels with 12 bit resolution
- 2 ADCs per channel (interleaved) $\Rightarrow$ 80 MS/s
- Virtex4 LX25
  - Digitization
  - Interleaving
  - Multiplexing
  - Zerosupression
  - Formatting

Carrier Card

- Powersupply via VME
- Combines 4 MSADCs
- Multiplexer
- I^2C Interface
- Transmitting of the data
- Connection via USB, RJ45, JTAG and VME

Stefan Huber, TU München,
Digital EMC Trigger at COMPASS



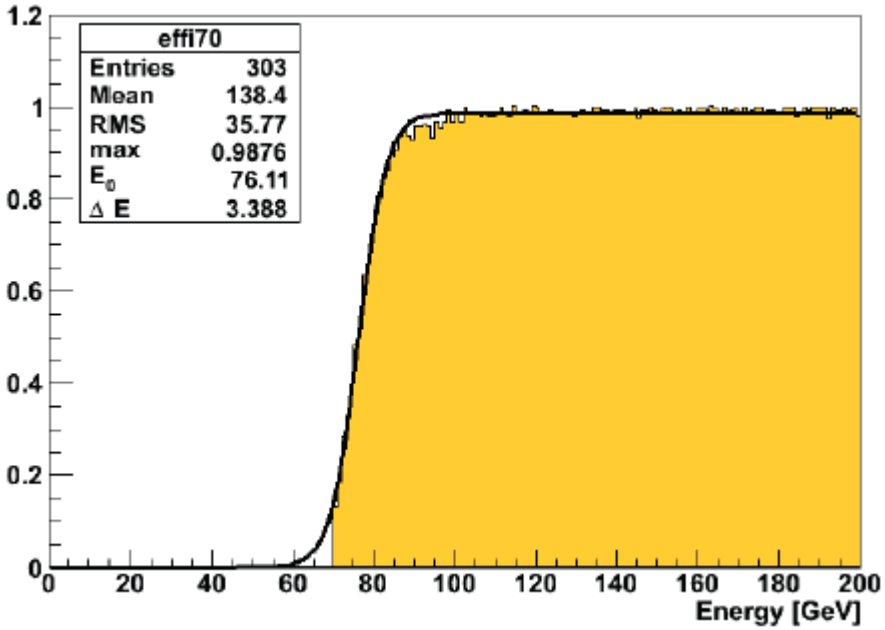


Stefan Huber, TU München,
Digital EMC Trigger at COMPASS

- Beamrate $2.5 \cdot 10^6$/s
- Triggerrates:
  - $40 \cdot 10^3$/s @ 50 GeV
  - $23 \cdot 10^3$/s @ 70 GeV
- Energy resolution ≈ 3.4 GeV

Online

- Determination of the Pedestals
- Signaldetection
- Signaltime
- Calculation of the Energy
- Alignment in time
- **Sum up all channels**



Algorithms

Algorithms

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Dates: Friday 16 April 2010 06:30

Contribution List | Time Table

Friday, 16 April 2010

09:00	[2] **Development of PANDA EMC Online High Level Trigger Algorithms** by Mr. Qiang WANG (II. Physikalisches Insitut,JLU Gießen) (09:00 - 09:30)	slides
	[3] **A FPGA helix tracking algorithm for PANDA** by David MüNCHOW (II. Physikalisches Institut, Universität Gießen) (09:30 - 10:00)	slides
10:00	[5] **Thoughts on analysing photon hit patterns from Disc DIRC detectors** by Dr. Klaus FöHL (Universität Gießen) (10:00 - 10:30)	slides
11:00	[1] **A Reconfigurable Design Framework for FPGA Adaptive Computing** by Mr. Ming LIU (II. Physik Institut, Uni-Giessen) (11:00 - 11:30)	slides
	[22] **GPU's for event reconstruction** by Dr. Mohammad AL TURANY (GSI) (11:30 - 12:00)	slides
12:00	[24] **Discussion Buffer** (12:00 - 12:30)	

Q. Wang, Giessen

An overlapped cluster

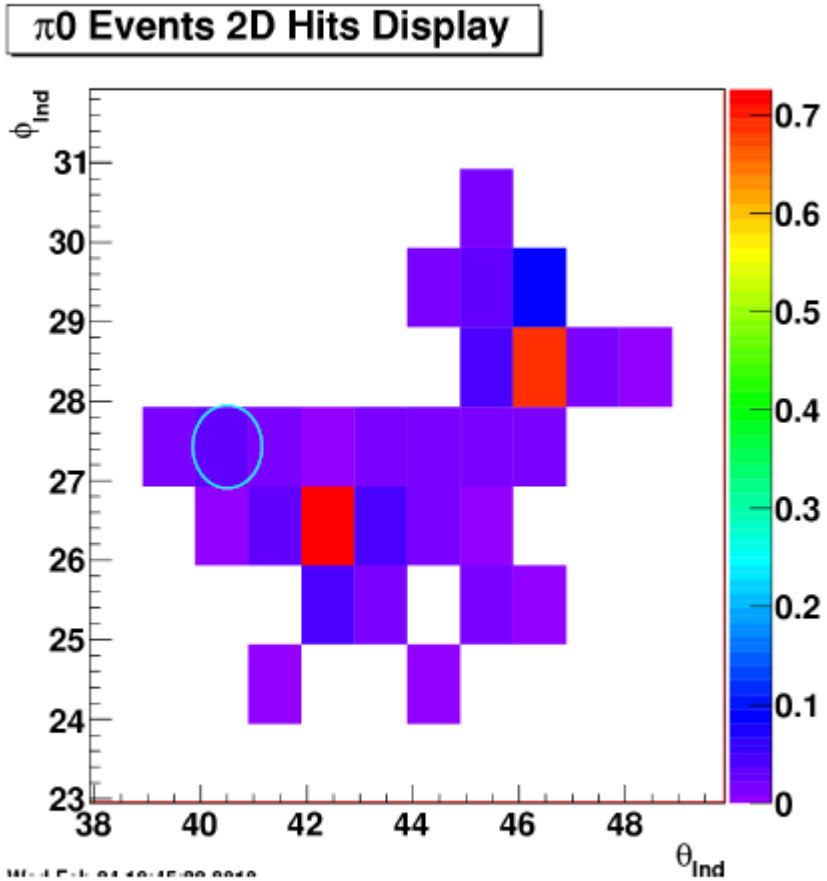

Fig. Three local maximums in the same cluster found which is considered as a real overlapped cluster.

Start Cluster Finding for Event:10,total Hit:27.
New cluster Found,start hit:Dx 27,Dy 39,from Entry:162,Energy 11.
Member Hit:Dx 26,Dy 40,Energy 3.
Member Hit:Dx 27,Dy 40,Energy 33.
Member Hit:Dx 26,Dy 41,Energy 22.
Member Hit:Dx 27,Dy 41,Energy 6.
Member Hit:Dx 27,Dy 40 is Local Maximum.
Member Hit:Dx 25,Dy 42,Energy 44.
Member Hit:Dx 26,Dy 42,Energy 719.
Member Hit:Dx 27,Dy 42,Energy 5.
Member Hit:Dx 25,Dy 43,Energy 9.
Member Hit:Dx 26,Dy 43,Energy 47.
Member Hit:Dx 24,Dy 41,Energy 3.
Member Hit:Dx 27,Dy 43,Energy 10.
Member Hit:Dx 26,Dy 42 is Local Maximum.
Member Hit:Dx 26,Dy 44,Energy 18.
Member Hit:Dx 27,Dy 44,Energy 8.
Member Hit:Dx 25,Dy 45,Energy 10.
Member Hit:Dx 26,Dy 45,Energy 2.
Member Hit:Dx 27,Dy 45,Energy 19.
Member Hit:Dx 28,Dy 45,Energy 40.
Member Hit:Dx 25,Dy 46,Energy 3.
Member Hit:Dx 27,Dy 46,Energy 6.
Member Hit:Dx 28,Dy 46,Energy 690.
Member Hit:Dx 29,Dy 46,Energy 86.
Member Hit:Dx 29,Dy 45,Energy 25.
Member Hit:Dx 29,Dy 44,Energy 10.
Member Hit:Dx 28,Dy 47,Energy 11.
Member Hit:Dx 28,Dy 46 is Local Maxum.
Member Hit:Dx 30,Dy 45,Energy 18.
Member Hit:Dx 28,Dy 48,Energy 3.

Q. Wang, Giessen

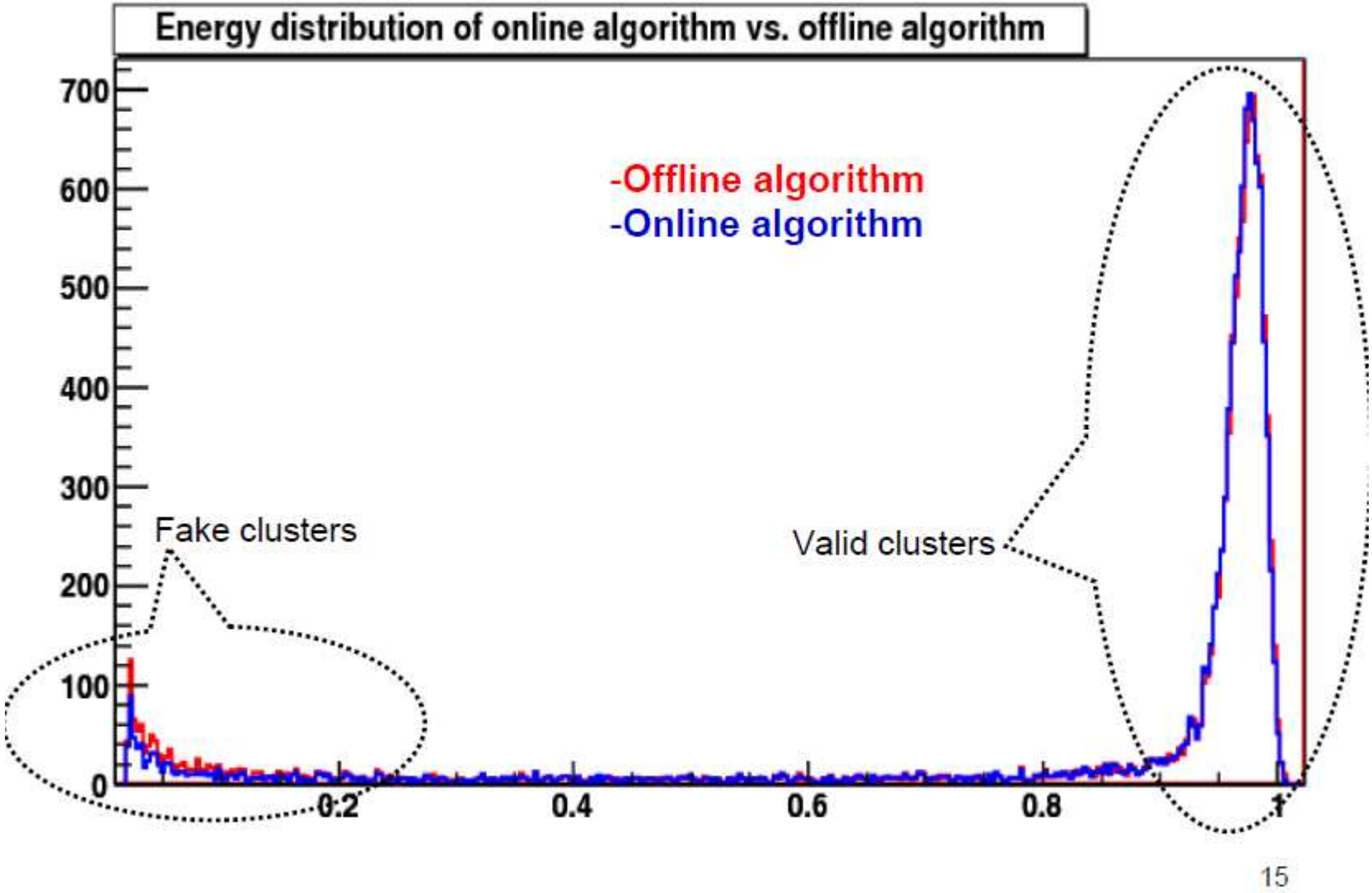

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Fig. 10k single gamma event, theta:22°~140°(Only barrel part)

Q. Wang, Giessen

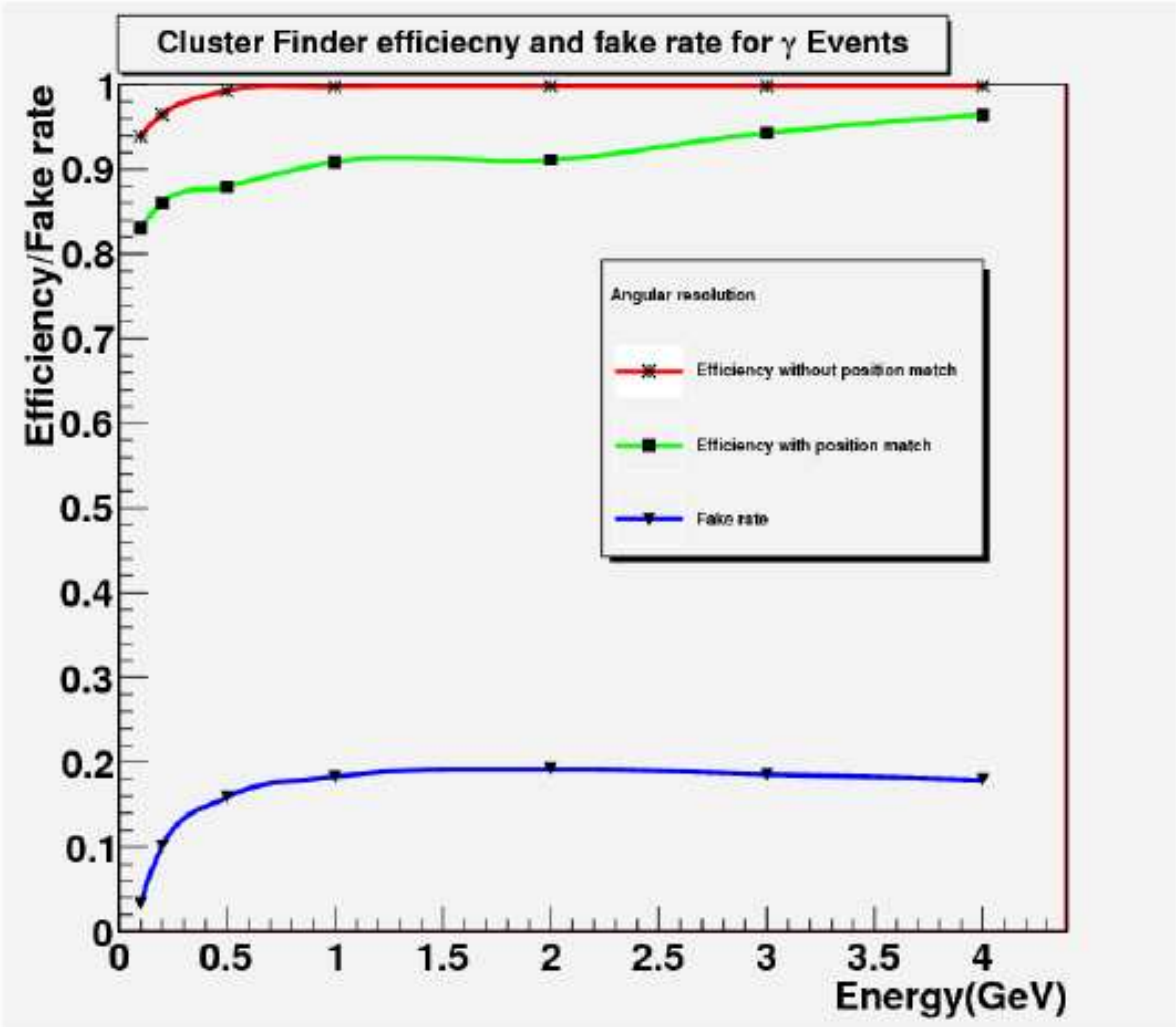

Fig. Cluster finder efficiency and fake rate check at different energy (10K gamma events at energy point)

Algorithms

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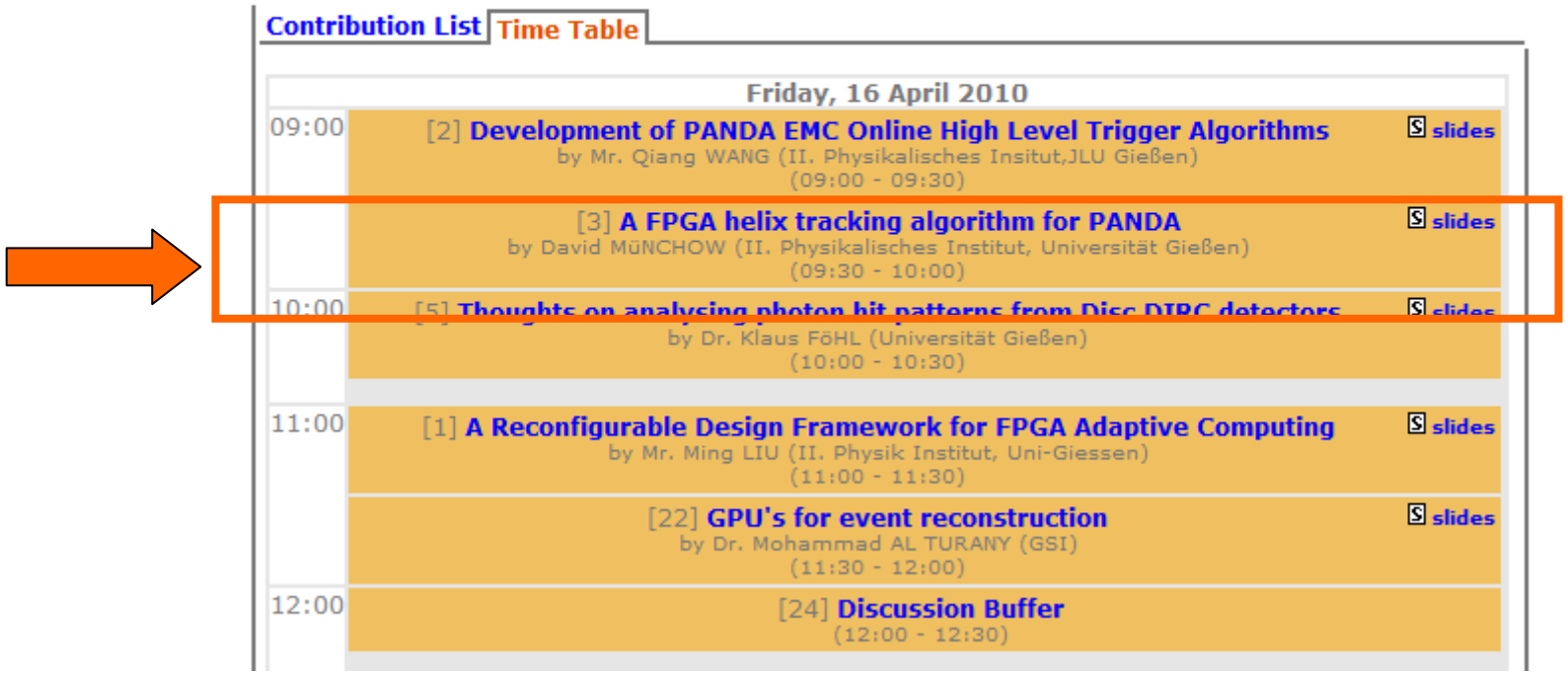

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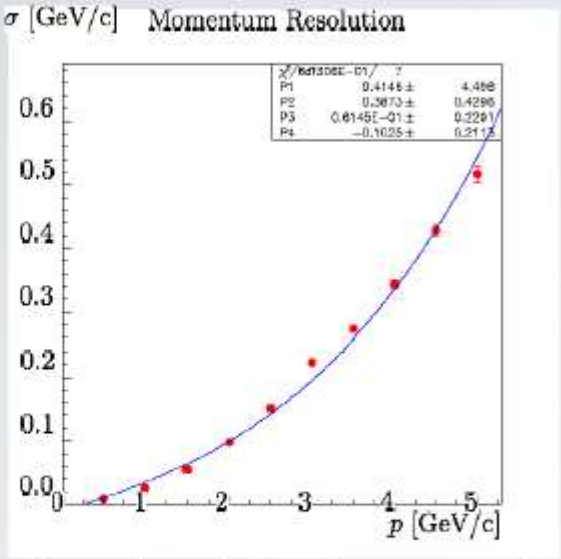
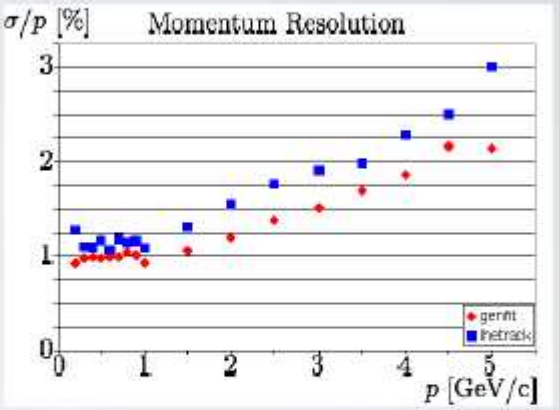
D. Münchow, Giessen

Momentum Resolution





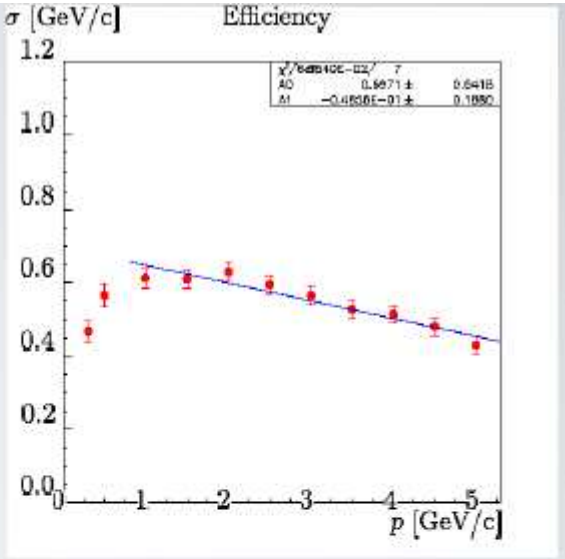
Stefano Spataro

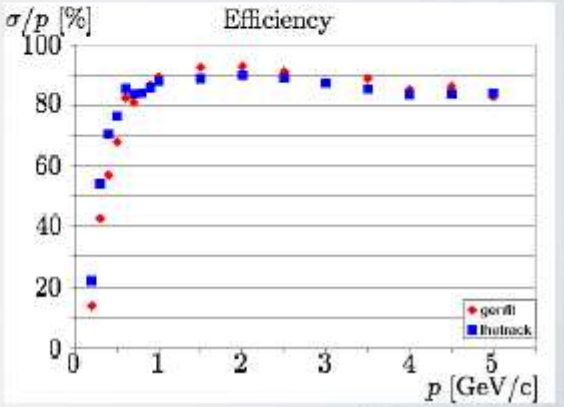
- With online algorithm between 3% (1 GeV/c) and 14% (5 GeV/c)
- With offline analysis framework (PandaRoot) between 1% (1 GeV/c) and 3% (5 GeV)

D. Münchow, Giessen

Efficiency

- Linear decreasing for Momentum over 1 GeV/c
- With online algorithm between 61% (1 GeV/c) and 43% (5 GeV/c)
  → further work required
- With PandaRoot between 90% (1 GeV/c) and 85% (5 GeV)
- Efficiency loss for momentum smaller 1 GeV/c
  - 46% at 0.3 GeV/c (online algorithm)
  - 20% at 0.3 GeV/c (PandaRoot)





Stefano Spataro

Implementation on FPGA ongoing

Algorithms

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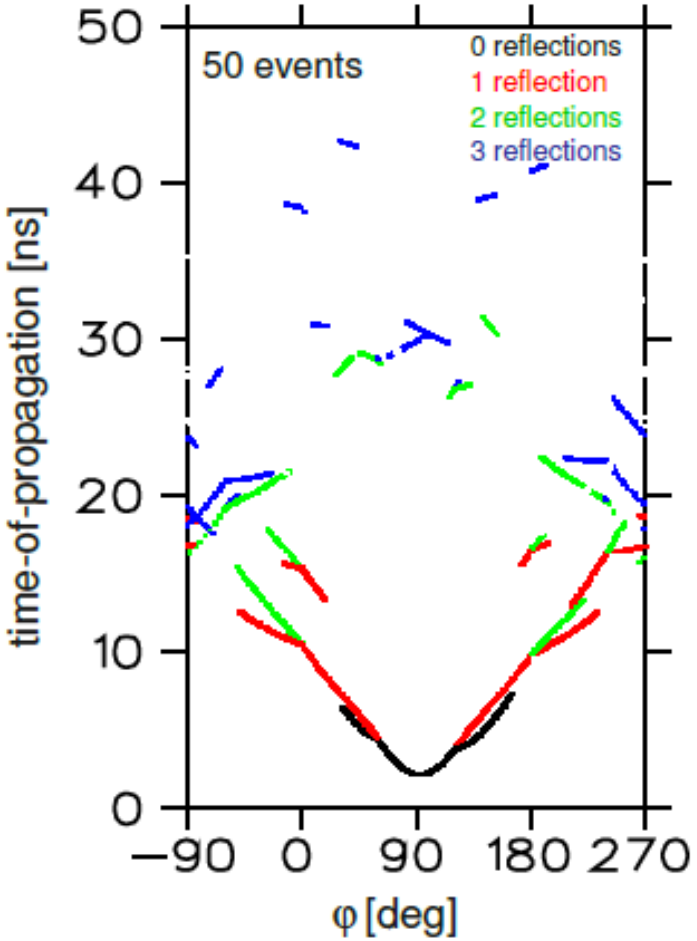
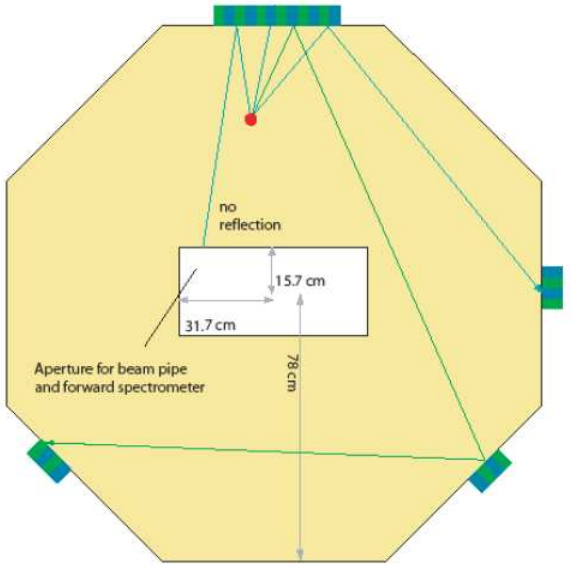
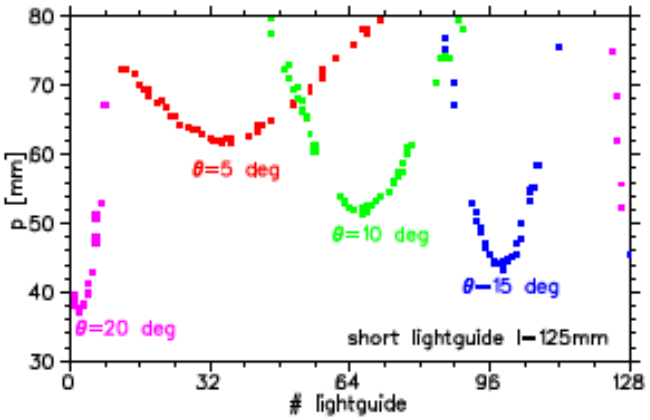
12:00	[24] **Discussion Buffer** (12:00 - 12:30)	

Klaus Föhl, Giessen

Time-of-Propagation







Algorithms

Place: *Rauischholzhausen Castle, Germany*
http://www.uni-giessen.de/uni/einrichtungen/Rauischholzhausen/about.html
Dates: Friday 16 April 2010 06:30

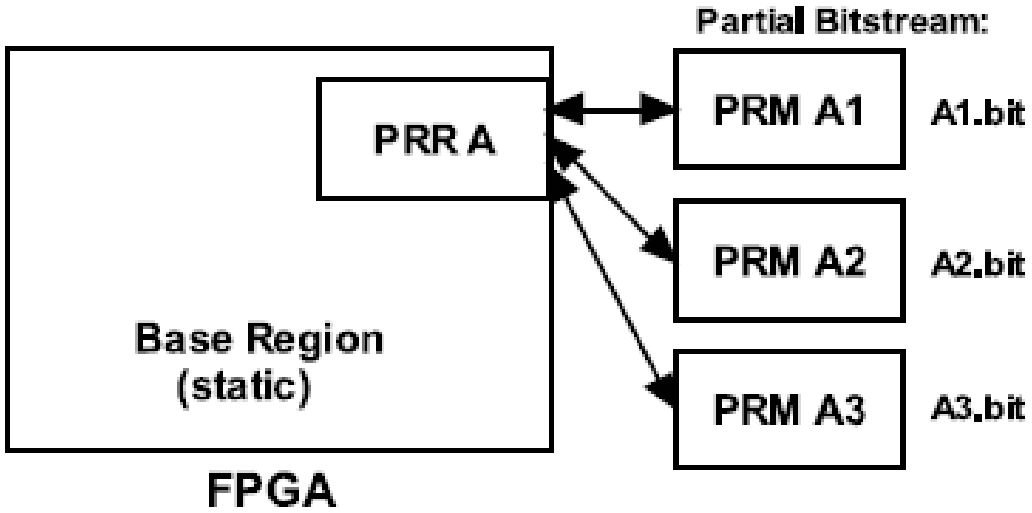
Contribution List | Time Table

Friday, 16 April 2010

09:00	[2] **Development of PANDA EMC Online High Level Trigger Algorithms** by Mr. Qiang WANG (II. Physikalisches Insitut,JLU Gießen) (09:00 - 09:30)	slides
	[3] **A FPGA helix tracking algorithm for PANDA** by David MüNCHOW (II. Physikalisches Institut, Universität Gießen) (09:30 - 10:00)	slides
10:00	[5] **Thoughts on analysing photon hit patterns from Disc DIRC detectors** by Dr. Klaus FöHL (Universität Gießen) (10:00 - 10:30)	slides
11:00	[1] **A Reconfigurable Design Framework for FPGA Adaptive Computing** by Mr. Ming LIU (II. Physik Institut, Uni-Giessen) (11:00 - 11:30)	slides
	[22] **GPU's for event reconstruction** by Dr. Mohammad AL TURANY (GSI) (11:30 - 12:00)	slides
12:00	[24] **Discussion Buffer** (12:00 - 12:30)	

Partial Reconfiguration Technology

Ming Liu, Gießen



- PR Region (PRR) dynamically loaded with different design modules (partial bitstreams)
- Designs can be switched in the system run-time for different algorithms
- HW resources are multiplexed by different PR Modules (PRM)

Algorithms

Place: *Rauischholzhausen Castle, Germany*
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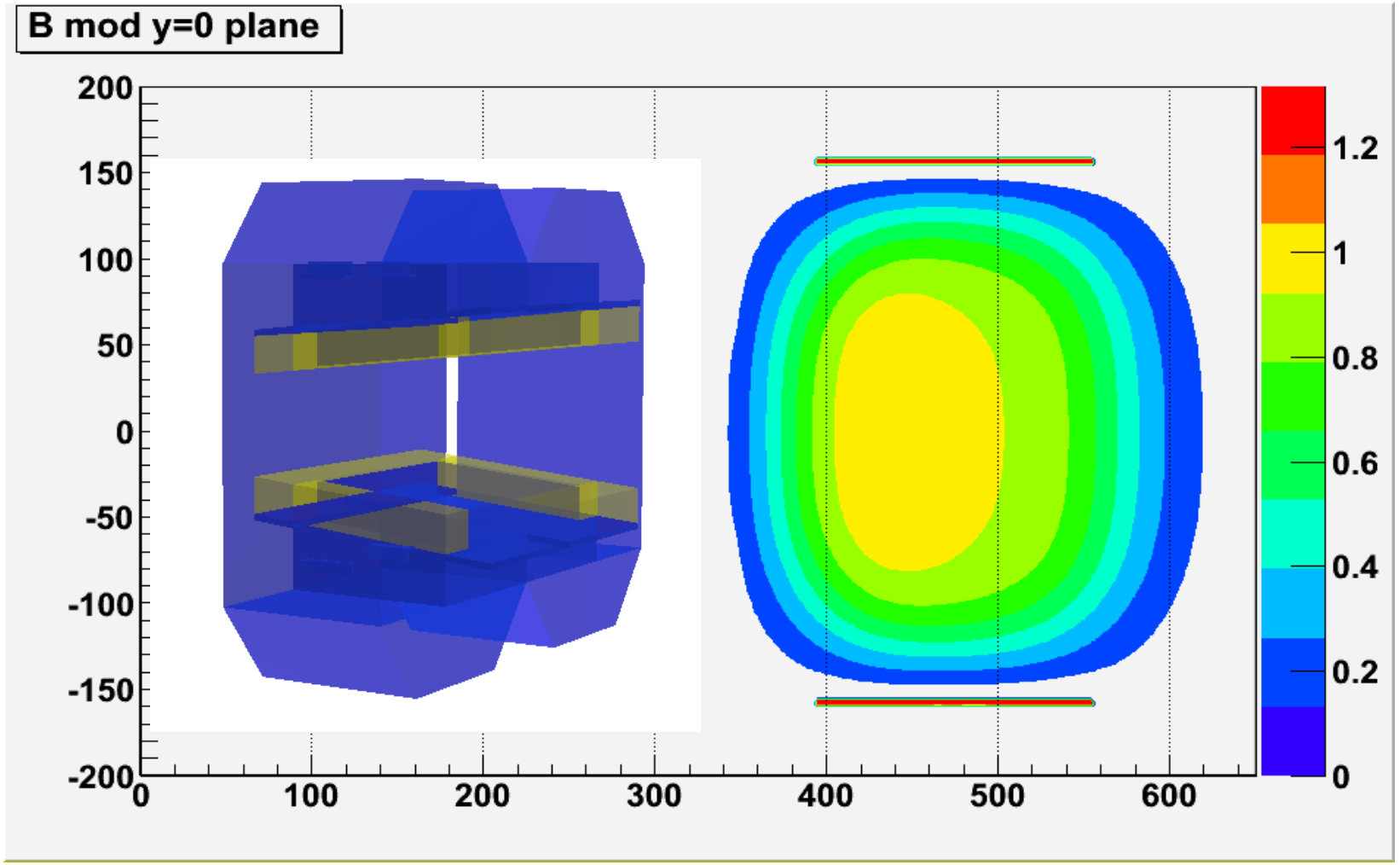
Runge-Kutta propagator

M. Al-Turany, GSI

- The Geant3 Runge-Kutta propagator was re-written inside a nVidia CUDA kernel
  - Runge-Kutta method for tracking a particle through a magnetic field.
    Nystroem algorithm
    (See Handbook Nat. Bur. Of Standards, procedure 25.5.20)
- The algorithm it self is hardly parallelizable, but one can propagate all tracks in an event in parallel
- For each track, a block of 8 threads is created, the particle data is copied by all threads at once, then one thread do the propagation

Magnet and Field

M. Al-Turany, GSI



Cards used in this Test

M. Al-Turany, GSI

	Qaudro NVS 290	GeForce 8400 GT	GeForce 8800 GT	Tesla C1060
CUDA cores	16 (2 x 8)	32 (4 x 8)	112 (14 x 8)	240 (30 x 8)
Memory (MB)	256	128	512	4000
Frequency of processor cores (GHz)	0.92	0.94	1.5	1.3
Compute capability	1.1	1.1	1.1	1.3
Warps/Multiprocessor	24	24	24	32
Max. No. of threads	1536	3072	10752	30720
Max Power Consumption (W)	21	71	105	200

Time needed to analyze one event in ms

M. Al-Turany, GSI