Storage-Ring Vacuum Solution for the EXL Silicon Particle Array

Branislav STREICHER[1)2)], Peter EGELHOF[1)], Vladimir EREMIN[3)], Stoyanka ILIEVA[1)], Nasser KALANTAR[2)], Holger KOLLMUS[1)], Jens Volker KRATZ[4)], Manfred MUTTERER[1)5)], Mirko VON SCHMID[5)], Michael TRÄGER[1)]

for the EXL collaboration

1) GSI Darmstadt, 2) KVI Groningen, 3) PTI St. Petersburg, 4) Universität Mainz, 5) TU Darmstadt

EMMI
workshop

Physics Prospects at the ESR and HITRAP
Eisenach
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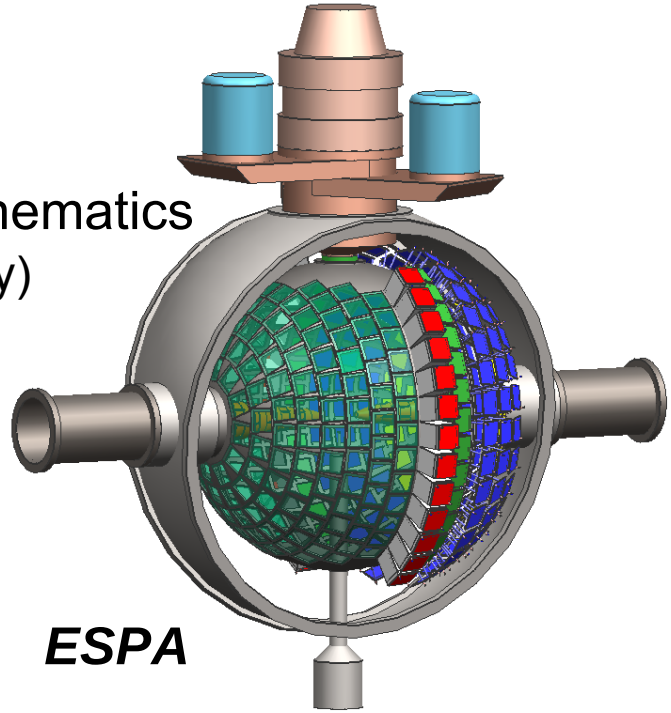
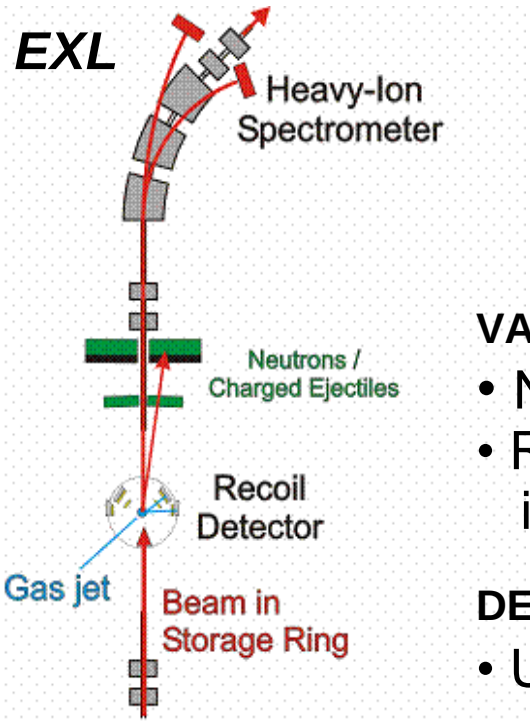
EXL Project at FAIR

EXPERIMENT:

- Reactions with radioactive beams in inverse kinematics
- Recoil detector **ESPA** (**E**XL's **S**ilicon **P**article **A**rray)
- Hundreds of DSSDs planned
- Placement in NESR environment





VACUUM REQUIREMENT:

- NESR vacuum better than 10^{-10} mbar
- Reasonable pumping-baking times after ESPA installation in NESR

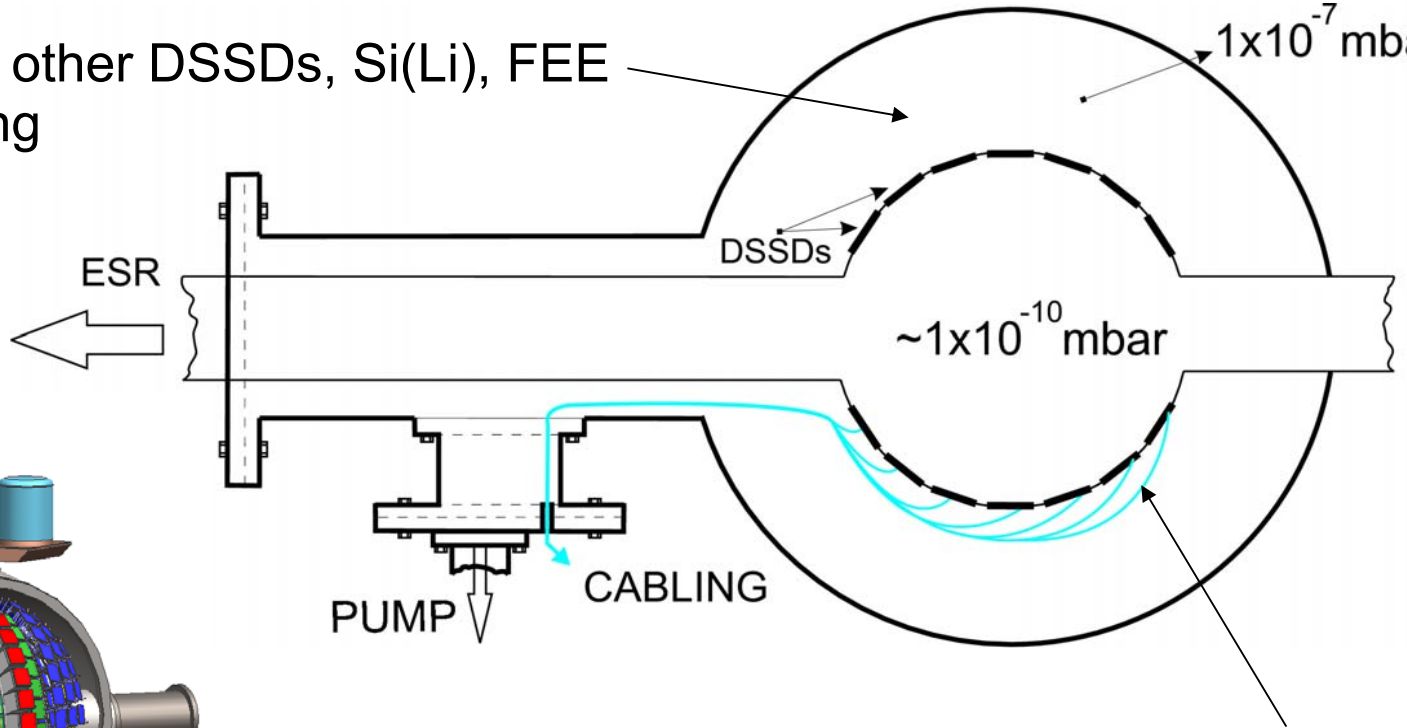
DEVELOPMENT:

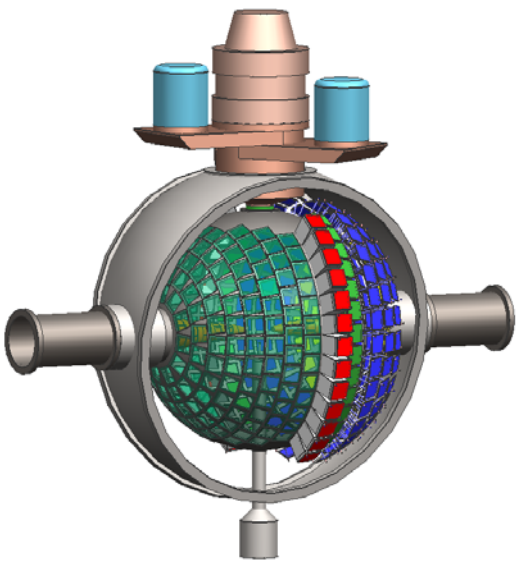
- UHVacuum barrier prototype using DSSDs

Using DSSDs as High-Vacuum Barrier

- Differential pumping proposed to separate NESR vacuum from EXL instrumentation (cabling, FEE, other detectors)

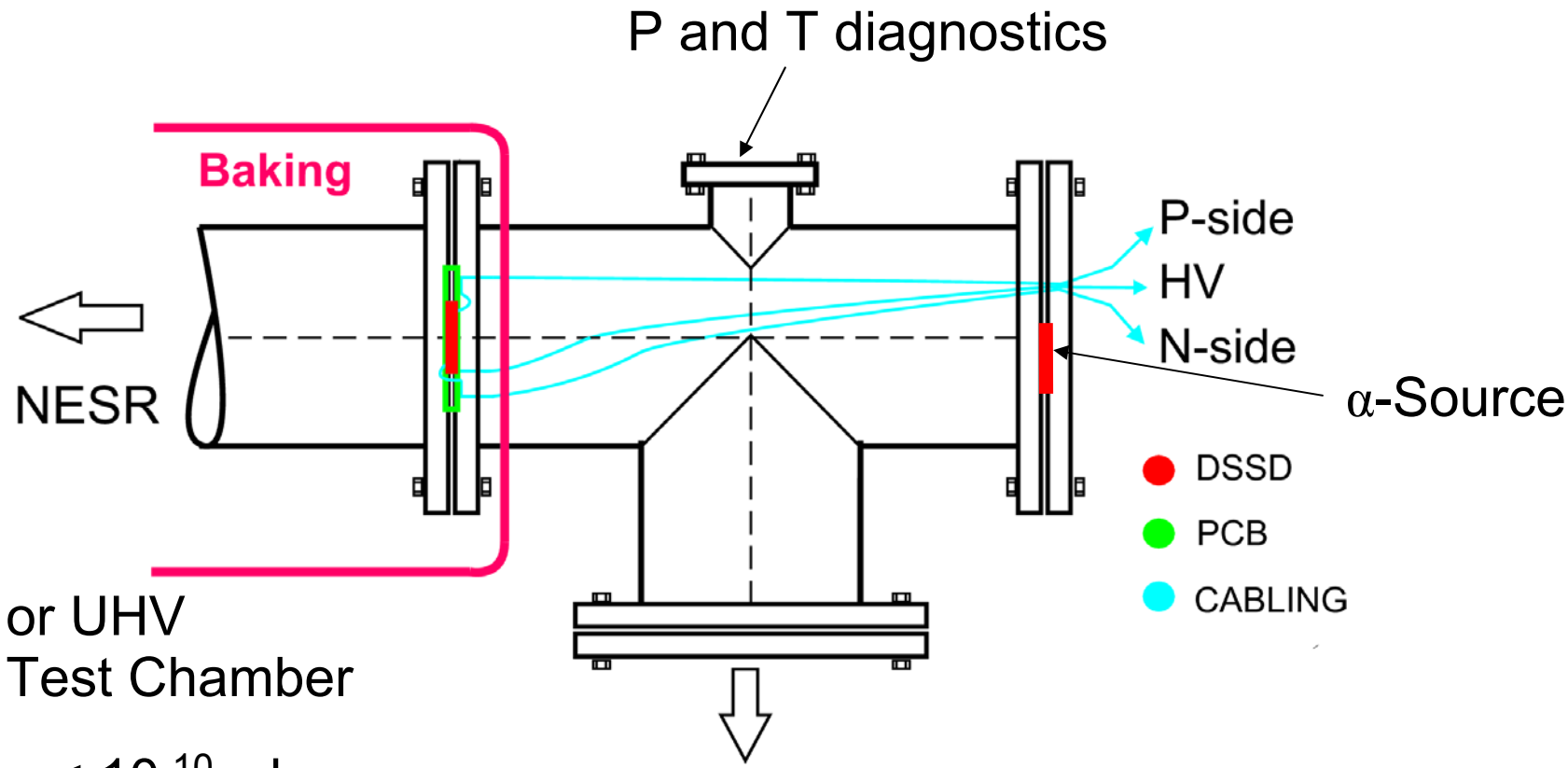
Space for other DSSDs, Si(Li), FEE and cabling





Inner shell of DSSDs on support frame forms (bakeable) vacuum barrier

Vacuum-Barrier Demonstrator



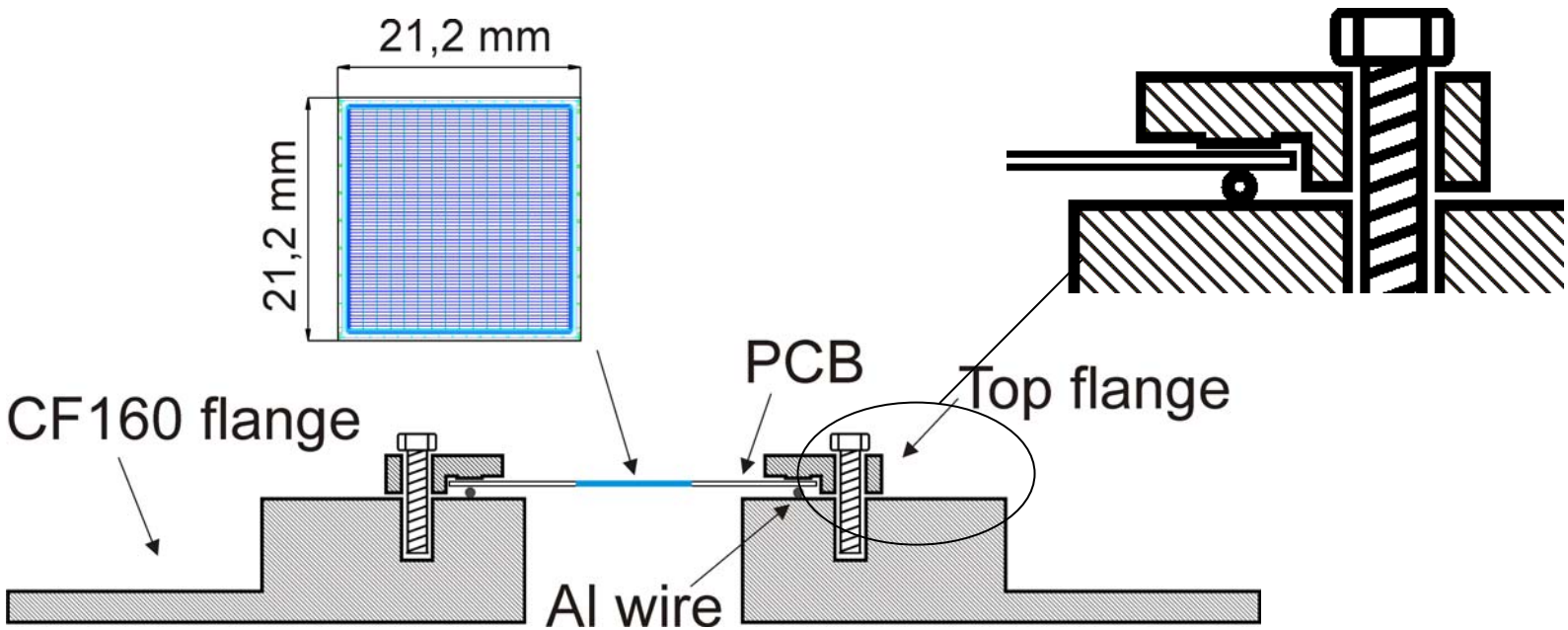
Requirements and Separation Principle

- PCB with one “clean” side – no connectors, soldering etc.
  - ♦ Connections from one side of DSSD must be driven on the other side

Bakeability up to at least 200°C

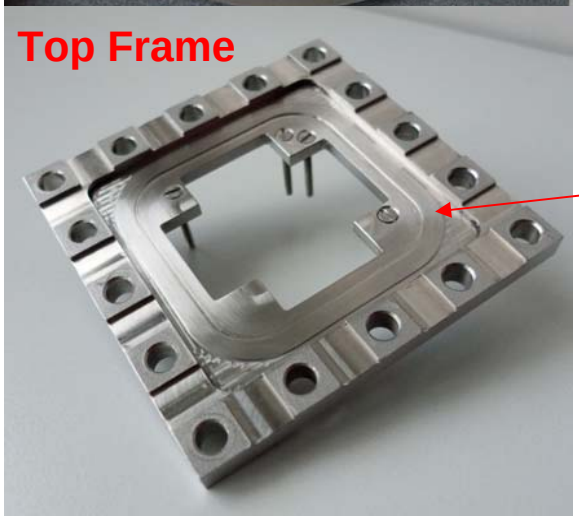
- ♦ Restricted choice of material
- ♦ Matched thermal expansion coefficients

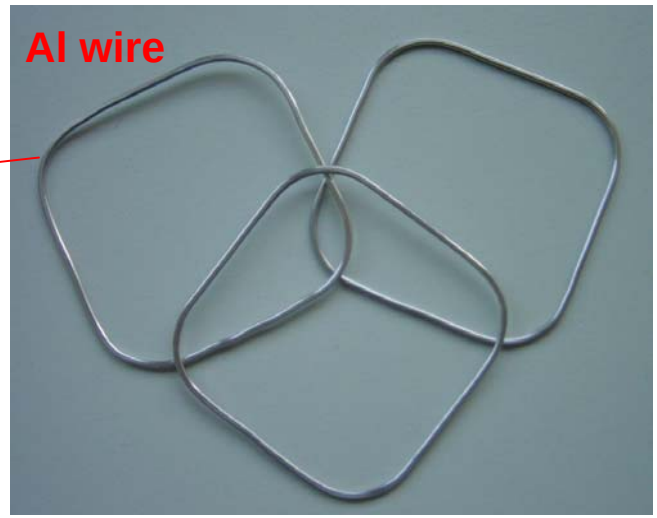
- PCB should be easily replaceable from the frame



Mechanical Construction

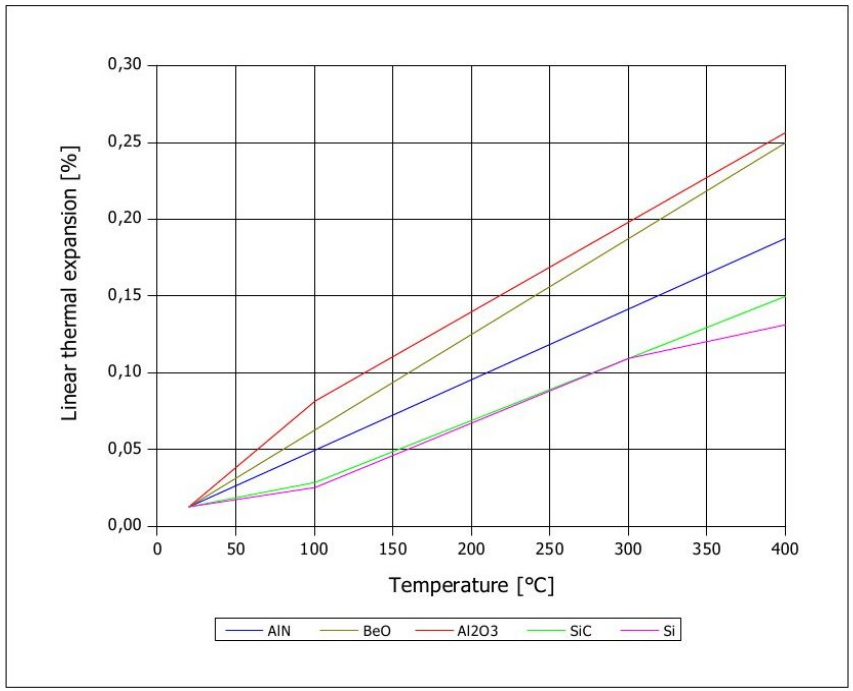
- Aluminium wire frame used as a vacuum seal
  - Welded wire
- Base frame machined from CF160 flange
  - Houses Al wire on top of which PCB is placed
  - Has α-source holder
- Top frame from stainless steal
  - Has groove that presses on PCB
  - Has mounts for connectors



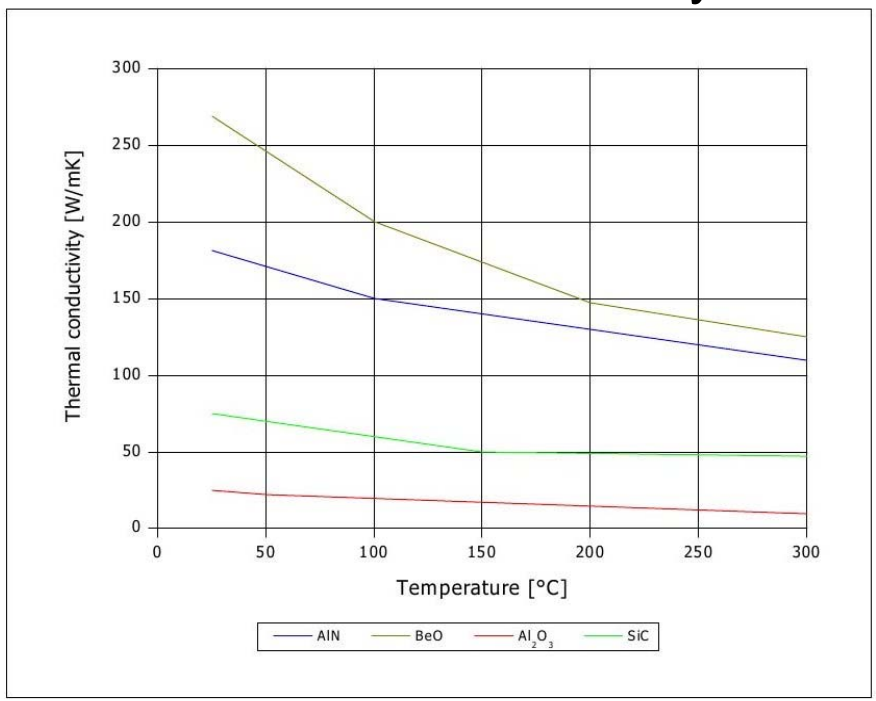


PCB Material Properties

Thermal expansion



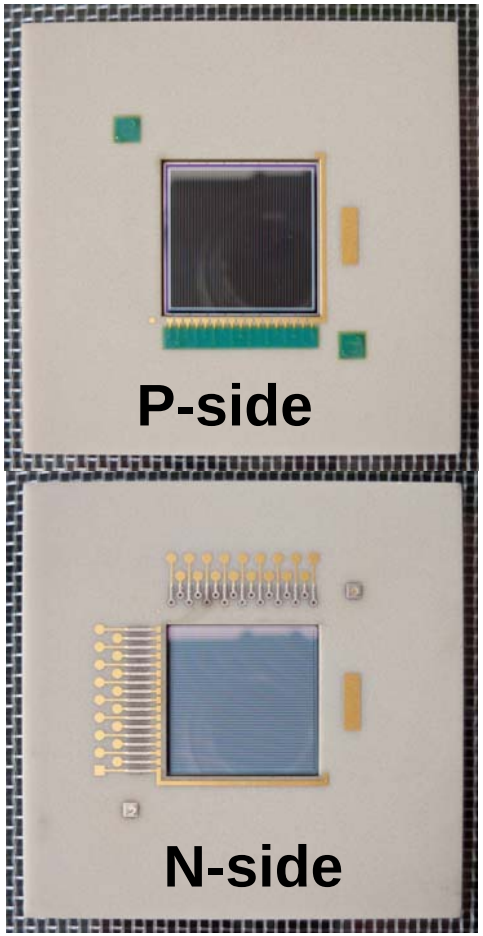
Thermal conductivity



IMPORTANT BAKING PARAMETERS:

- Thermal expansion of AlN fits best to Silicon (≈ 0.03% @ 200ºC)
- AlN has high thermal conductivity (170 – 200) W/mK – Silicon 160 W/mK

AlN Ceramic PCB and Connectors



PCB designed to have “through board” contacts
- Laser drilled holes for routing P-side contacts to N-side
- Holes hermetically filled and covered with glass

• Manufactured from Aluminum Nitride (AlN)
- Ultra-low outgassing + bakeable to > 200°C
- Expansion coefficient close to Silicon
- High thermal conductivity

• DSSD glued with EPO-TEK®H77S low-outgassing glue

LUST HYBRID-TECHNIK

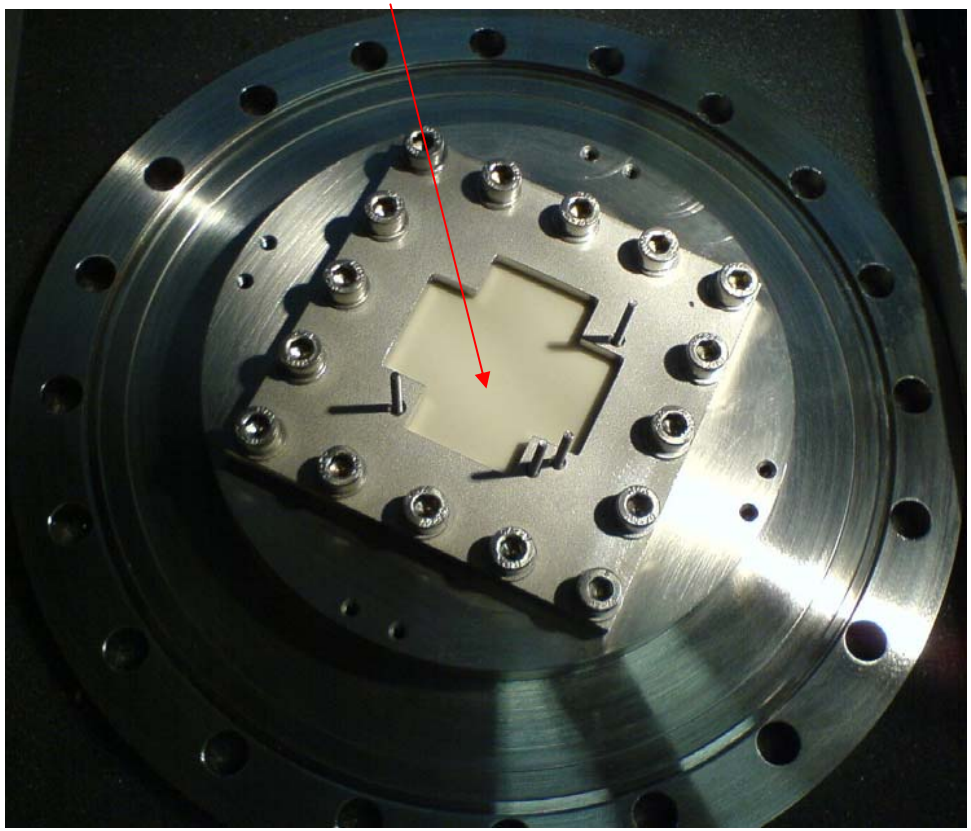
IDI INTERCONNECT DEVICES, INC.

Connectors machined from PEEK®
• Spring pins of 0.52 mm diameter used
• Kapton coated bakeable cables used

Blind PCB Vacuum Test

- Test of the Al wire tightness with the blind (no detector) PCB
  - UHV side → **5 * 10^{-10} mbar** vs. Low-vacuum side → **1 * 10^{-1} mbar**

Mounted blind PCB



CONDITIONS:

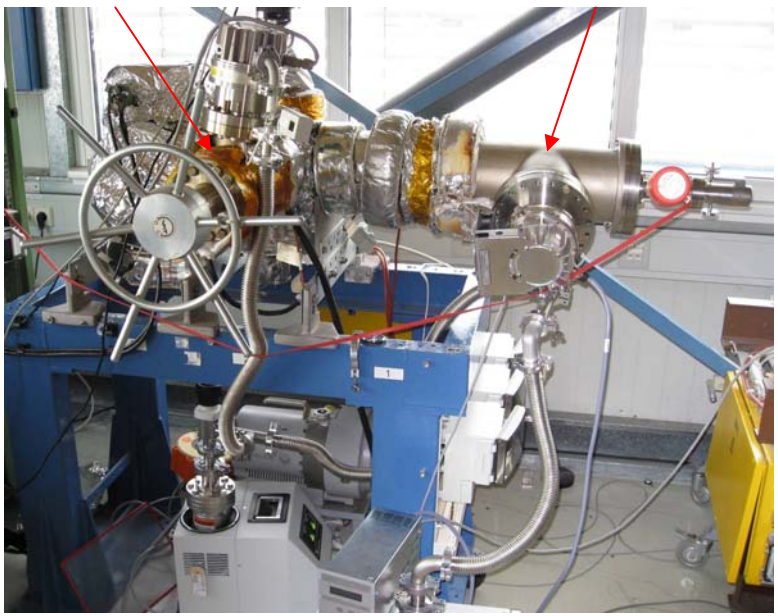
- Low-vacuum side
  - Oil-free prepump
- High-vacuum side
  - Turbo pump
  - Baking for 3 days
  - Up to 200°C

Differential Vacuum Test

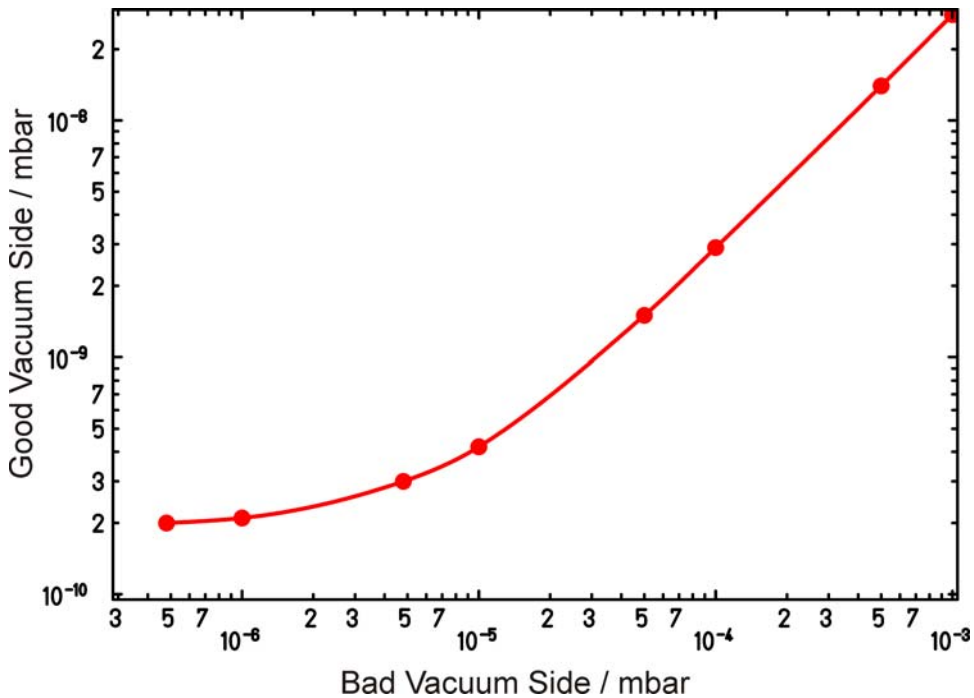
- Differential vacuum test using **real DSSD** as a vacuum barrier
  - 4 orders of magnitude difference between low and UH vacuum in wide pressure region
- Vacuum of **$2 * 10^{-10}$ mbar** reached – pumping limit of the station

UHV part

Low vacuum part

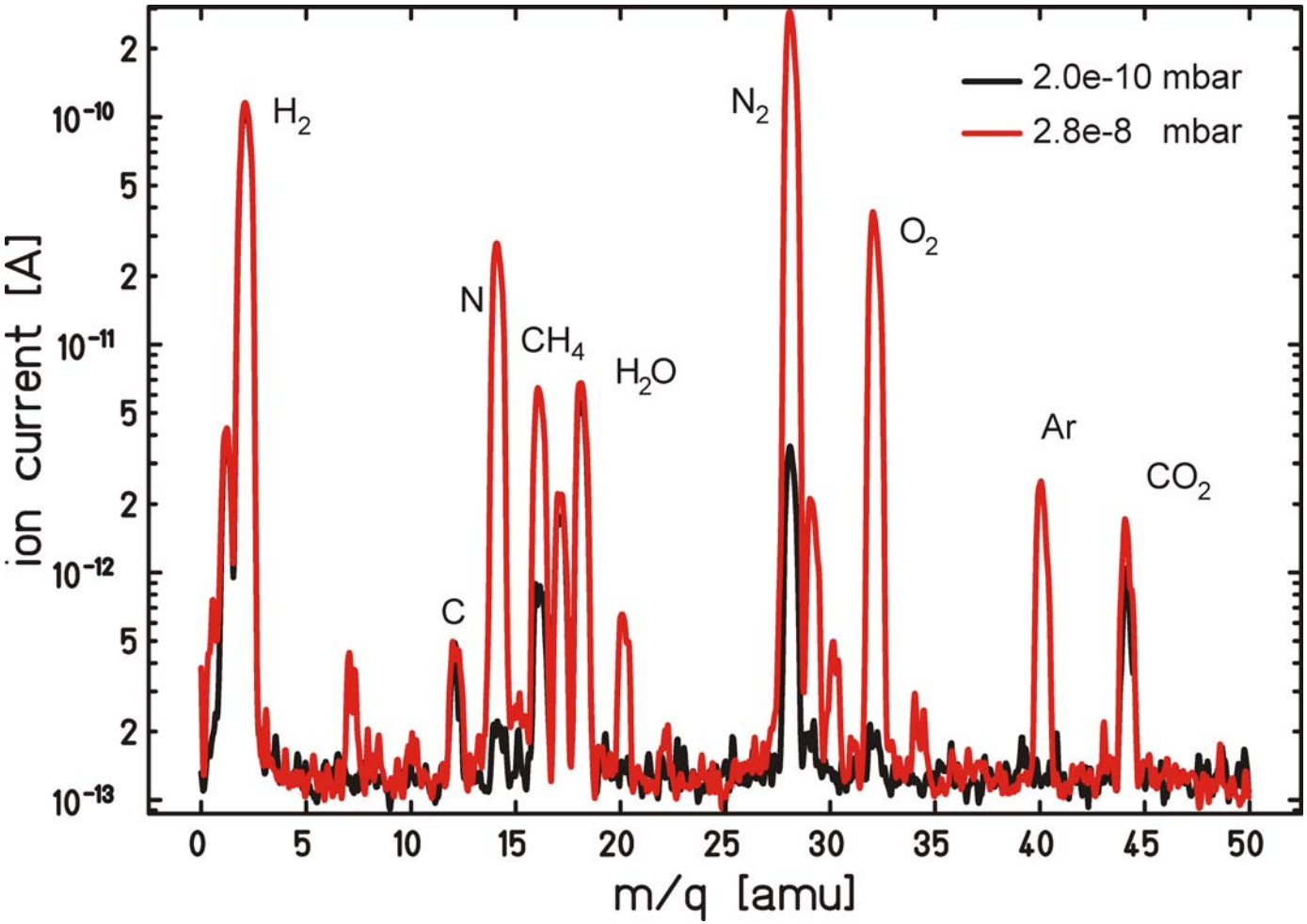


Vacuum separation

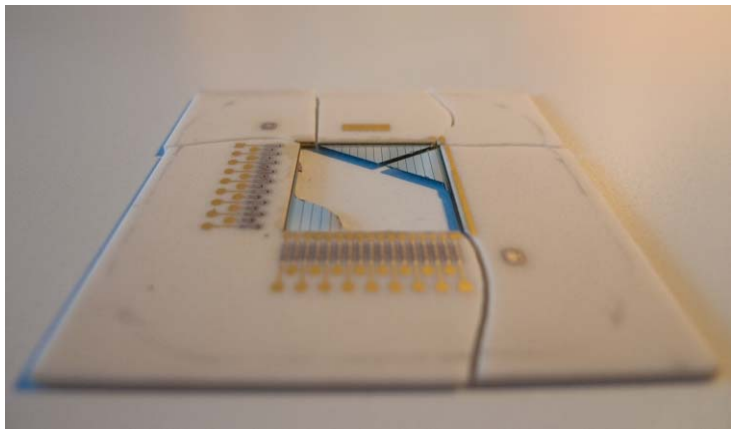


Outgassing Results

Low rate of outgassing and rest-gas spectra clear of contaminants for glued DSSD



Current Status



...from break to breakthrough?...

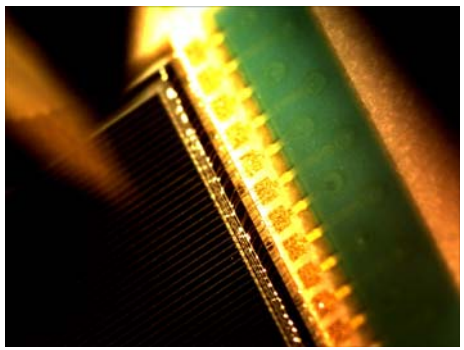
(Hair-line crack occurred during baking)

- ✓ DSSD detector on ceramic PCB constructed for vacuum test
- ✓ 9 orders of magnitudes of vacuum difference held by Al wire seal
- ✓ Vacuum separation by 4 orders of magnitudes in pressure reached using DSSD as vacuum window
- ✓ No vacuum deterioration by outgassing components

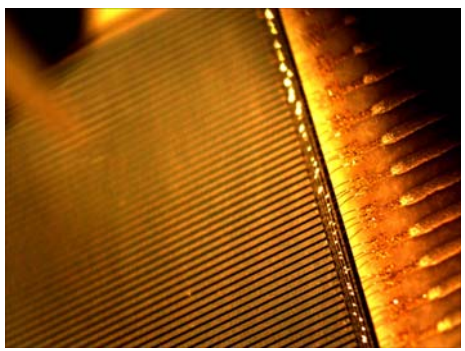
Next Steps

- Improve mechanical forces and reliability (double Alu-ring structure)
- Test a bonded DSSD (16 x 16 channels)

P-side

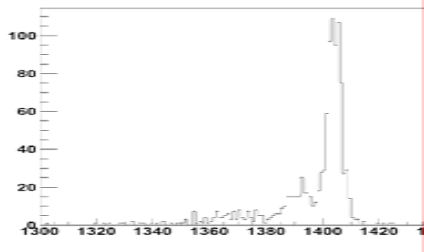


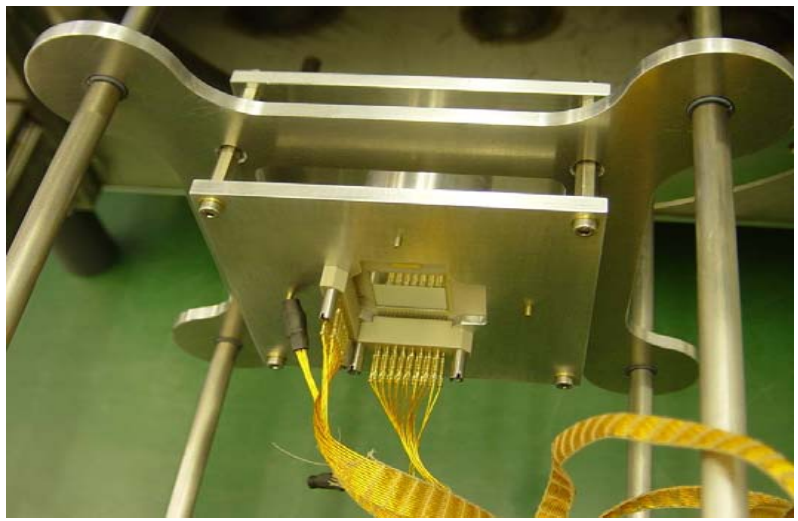
N-side



Performance Test

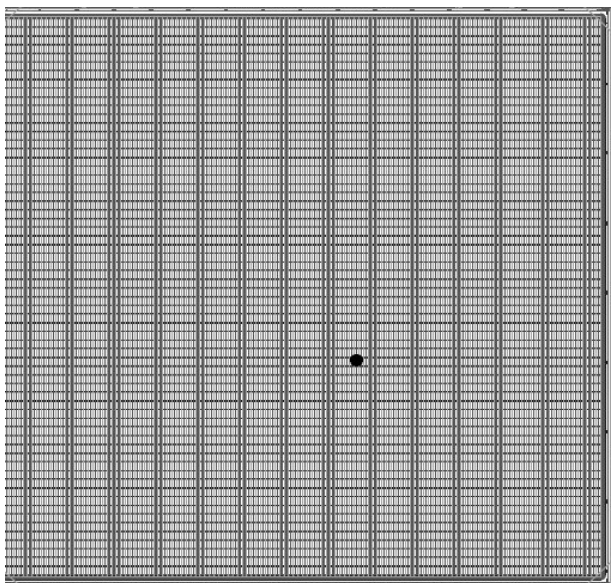
α - spectrum





Outlook

- Optimizing the design to maximize active area
- Mechanical solutions other than demonstrator setup
- New ceramic PCB design for 6.5 x 6.5 cm^2 DSSDs (128 x 64 strips)



Silicon: 7 - 20 kOhm×cm

Diode structure: p+ (strips) – i - n+ (strips), orthogonal, n+ - strip insulation by p+ implant

Diode area: 65 x 65 mm^2

Diode topology: Strips on p+ side: 128
Strips on n+ side: 64

Diode thickness: 300 µm

Operational reverse voltage limit: > 100 V

Thank You