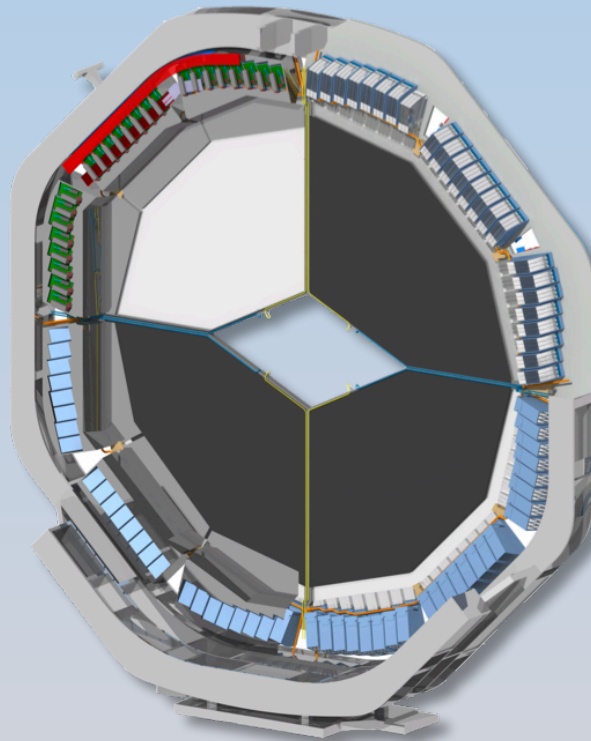


Endcap Disc DIRC-Mechanics Status

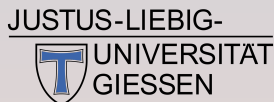


PANDA CM 19/3 – MEC Session - 2019/11/08

Ilknur Köseoğlu Sarı, Simon Bodenschatz, Lisa Brück, Michael Düren, Avetik Hayrapetyan, Jan Hofmann,
Sophie Kegel, Jhonatan Pereira de Lira, Mustafa Schmidt, Marc Strickert



Bundesministerium
für Bildung
und Forschung



HGS-HIRe for FAIR
Helmholtz Graduate School for Hadron and Ion Research

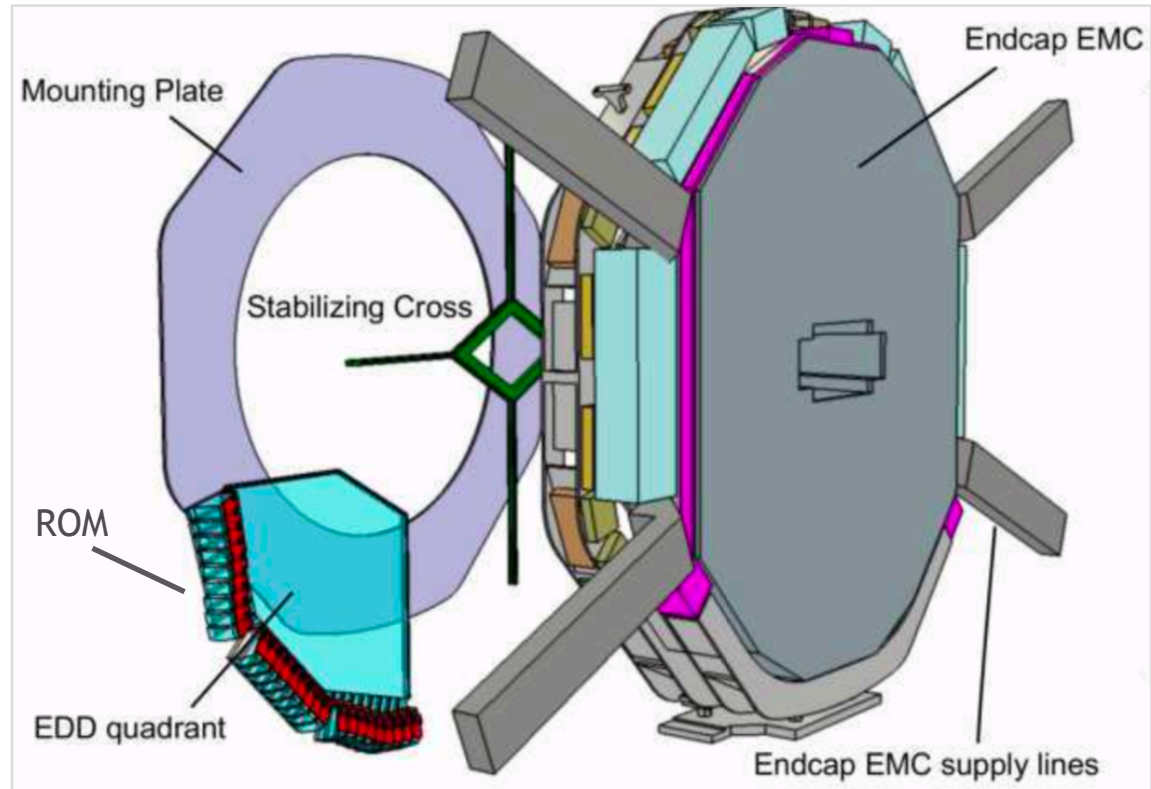
GSI
GSI Helmholtzzentrum für Schwerionenforschung GmbH

HIC for FAIR
Helmholtz International Center

panda

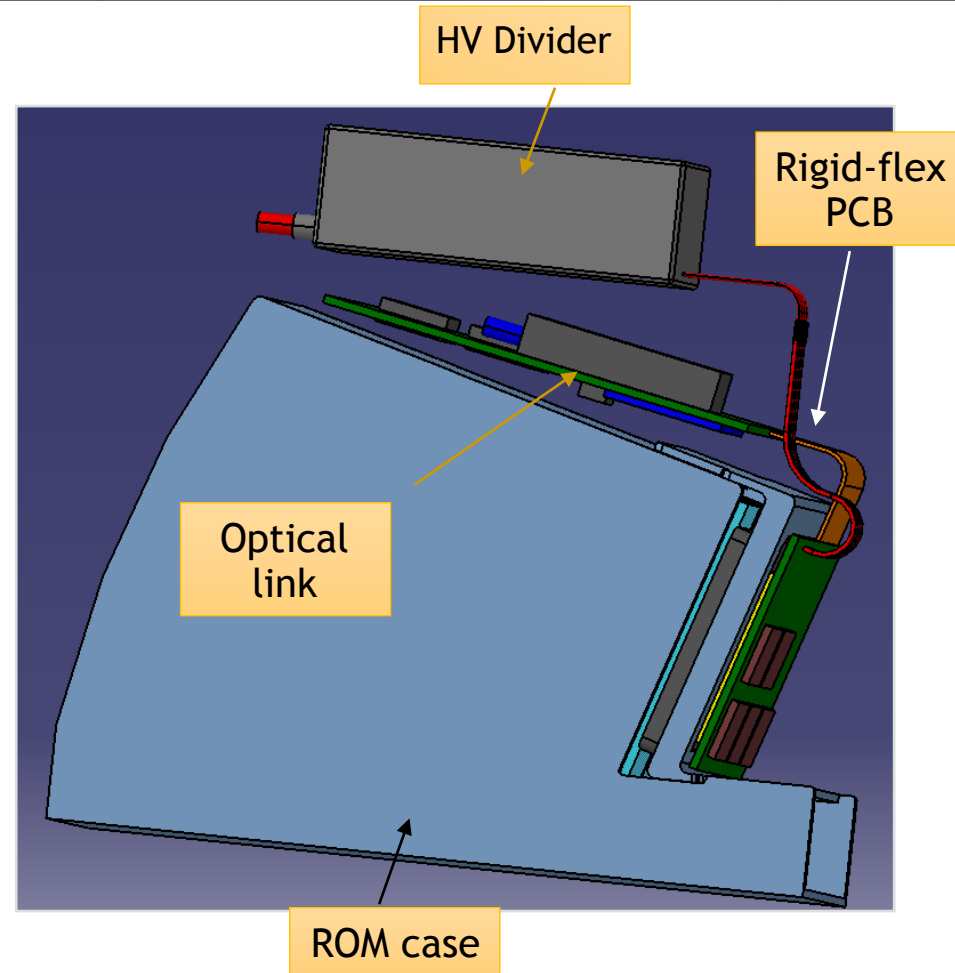
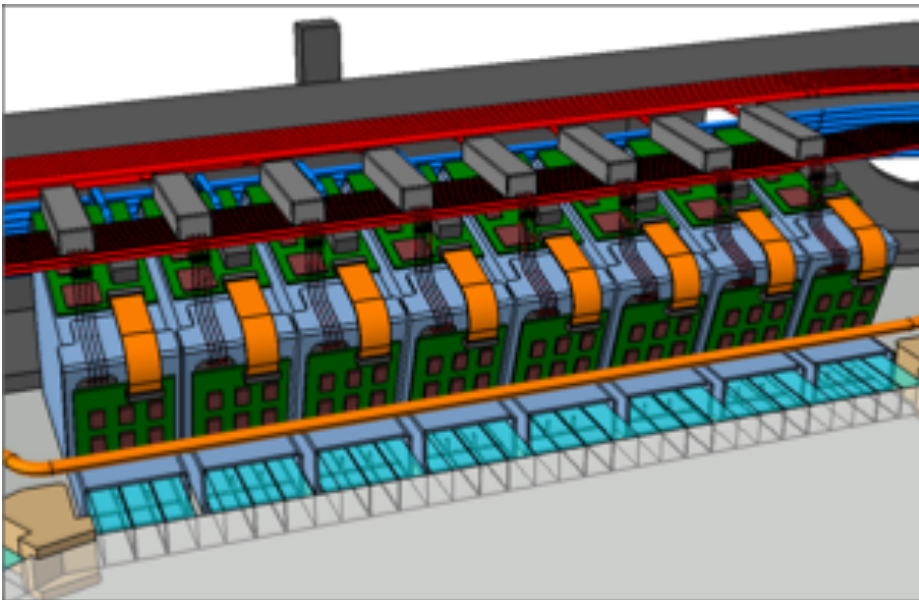
EDD elements

- Quadrants
 - Light tight
 - Gas tight
- Mounting Plate, MP
- Stabilizing Cross
- Readout Modules, ROM
 - Light tight
 - Gas tight
 - 96 ROMs in total
 - 24 ROMs/Quadrant



Readout module (ROM)

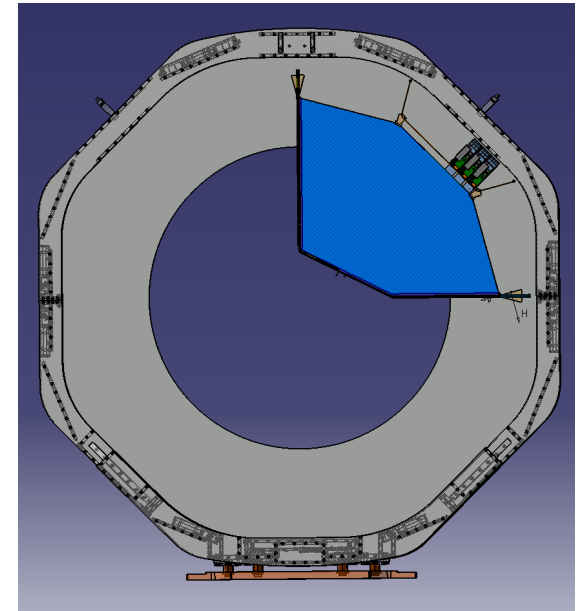
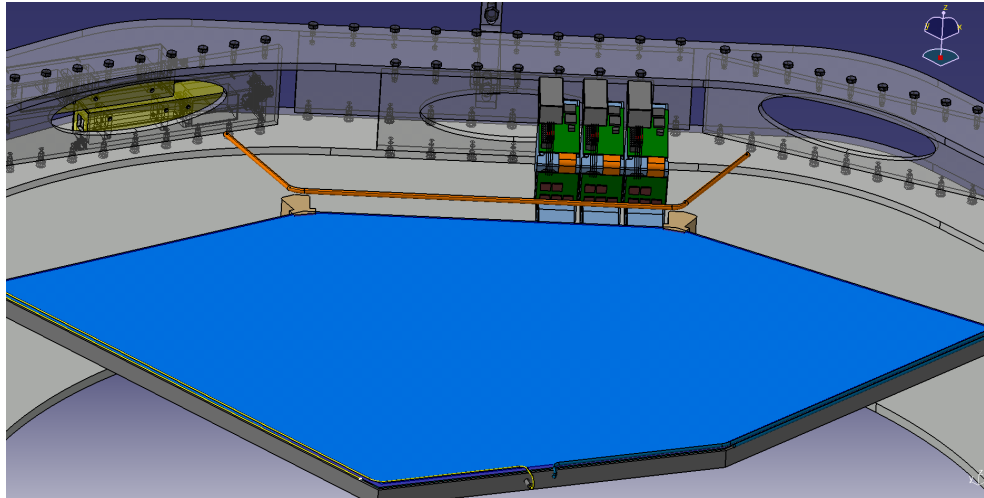
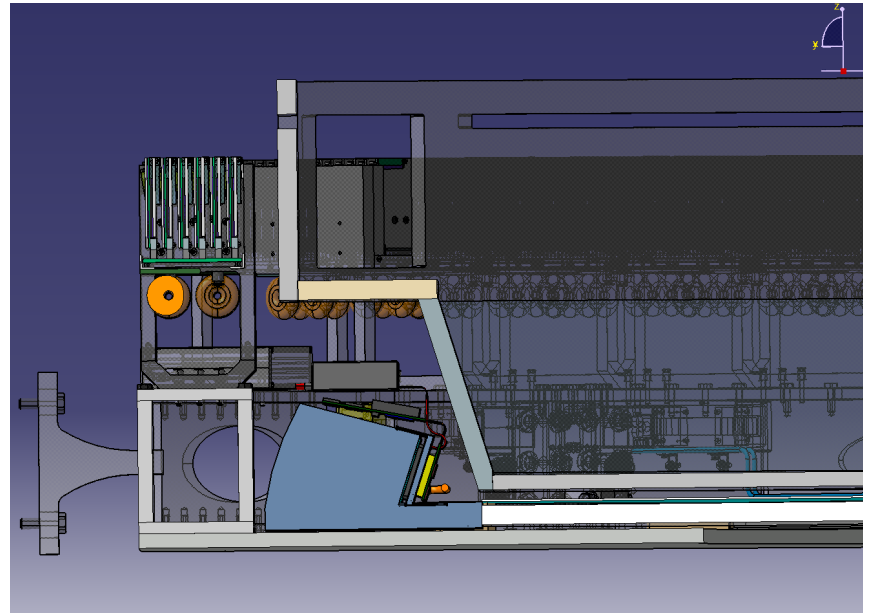
- 3 Focusing elements
- 3 Bars
- ROM case
- Rigid-flex PCB
- HV divider



Alignment of 8 ROMs

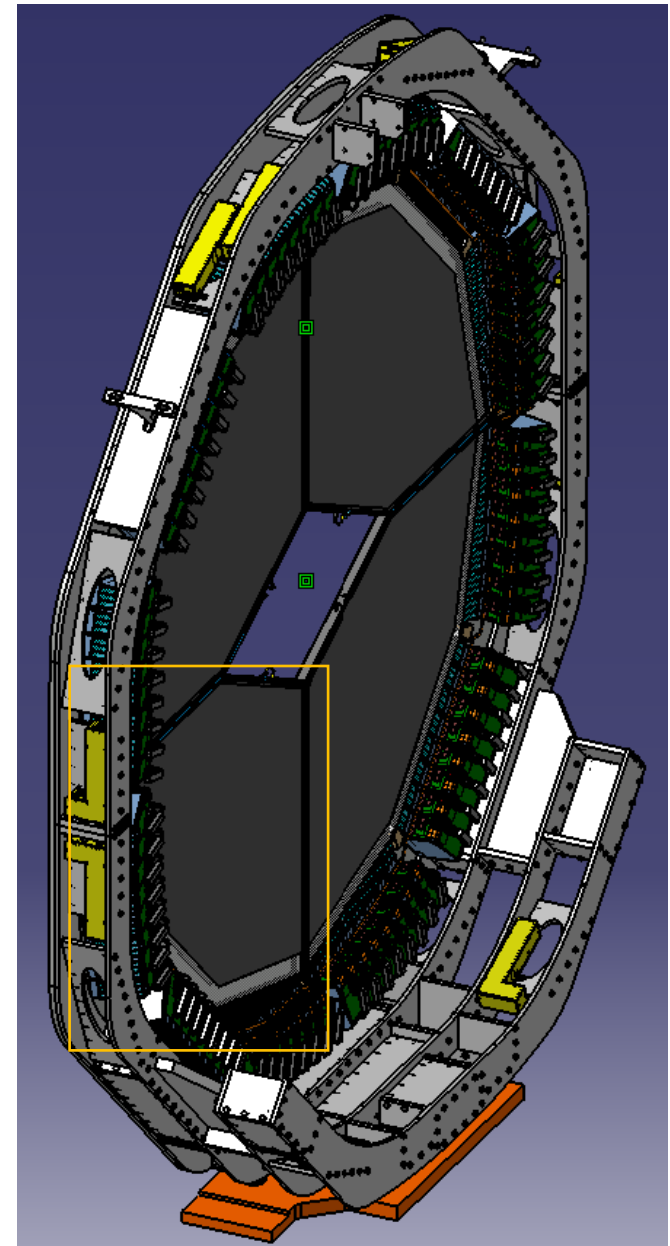
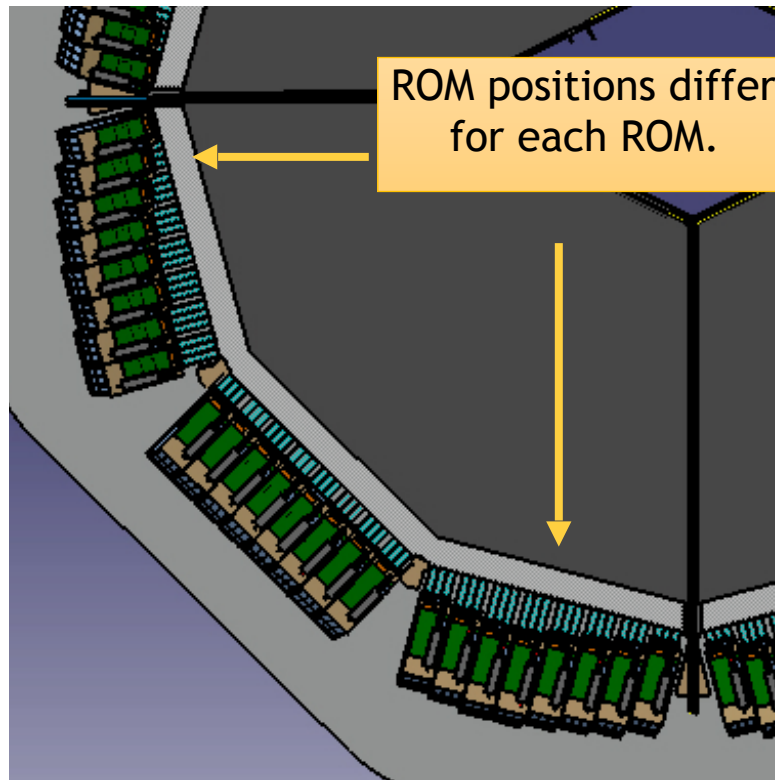
Design for Prototype & Phase 1

- ➔ We need financial support for a better setup during Phase-1.
- Our desire is to have one full quadrant for Phase-1
 - 24 ROMs, 24 MCP-PMTs
 - 24 FEE-board
- We can install our prototype for phase 1 if we have a financial support otherwise we have only 3 ROMs.



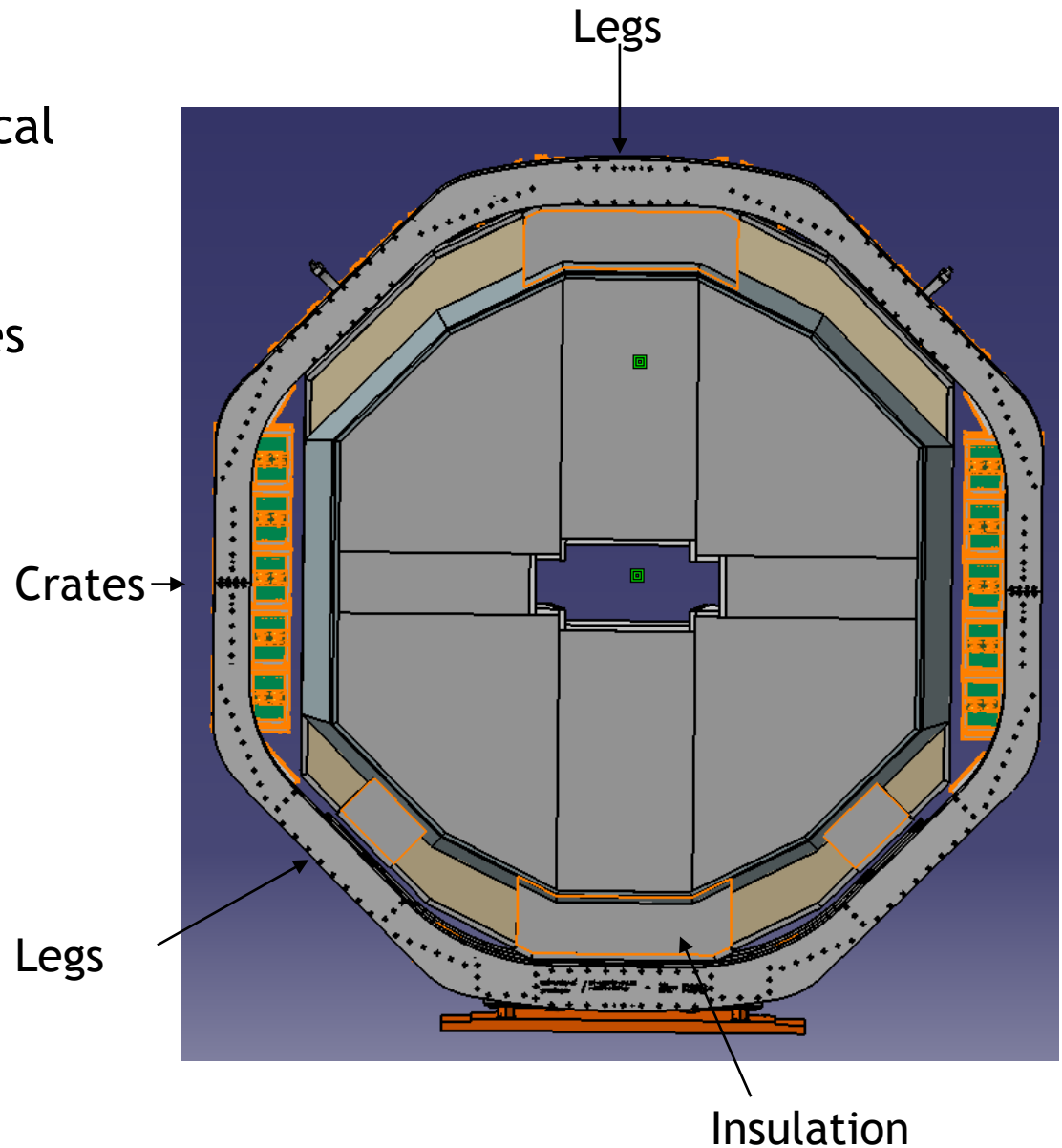
Design for Phase 2, Mounting plate & Support frame

- 96 ROMs align around the EDD radiator
- Because of the EMC insulation, ROM position differs for each region.



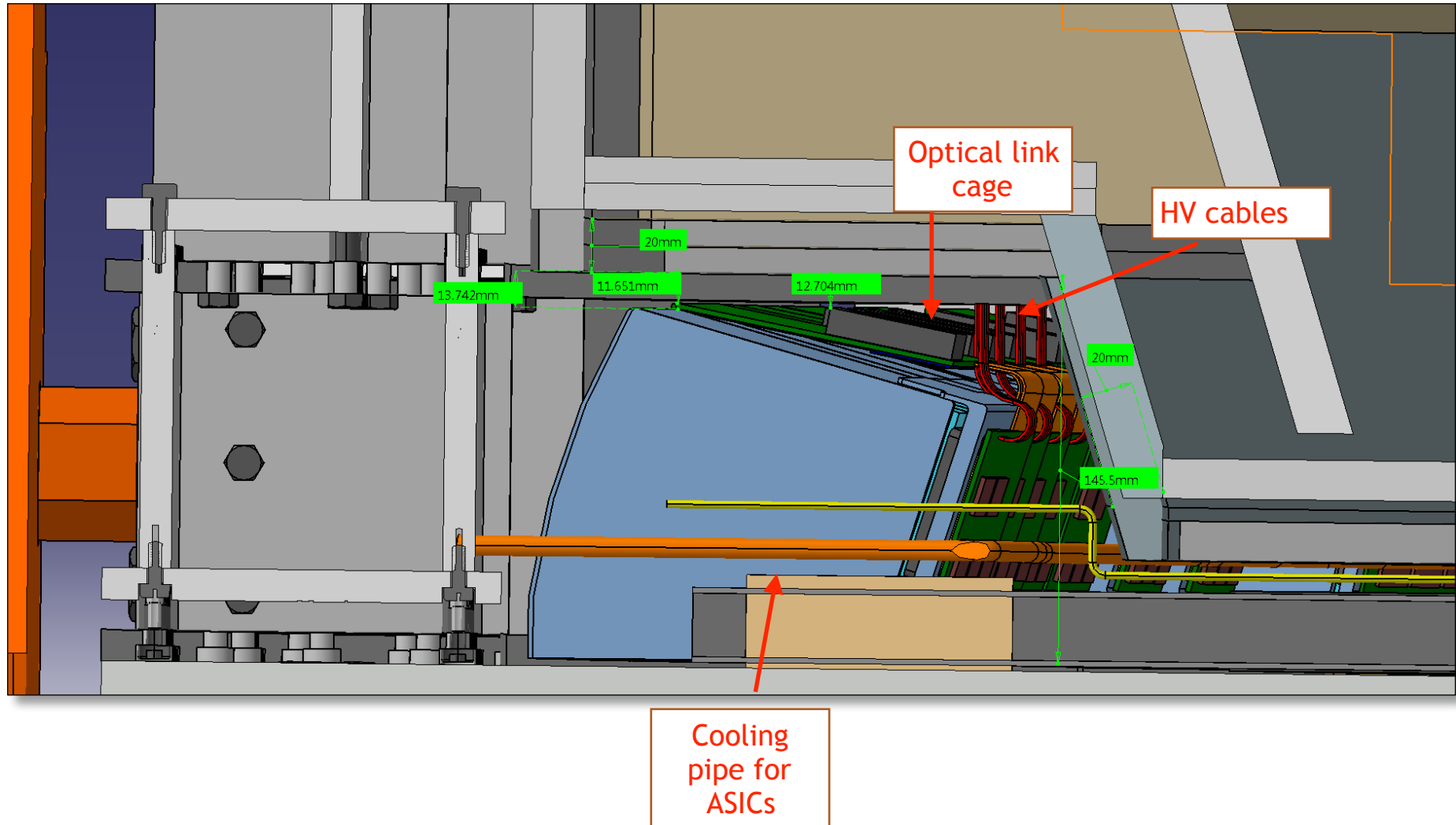
Limited regions

- Lightened areas are critical regions
- Spatial constraint changes depending on phi-angle.
 - Crate region at two sides
 - Leg region
 - Insulation at bottom



Limited leg region

Minimum distance between EDD and EMC insulation ~ 7mm

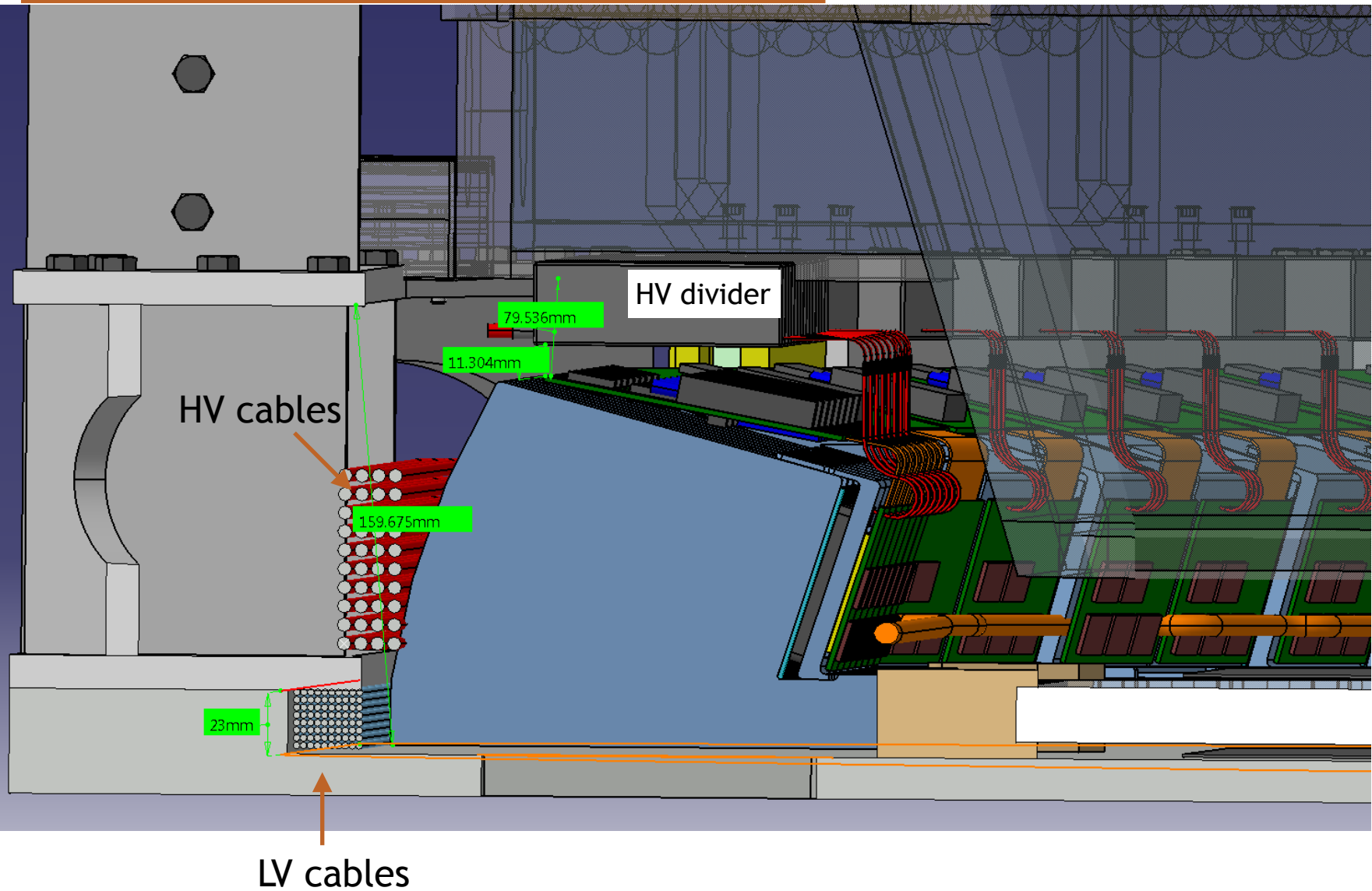


Problems

- There are limits both z-direction and radial direction.
- No space for cable alignment
 - HV cables, LV cables, Optical link
- Cooling system for FPGA has not been implemented yet!
- No space for HV divider
- Not enough space for FEE!

Proposed solution from CM 19/2

◆ Moving the EDD 23 mm through GEM station



Problems

- There are limits both z-direction and radial direction.
- No space for cable alignment
 - HV cables, LV cables, Optical link
- Cooling system for FPGA has not been implemented yet!
- No space for HV divider
- Not enough space for FEE!

Proposed Solutions from previous CM

1. Reducing the number of ROMs in each quadrant, **not preferable. (Efficiency loss!)**
2. Moving EDD through the upstream direction. EDD is in-between GEM detectors and forward EMC. -> GEM group tried to find a solution but as a result this is **not possible** either.
3. EMC group has already produced insulation part. From neighbors, we could not get extra space!



Not enough space for the EDD!





Thanks for your attention!