

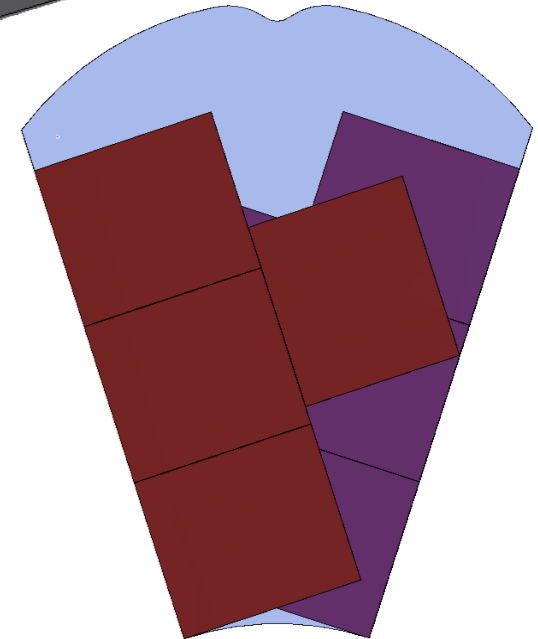
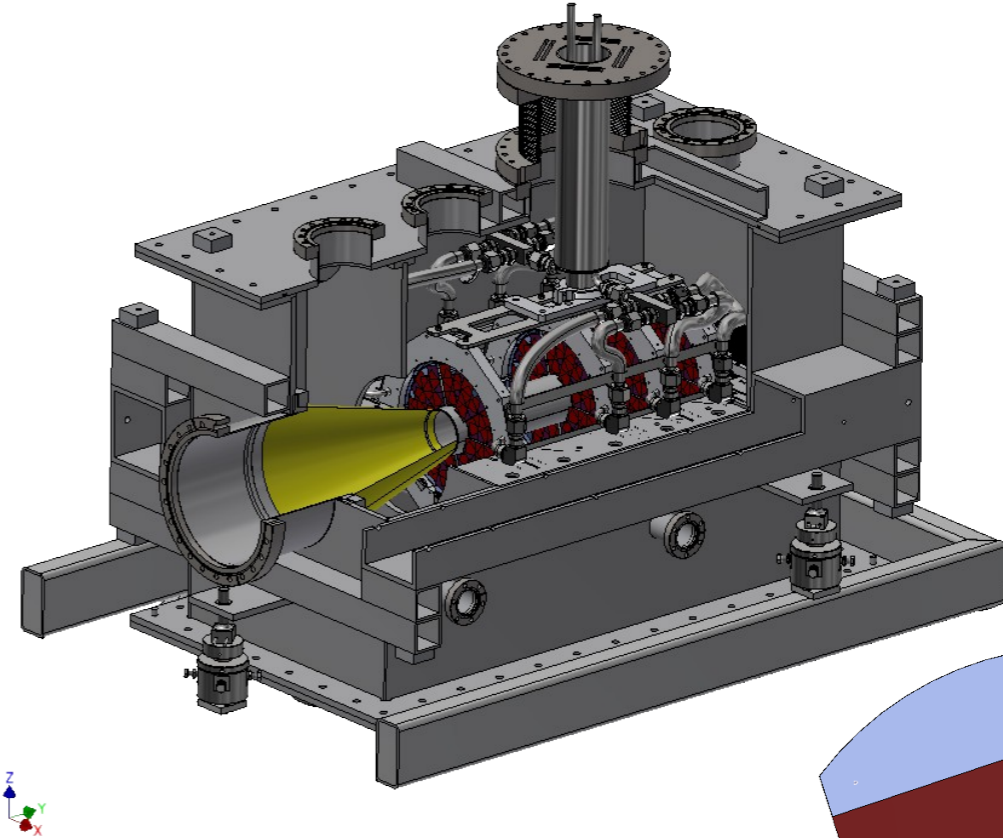
# **MuPix8 Status and Reworking of DAQ**

**– PANDA Collaboration Meeting 2019/3 –  
Luminosity Detector Session**

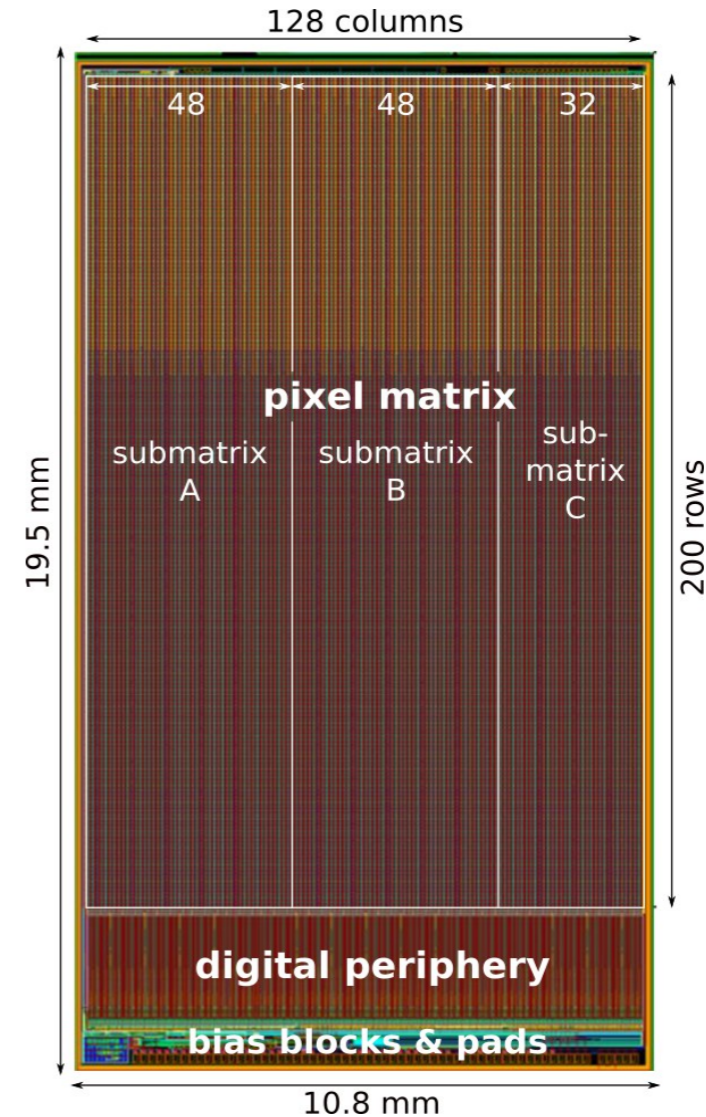
René Hagdorn  
Ruhr-Universität Bochum

Darmstadt, November 5, 2019

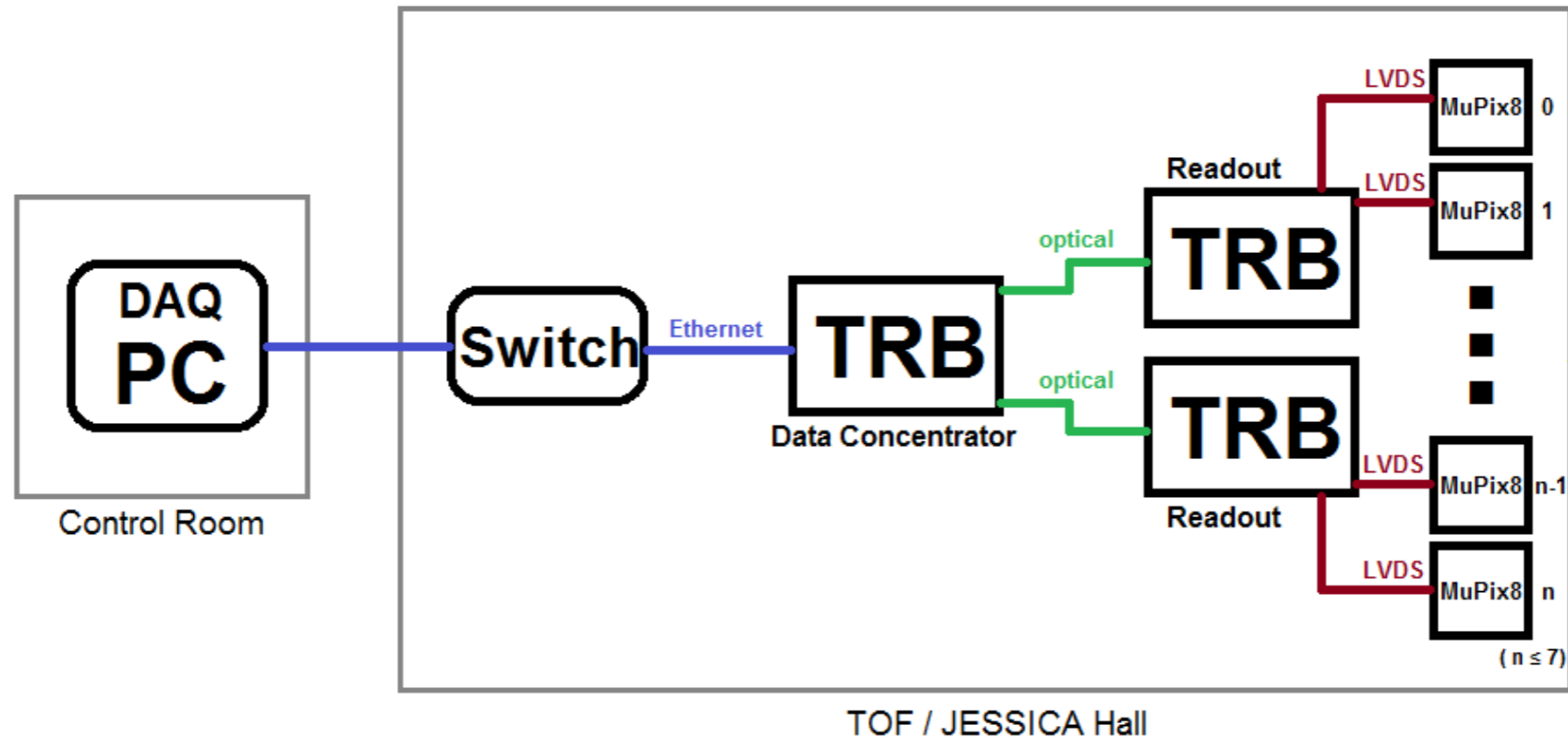
- 11 m behind IP
- Measure tracks of elastically scattered anti-protons
- Anti-protons enter detector vacuum through transition cone
- 4 detector layers with HV-MAPS on both sides
- 10 sensor modules per layer
- Aluminum holding structure with embedded steel pipe for cooling (coolant:  $-20^{\circ}\text{C}$  ethanol)
- Total number of sensors: 320
- Active area of one sensor:  $2 \times 2 \text{ cm}^2$
- Pixel size:  $80 \times 80 \mu\text{m}^2$



- Originally developed for Mu3e
- Physical size:  $10.8 \times 19.5 \text{ mm}^2$
- Active area:  $\sim 10.2 \times 16.2 \text{ mm}^2$
- Matrix:  $128 \times 200$  Pixels, three Submatrices  
MatA: source follower  
MatB/C: current mode
- Pixel:  $80 \times 81 \text{ }\mu\text{m}^2$
- Charge sensitive amplifier in each pixel
- Two comparators in each peripheral cell (timewalk compensation)
- 4 LVDS links (each submatrix + select/mux)
- Analog readout of Hitbus (ToT information) and amplifier output (for leftmost column only)

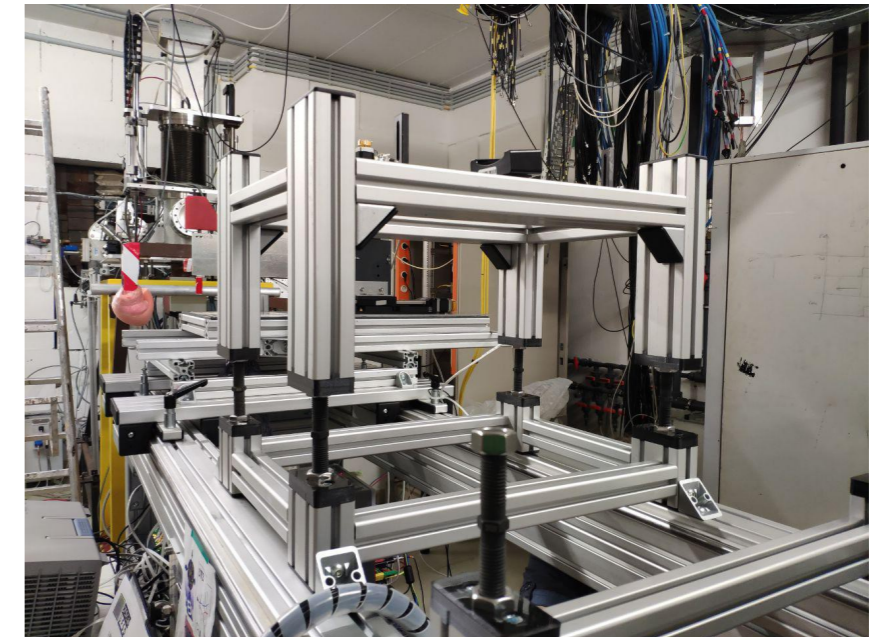
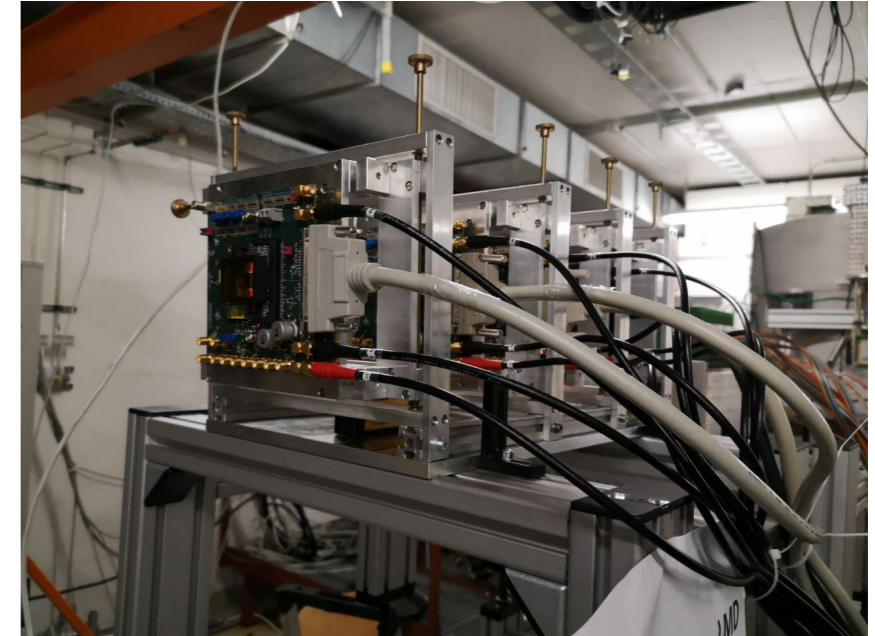
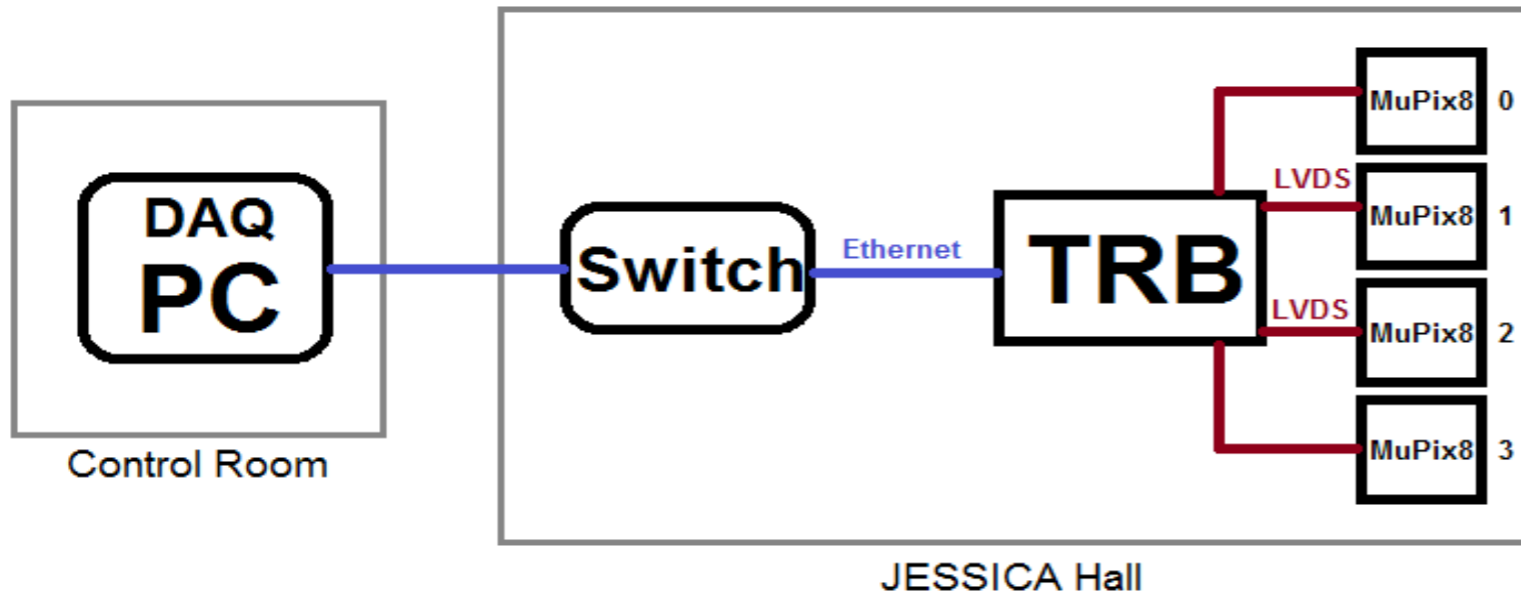


- Testbeam September 2019 – Idea: Use setup similar to final LMD readout scheme
  - Only one TRB as data concentrator / interface to DAQ PC
  - Use separate TRB(s) as readout unit(s)
  - Optical connection
  - Synchronize via SODAnet → **DID NOT WORK OUT FOR SEPTEMBER TESTBEAM**



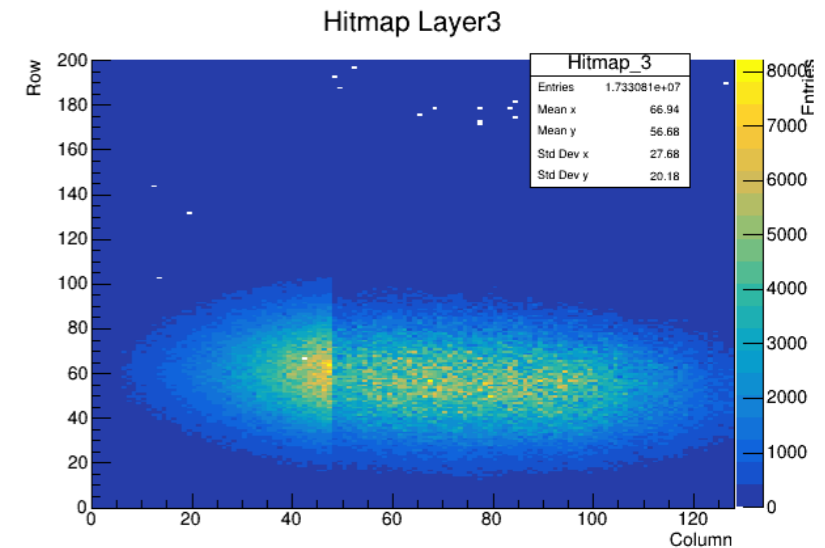
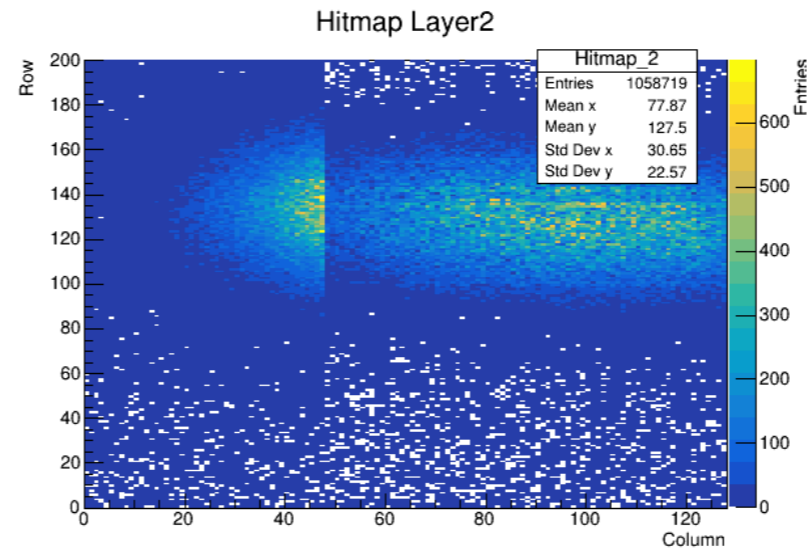
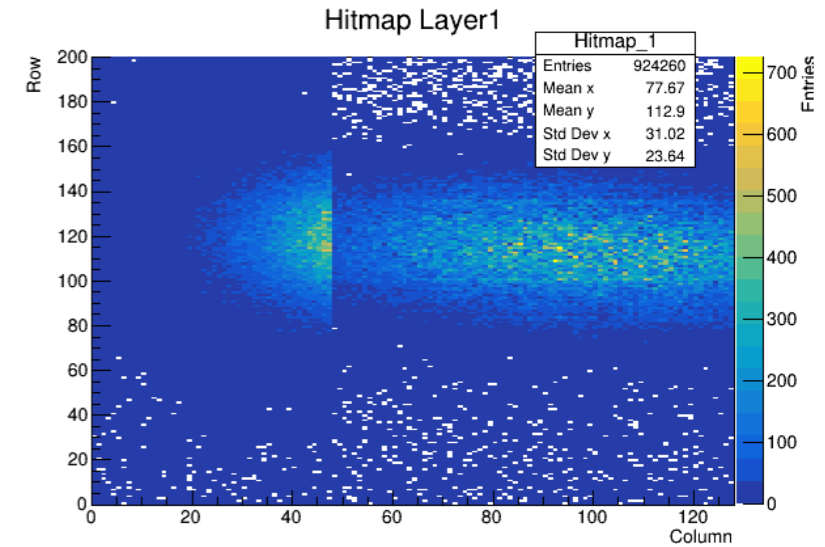
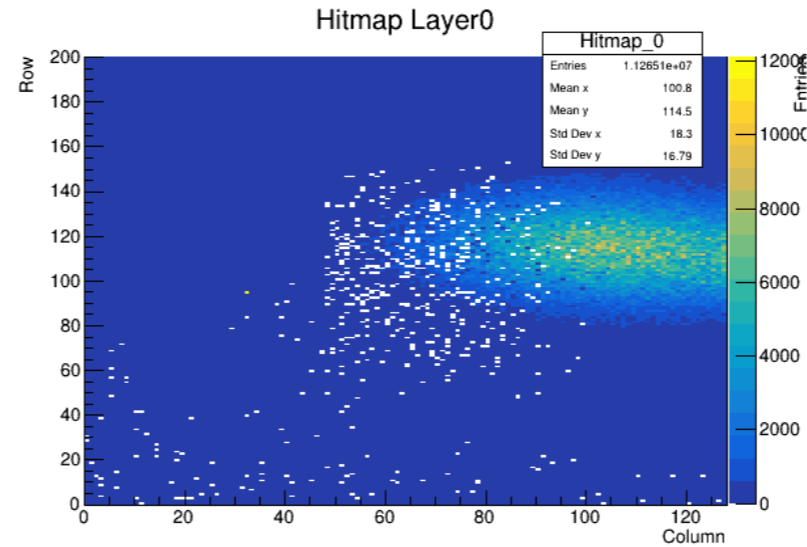
# Four-Layer MuPix8 Setup at COSY

- Testbeam in September 2019
- Four MuPix8 chips in beam (JESSICA hall)
- x-y-adjustable holding frames and positioning rail from HIM + height adjustable pedestal
- Goals: Readout of all submatrices (A,B,C) of four chips, test new control software based on EPICS for LV/HV and sensor configuration
- Old DAQ with only one TRBv3



- Hitmaps of first run (w/o MWPC)
- HV = 0 V, ThHigh = 600 mV for all layers
- Beam spot visible in all layers
- Sharp cut between Matrix A and B/C

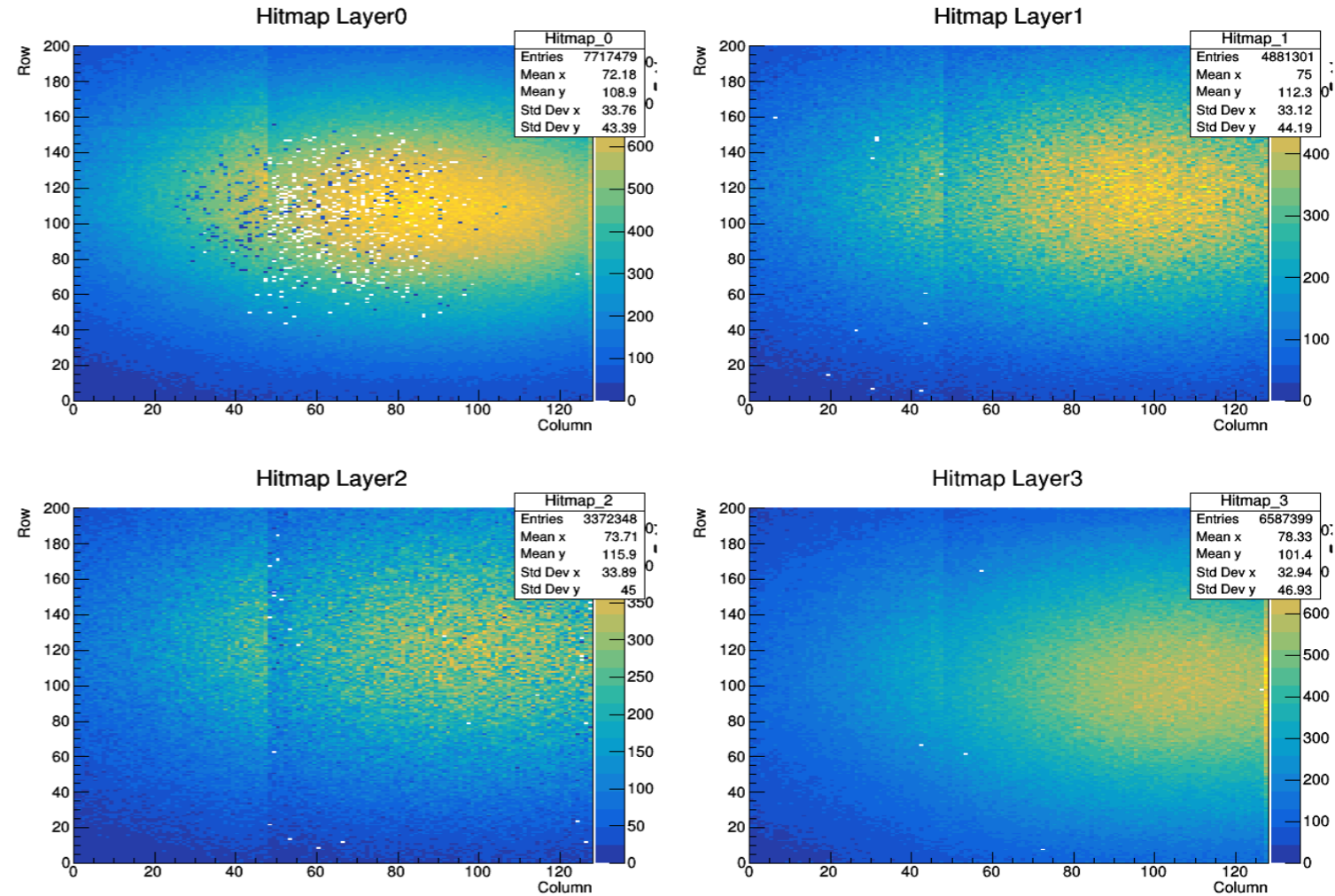
Beam parameters:  
 $p \lesssim 2.9 \text{ GeV}/c$   
 $\sim 10^6 \text{ protons} / \text{s}$



Hitmaps @ HV = 0 V and ThHigh = 600 mV

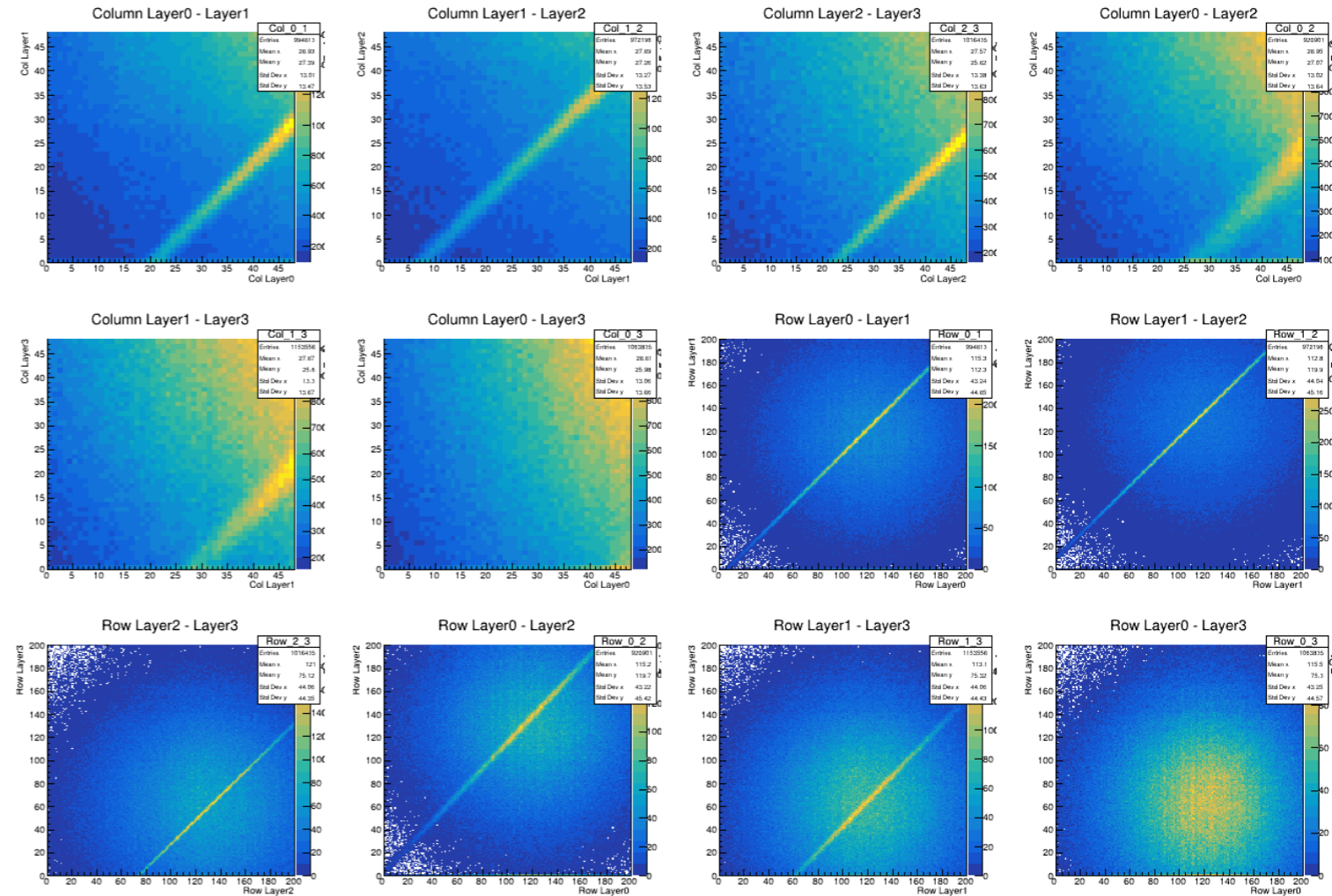
- Inserted MWPC into beam to get wider spread
- Only used matrix A for alignment

Hitmaps with MWPC in beam  
HV = 50 V and ThHigh = 600 mV



- Inserted MWPC into beam to get wider spread
- Only used matrix A for alignment

Column and Row Correlations for matrix A before alignment:  
DUT: HV = 50 V and ThHigh = 600 mV

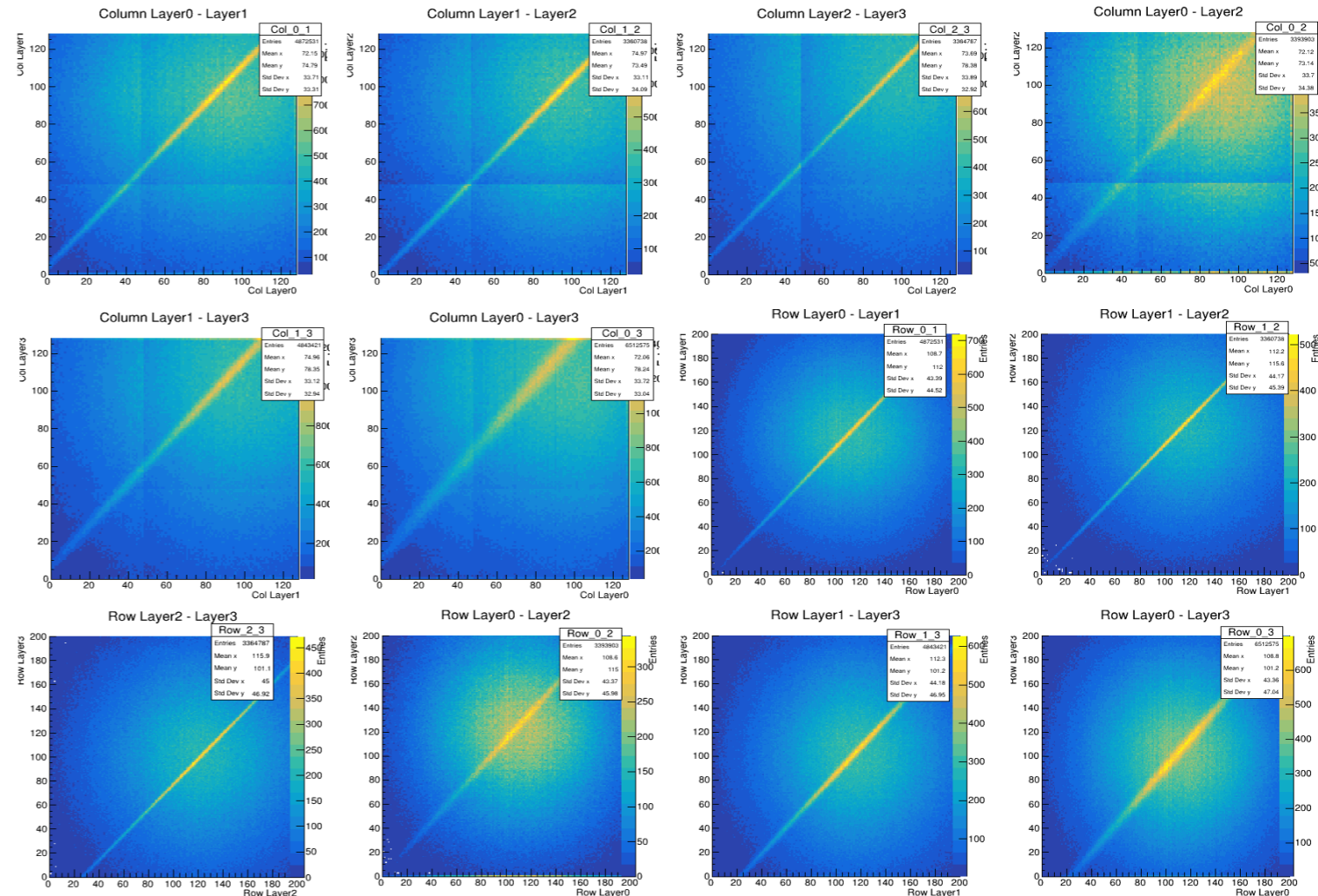




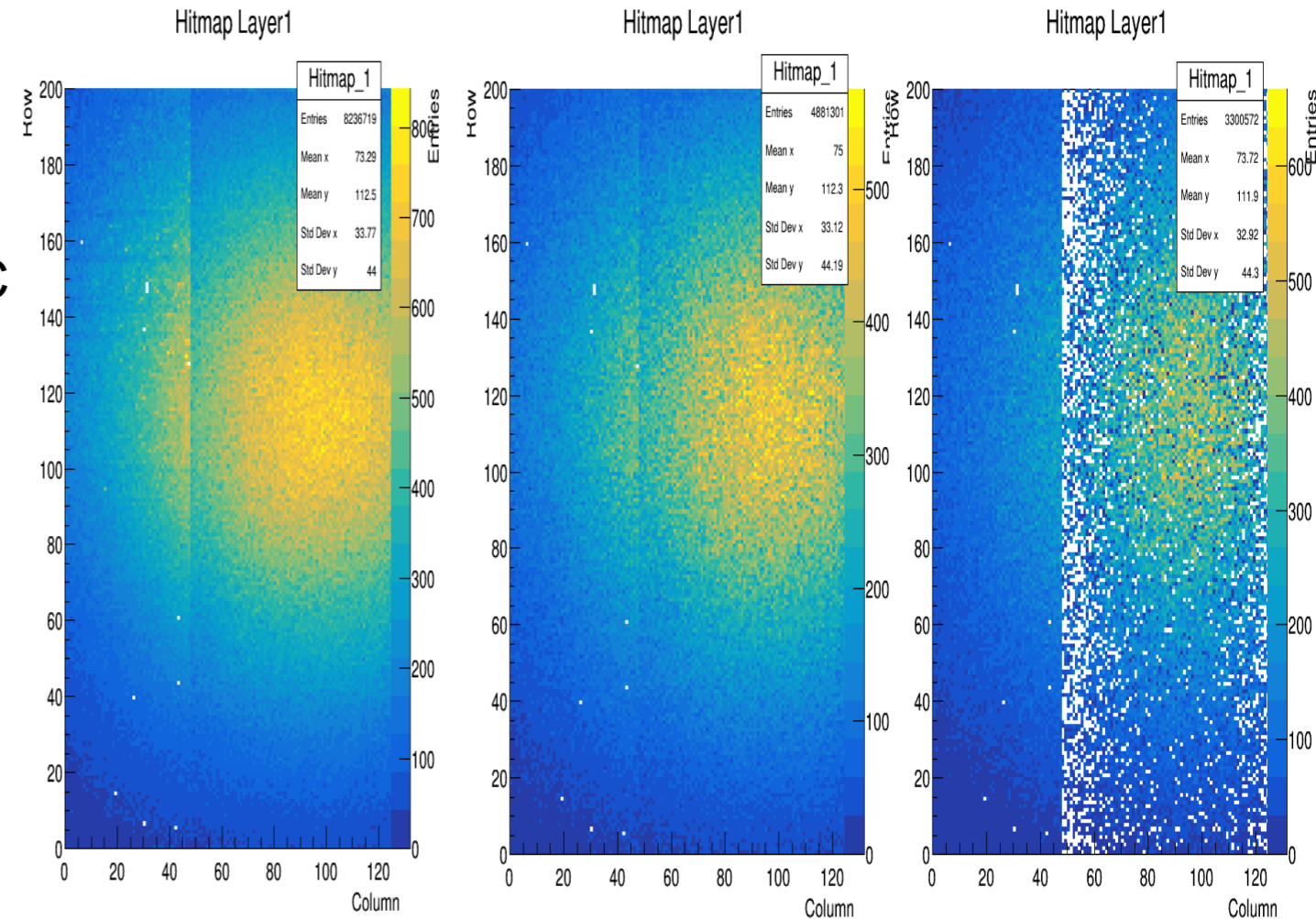
- Inserted MWPC into beam to get wider spread
- Only used matrix A for alignment

Column and Row Correlations for all matrices after alignment:  
DUT: HV = 50 V and ThHigh = 600 mV

- For data taking:  
Keep tracking layers (L0, L2, L3) at  
HV = 50 V and  
ThHigh = 600 mV (100 mV above baseline)
- Vary DUT (L1): HV 10 V – 50 V (10 V steps),  
ThHigh 550 mV – 650 mV (5 mV steps)
- Faster RO statemachine settings for MuPix  
(timerend = 0)
- No rate problems due to beam intensity  
(usually seen in row correlations)



- Overall different response from matrix A and B/C (sharp cut)
- Smaller / different Threshold range to operate Matrices B/C
- No difference in response between B and C (at least at lower beam intensity)

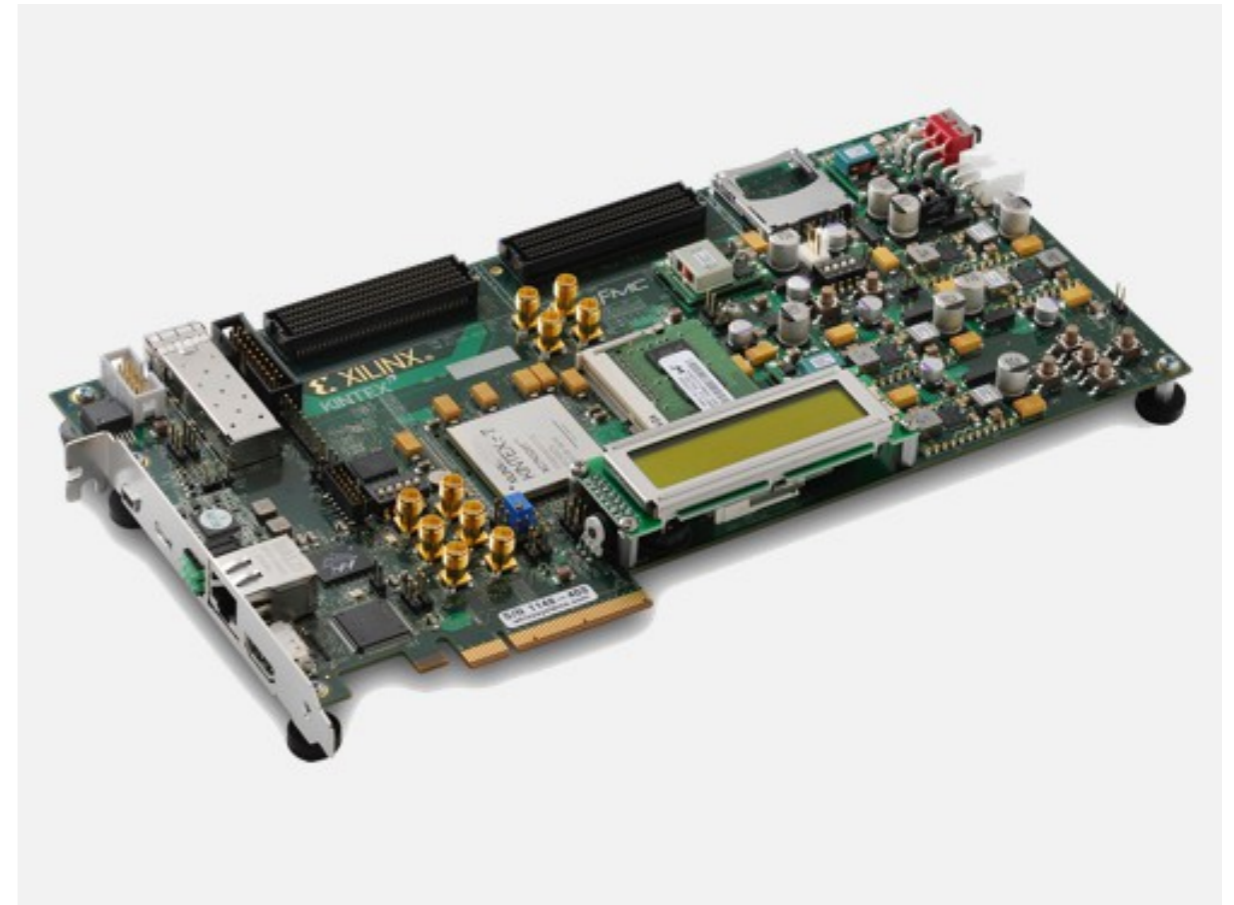


DUT @ HV = 50 V and ThHigh = 550 mV, 600 mV, 650 mV

- Limitations of the TRBv3:
  - Current mupix firmware incompatible with SODAnet
  - black box / magic
  - Unsuitable for Lumi prototype (max. one Sensor per peripheral FPGA)
- Use new readout unit based on EMC Digitizer (designed by P. Marciniewski)
  - Uses Kintex7 FPGA
- Kintex7 Evaluation Board for first tests in Bochum and for Lumi prototype

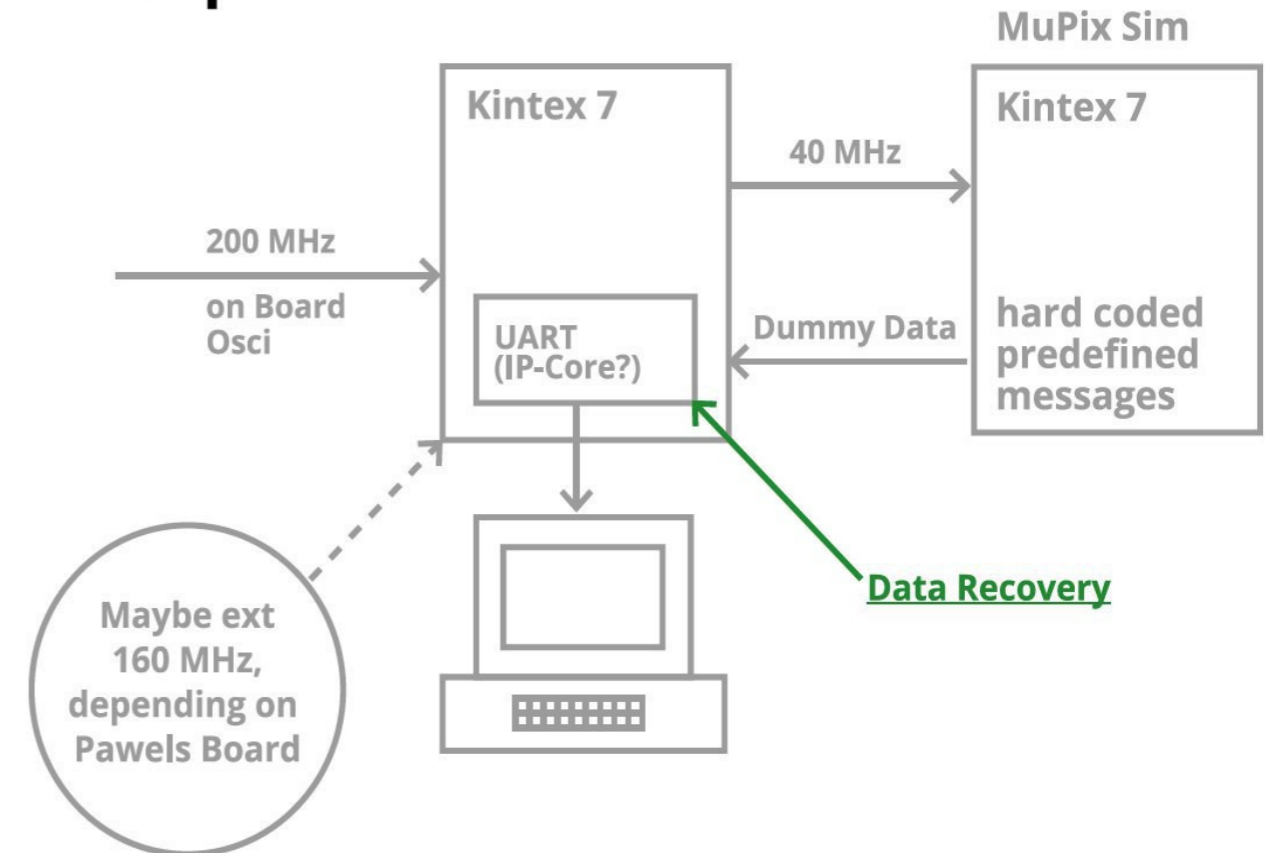
Kintex7 Evaluation Kit by Xilinx

<https://www.xilinx.com/products/boards-and-kits/ek-k7-kc705-g.html>

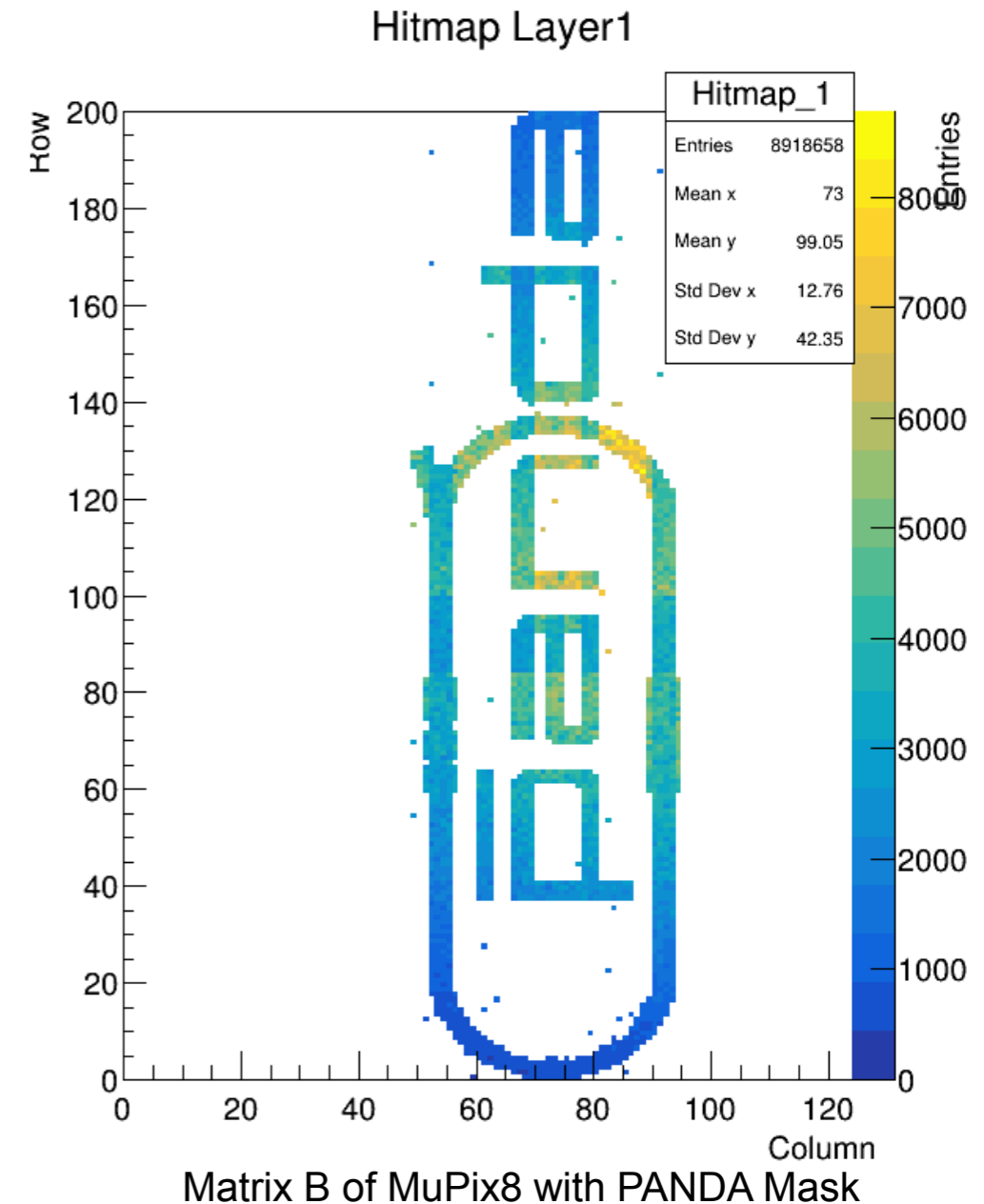


- MuPix Simulation:
  - 1) Create 40MHz clk on one board and send it to second board
  - 2) Create dummy data with fixed known datawords and send it back to first board at 400Mbit/s
  - 3) Synchronize, de-serialize, and 8b/10b decode incoming data stream to recover dummy data
  - ...
  - n) Connect upto 8 MuPixes to one eval board using FMC adapter board
- Later: Use two Kintex7 boards for readout of Lumi prototype (16 MuPixes)
- Final detector: Upto 16 MuPixes per *Pawelboard* (two FPGAs on one board)
  - 20 boards needed for full LMD readout

## LAB Set Up 2



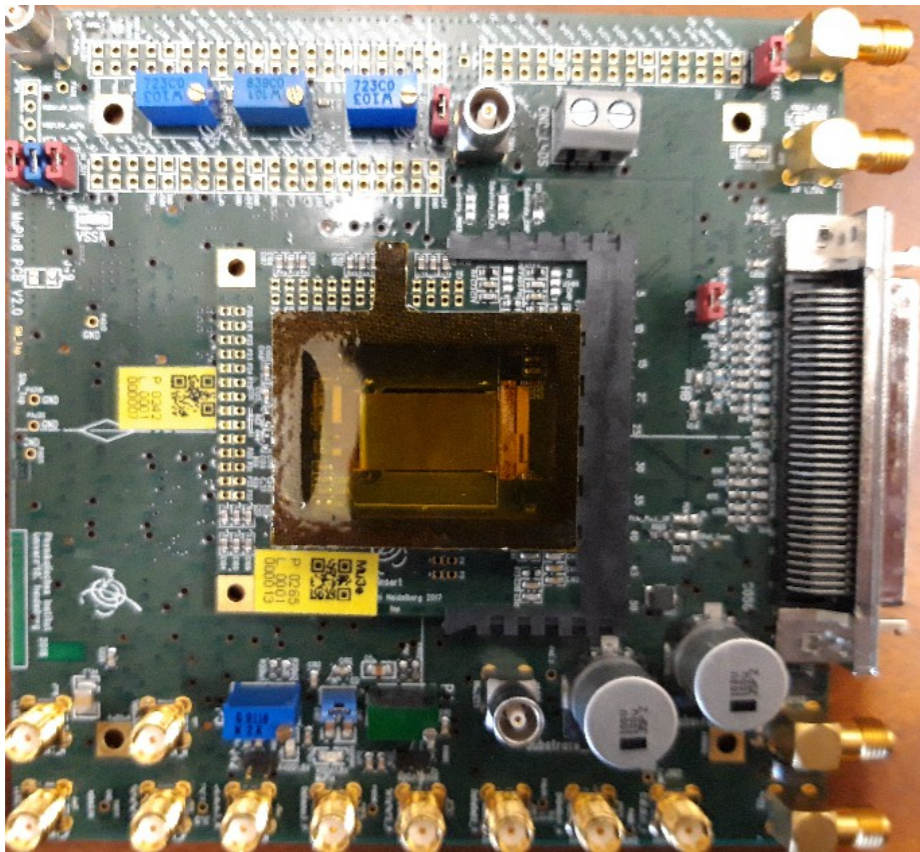
- Testbeam at COSY with four layer telescope
  - Observed correlations in rows and columns
  - New settings for MuPix8 RO state machine  
→ higher rates w/o readout errors
  - All submatrices read out simultaneously  
differences in behaviors are seen
  - Efficiency studies, cluster analyses, etc. are WIP
- New DAQ with Kintex7 FPGA
  - First evaluation kit purchased
  - Planned MuPix data simulation with second board
  - Read out Lumi prototype with two Kintex7 boards



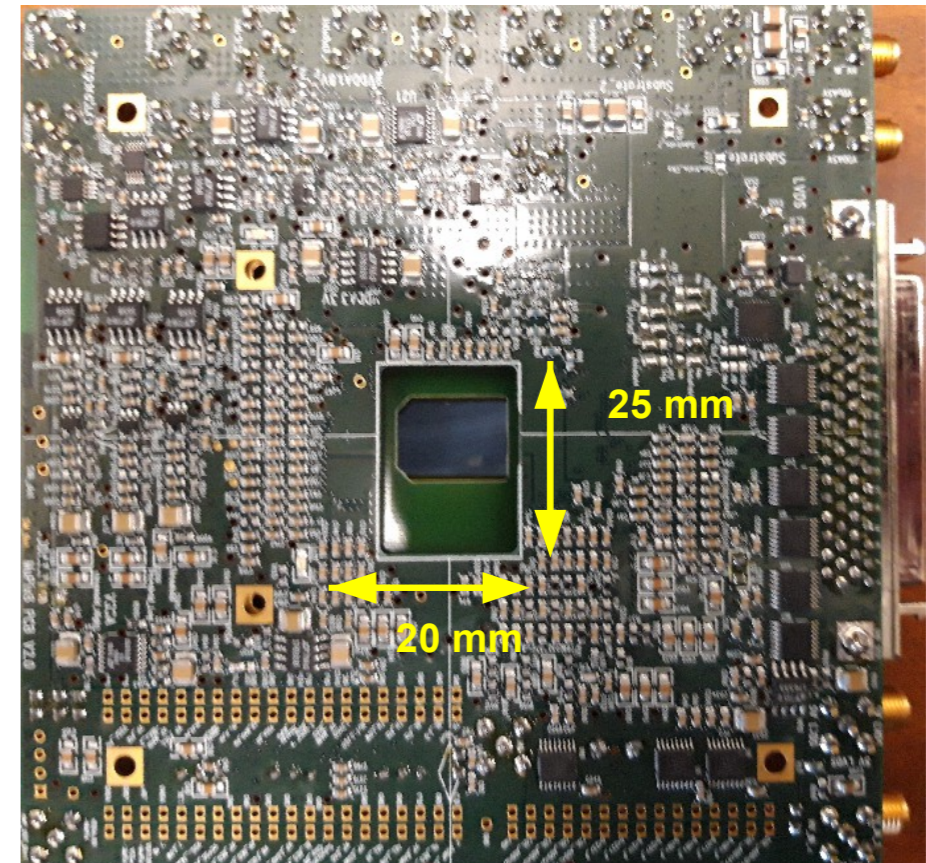
**– Backup –**

- Different substrate resistivities (80  $\Omega\text{cm}$  and 200  $\Omega\text{cm}$ )
- New Sensorboards with adjustable VDD (1.9 V for more stable working point)
- PCB cutout  $\rightarrow$  ideal for usage in telescope setup

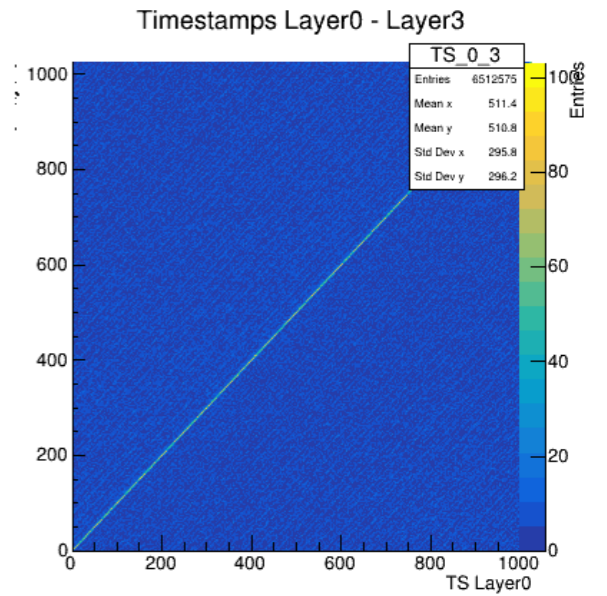
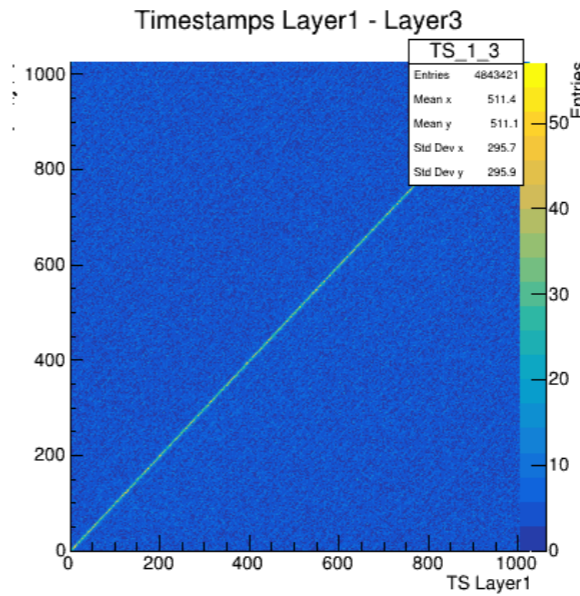
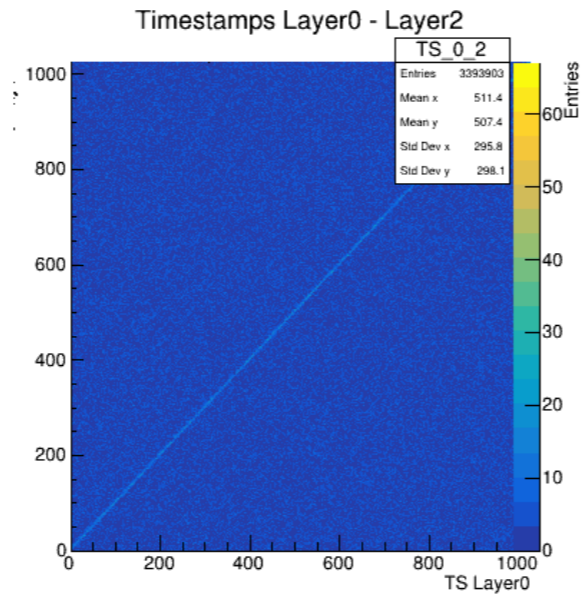
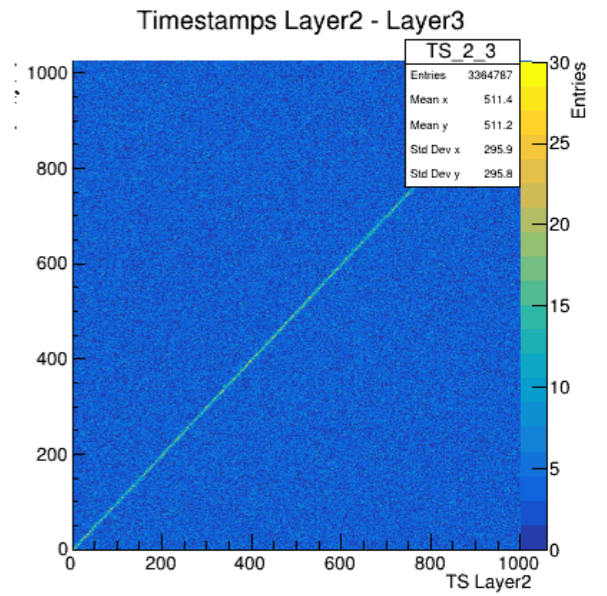
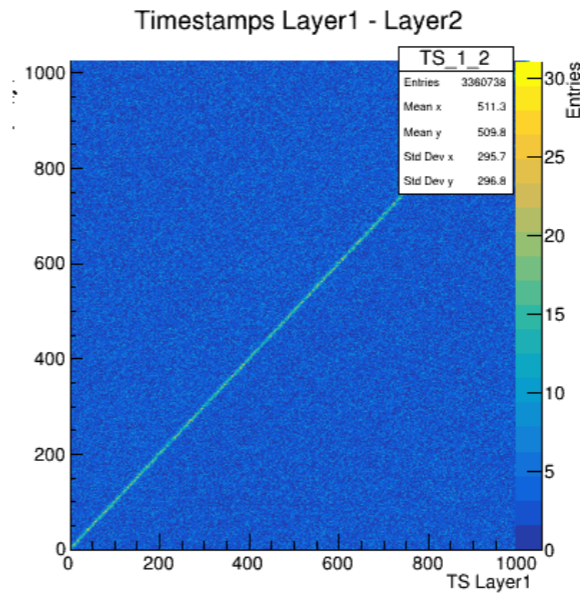
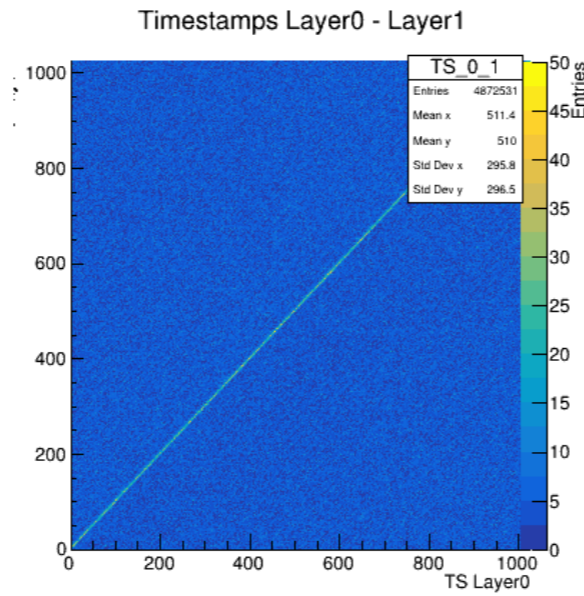
Front side



Back side



- All 4 Layers synchronized





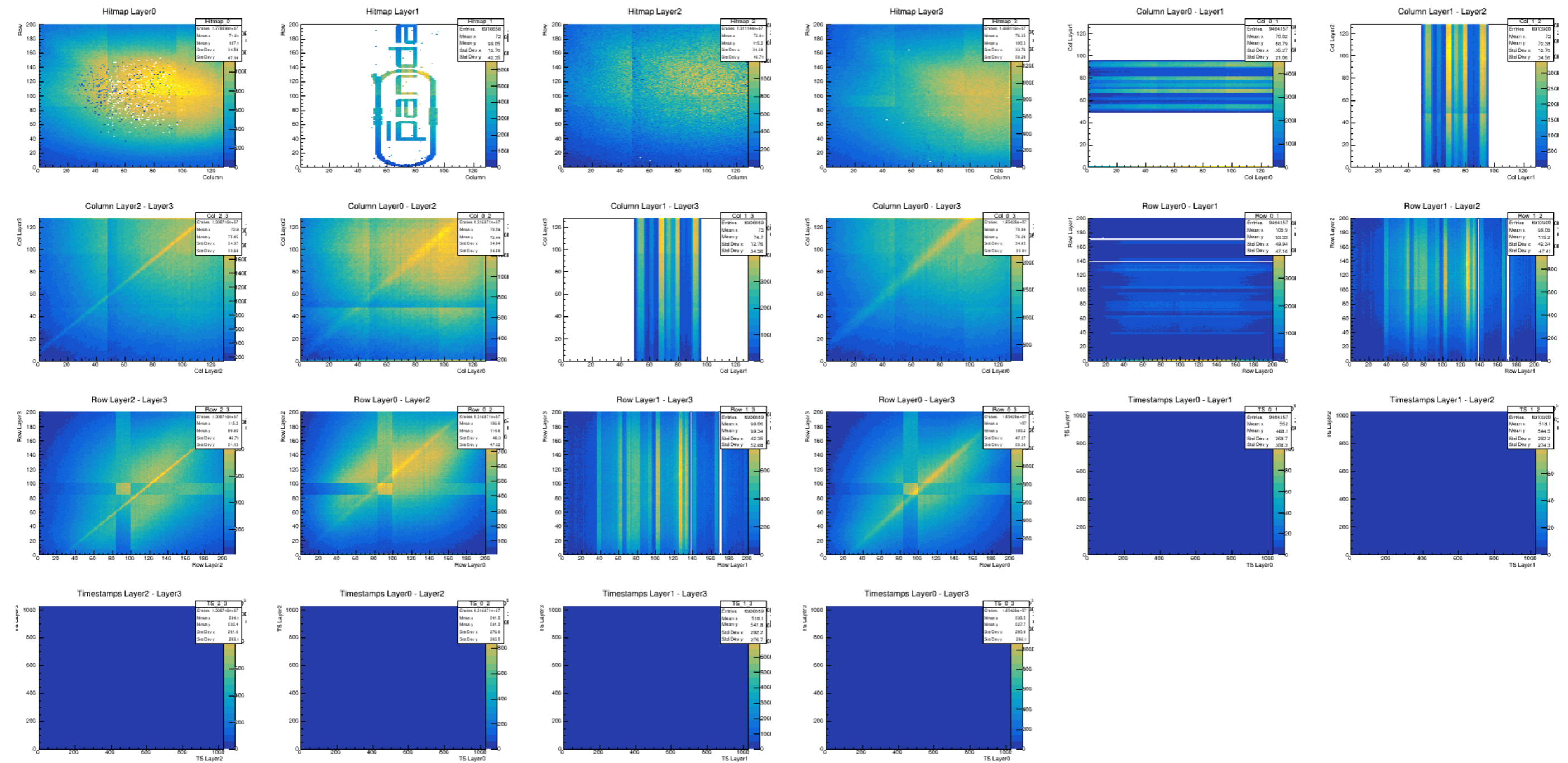
- Priority based readout of digital cells:  
Lower row addresses get read out first
- Physical rows 84 – 99 have highest digital addresses
- Hits get stuck in cells and are read out at a later cycle  
→ pixels are insensitive to further hits during that time
- Current settings:  
ref\_clock = 40 MHz and timerend = 3  
→ approx. max hit rate: 2.3 MHz
- For future: set timerend = 0  
→ max. hit rate  $\approx$  9.2 MHz

Digital Row Address	Pixel Row
0 – 55	—
56 – 139	0 – 83
140 – 239	100 – 199
240 – 255	84 – 99

Row addresses of digital cells (8 bit)

Analogue & Digital DACs		Statemachine & General DACs	
BLResPix	5	VNDcl	c
VNPix	14	resetckdivend	f
VNFBPix	a	maxcycend	3f
VNFollPix	a	slowdownend	0
VNBiasPix	0	<b>timerend</b>	<b>3</b>
VPLoadPix	5	tsphase	0
VNOutPix	a	ckdivend2	7
VNPix2	0	ckdivend	0
BLResDig	5	VNLVDS	3f
VPComp	5	VNLVDSDel	0
VPDAC	0	VPFoll	a
VDel	a	VNDACPix	0

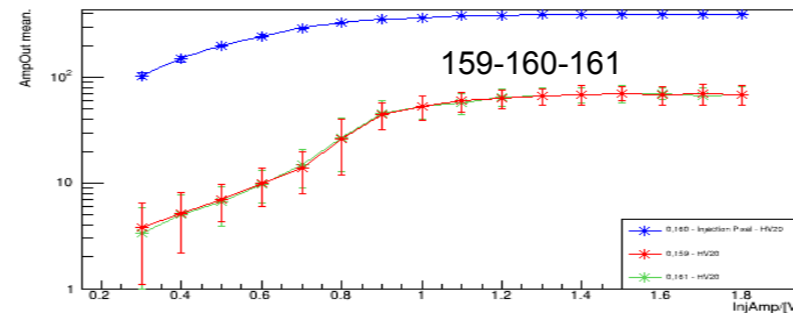
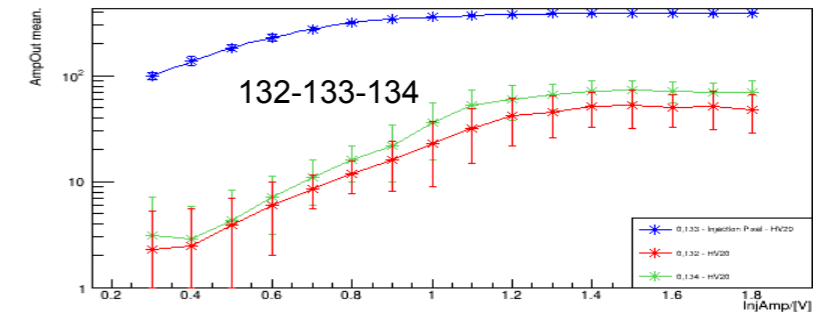
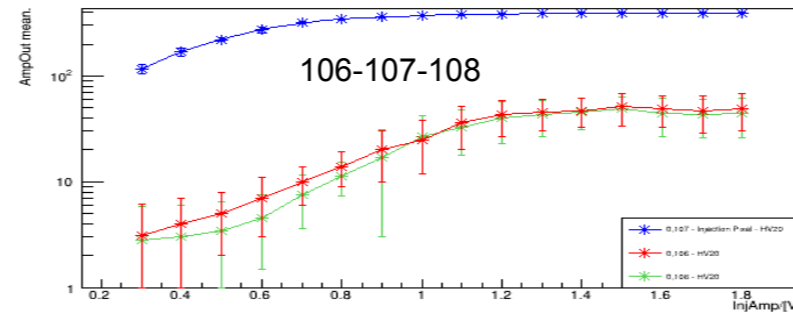
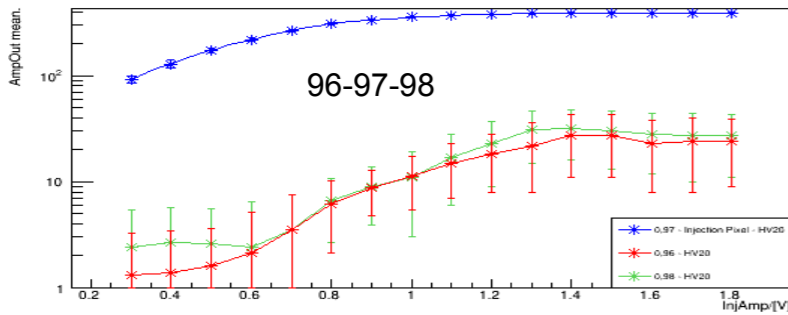
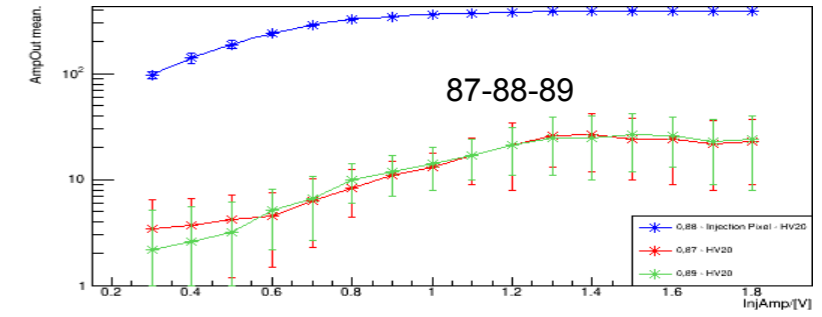
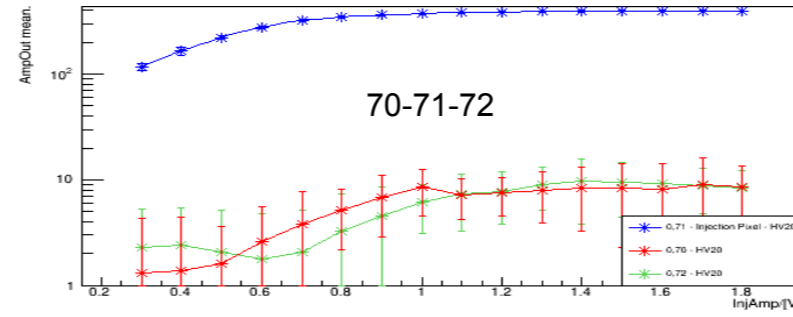
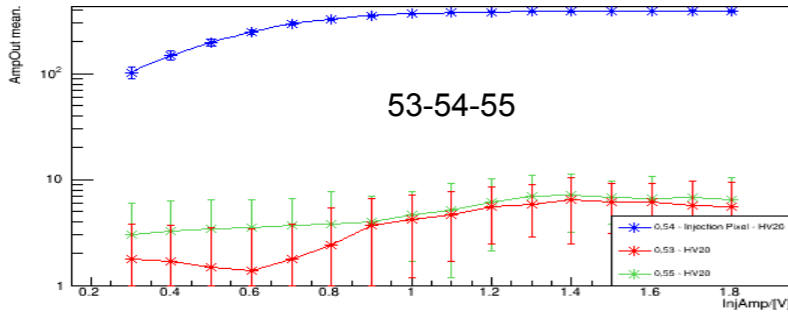
Excerpt from chip config GUI. timerend sets a clock divider that reduces the speed of the readout FSM by (timerend + 1)



# Crosstalk

- Row dependence of crosstalk in Matrix A
- Using analog amplifier readout

- Injected pixel (blue) and neighboring pixels (red/green)



# Recap: Last November

- Cluster analysis of testbeam data (MAMI october 2018)
- Different cluster sizes show different distributions
- Multi clusters (three or more pixels) show pattern related to crosstalk

