ToASt ASIC development update

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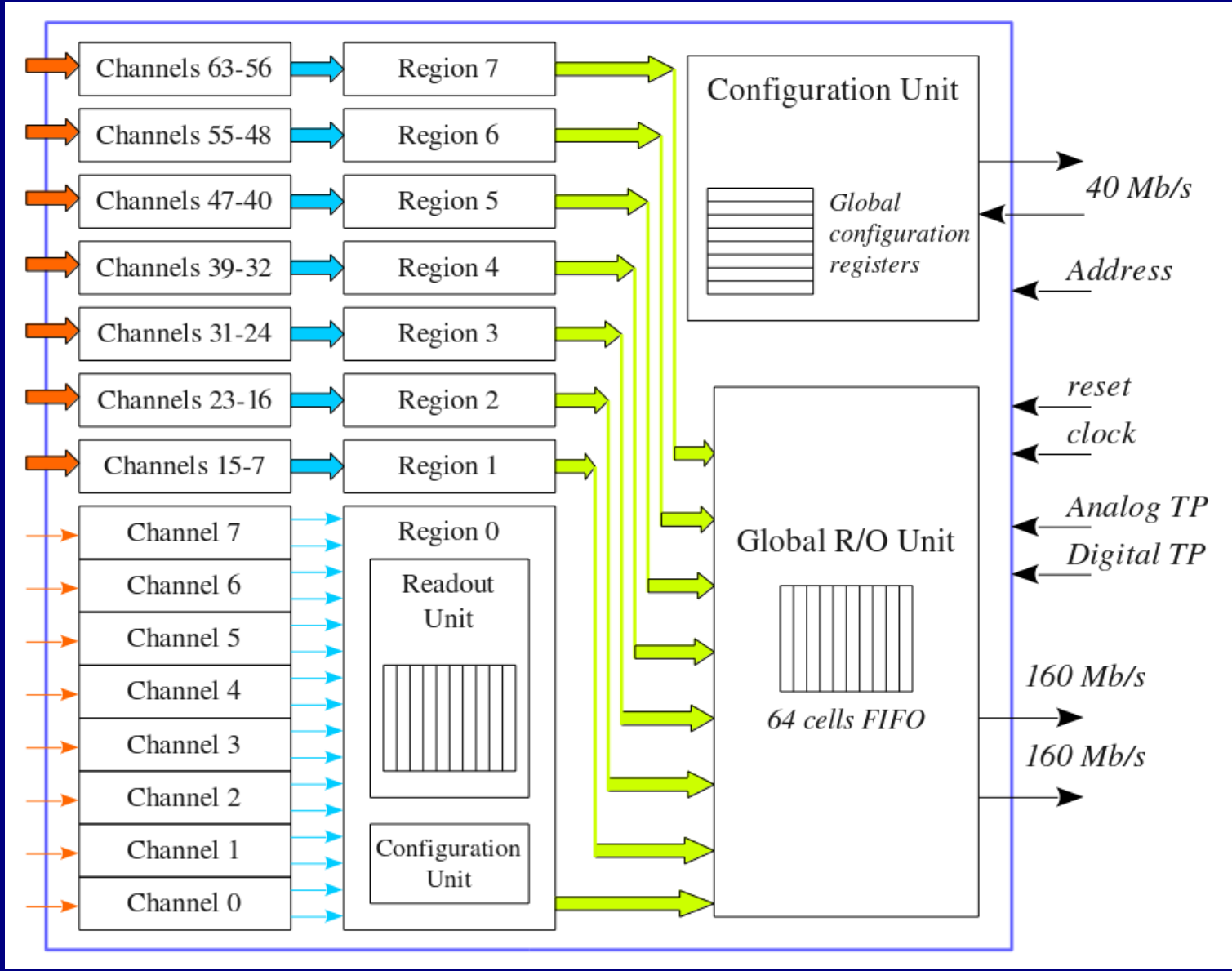
Specifications

Specification	Min	Max	Unit
Input capacitance	2	17	pF
Max rate per strip		40	kHz
Input charge	1	40	fC
Noise		1500	e^-
Preamp peaking time	50	100 (?)	ns
Channels per chip	64		
Reference clock		160	MHz
Charge resolution	8		bits
Time resolution (pk-pk)		6.25	ns
Time resolution (r.m.s.)		1.8	ns
Power consumption		256	mW
Chip dimensions	4.2×3.5		mm^2
Pads position	On two sides only		

ToASt main characteristics

- 64 input channel channels
- Time of Arrival (ToA) and Time over Threshold (ToT) measurements
- Master clock frequency : 160 MHz
- Region : groups of 8 channels with local FIFO
- Second level FIFO buffering for the 8 regions
- Two output serial links at 160 Mb/s
- Serial configuration protocol at 40 Mb/s
- SEU protection for registers and FSM
- CMOS 0.11 μm technology

ToASt architecture



ToASt preliminary pinout

Pin name	Direction	Description
in[63:0]	In	Analog inputs
SyncReset	Rx	Synchronous reset
ChipAddr[6:0]	In	Chip address
TestPulse	In	Digital test pulse
CfgRx	Rx	Configuration receiver
CfgTx	Tx	Configuration transmitter
TxOut_0	Tx	Data serial output 0
TxOut_1	Tx	Data serial output 1

Digital logic status

Task	Status
HDL code of the channel/region/chip readout logic	done
HDL code of the chip configuration logic	done
HDL code of the serializers	done
8b10b output encoding	to be done
TMR based SEU protection	done
Header and trailer insertion with CRC calculation	done
Synthesis	done
P&R	done
Signoff and test	ongoing

Analogue front-end status

Task	**Status**
Removal of the TDC section	done
Redesign of the power distribution	done
FE bias bug fixing	ongoing
Peaking time adjustment modification	ongoing

Notes on the analog FE

- Power distribution requires significant improvement :
  - Cell level : power lines moved to upper layers
  - Chip level : replace ME7 with ME8 on vertical power distribution for minimum resistance
  - Pad level : power pads on top and bottom.
- Bug in the preamp bias to be corrected (not possible to reach nominal current without negative supply)

Summary

- Development for the PANDA MVD strip detector :
  - 64 channel ASIC
  - Configurable for both input signal polarities.
  - Time of Arrival measurement with system clock resolution
  - Charge measurement via Time over Threshold
  - Local FIFOs for data de-randomization
  - 2×160 Mb/s serial outputs
- BE design almost completed
- FE design under optimization
- Submission foreseen for 4Q2019 or 1Q2020 *(to be confirmed)*