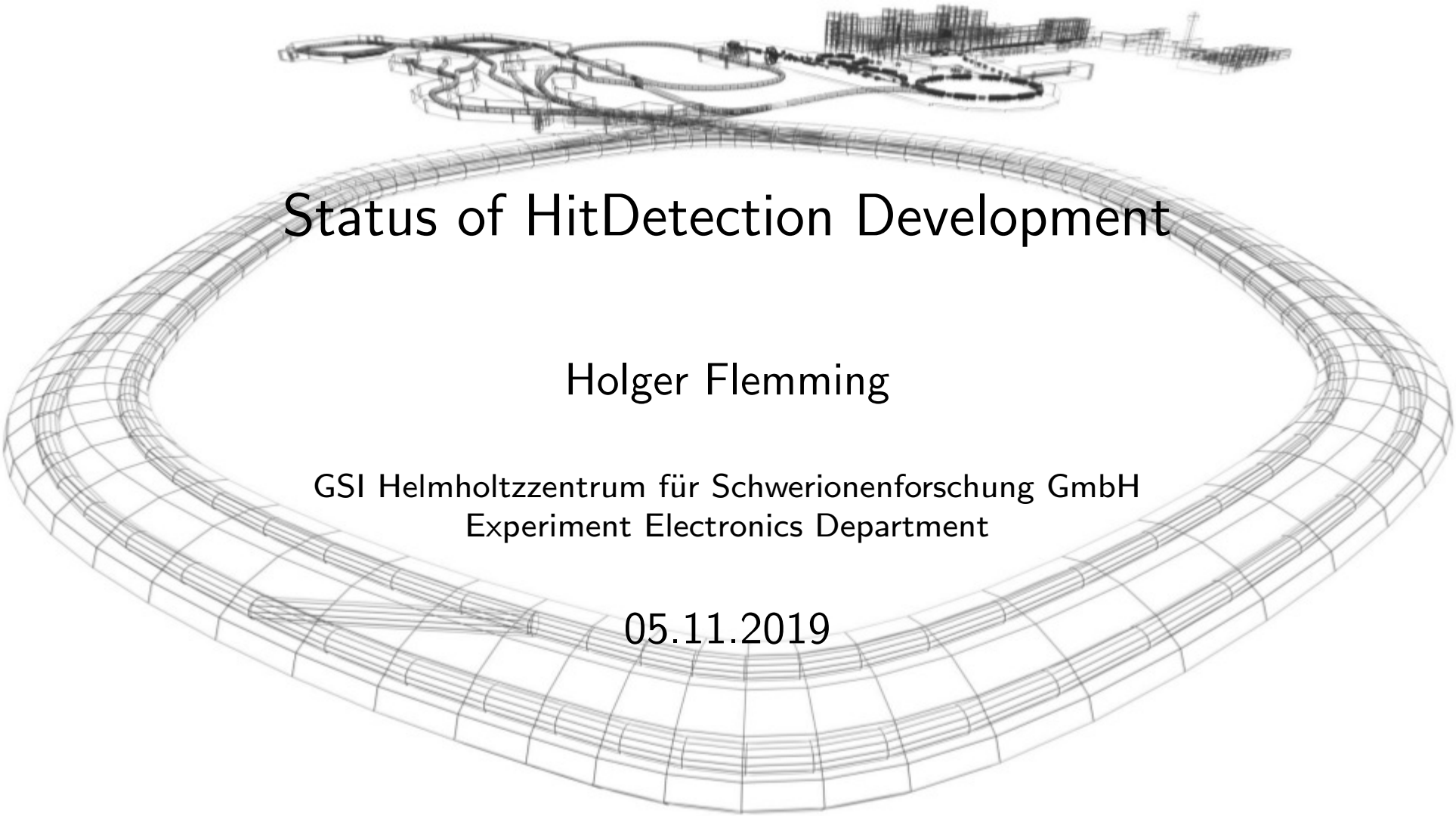

Status of HitDetection Development

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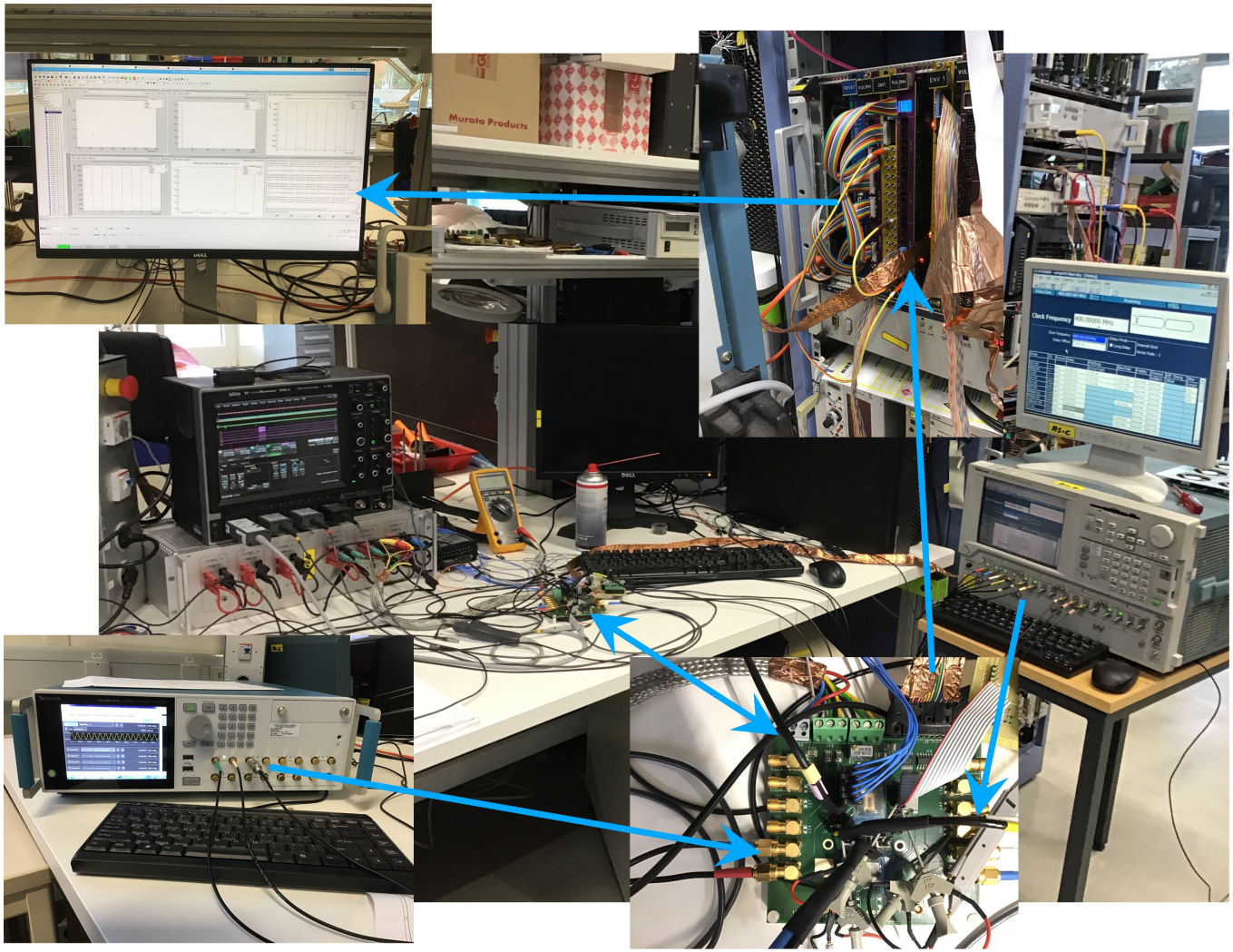
Experiment Electronics Department

05.11.2019

Outline

Outline

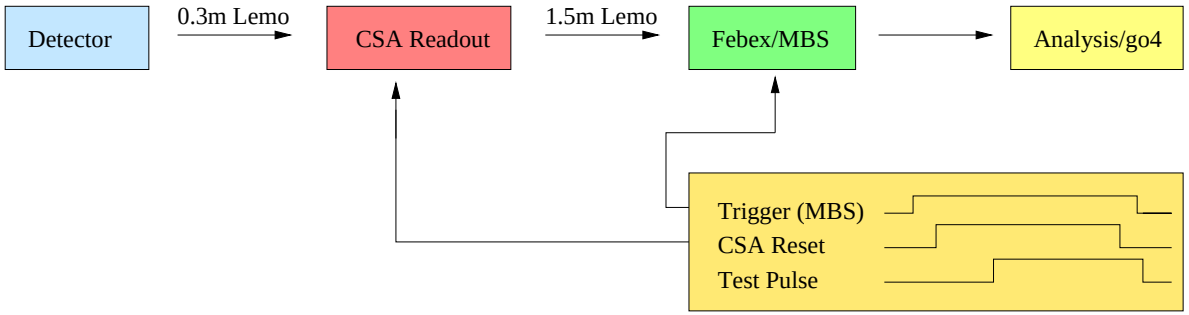
- Previous ASIC Version: Corrupted Data due to wrong ADC timing model during logic synthesis
- New ASIC under test
- Initial test setup bugs are fixed
  - Bonding problem: One clock input shortened to scribe line
  - Bit errors in data stream observed $\rightarrow$ timing problem in FPGA of readout board
- ASIC is fully operational!
- Measurements for ADC characterisation are done. Data will be analysed now
- Second measurement setup will be installed in Mainz


Murata Products

- Characterisation will be continued in Mainz
  - ADC
    - Analyses of data already taken
    - DC Scan
  - Characterisation of Analogue Memory cells
  - Extracting calibration constants for linear calibration of individual analogue memory cells
  - Determination of linearity and dynamic range of full analogue path
- Realisation of full detector readout chain
  $PbWO_4 \rightarrow$ APD $\rightarrow$ APFEL $\rightarrow$ HitDetection $\rightarrow$ DAQ

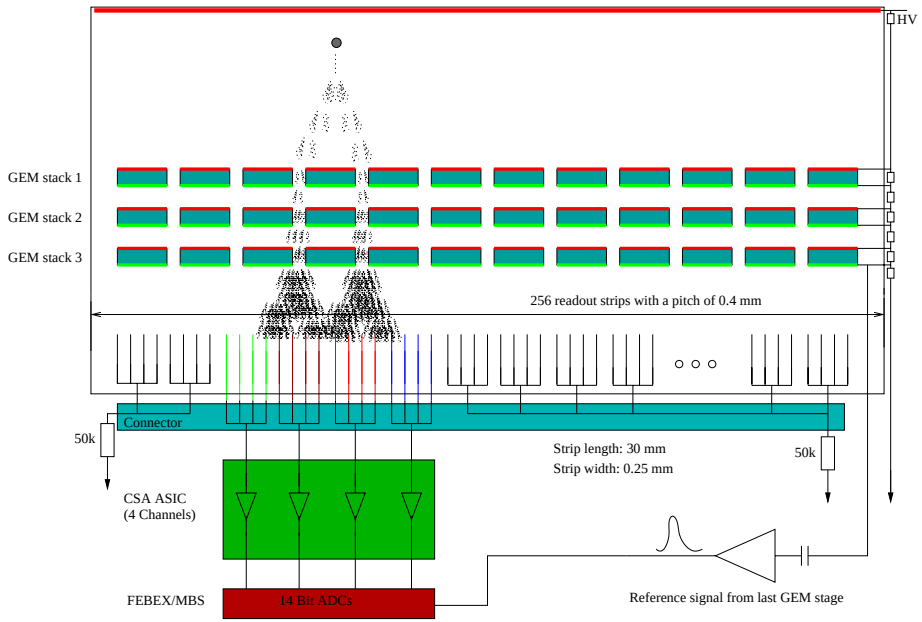
Outline

- Multi purpose read out ASIC for a wide range of detectors
- Discussed application: Common read out ASIC for PANDA GEM tracker and SFRS GEM-TPC
- Requirements:
  - Large dynamic range (SFRS: ≈ 85000)
  - High granularity
  - Time precision ≈ 1 ns
- Front end based on a charged sensitive amplifier with dynamically switched capacitive feedback[Wie19]
- Test ASIC with four analogue channels available for tests.
- First detector tests have been done in April



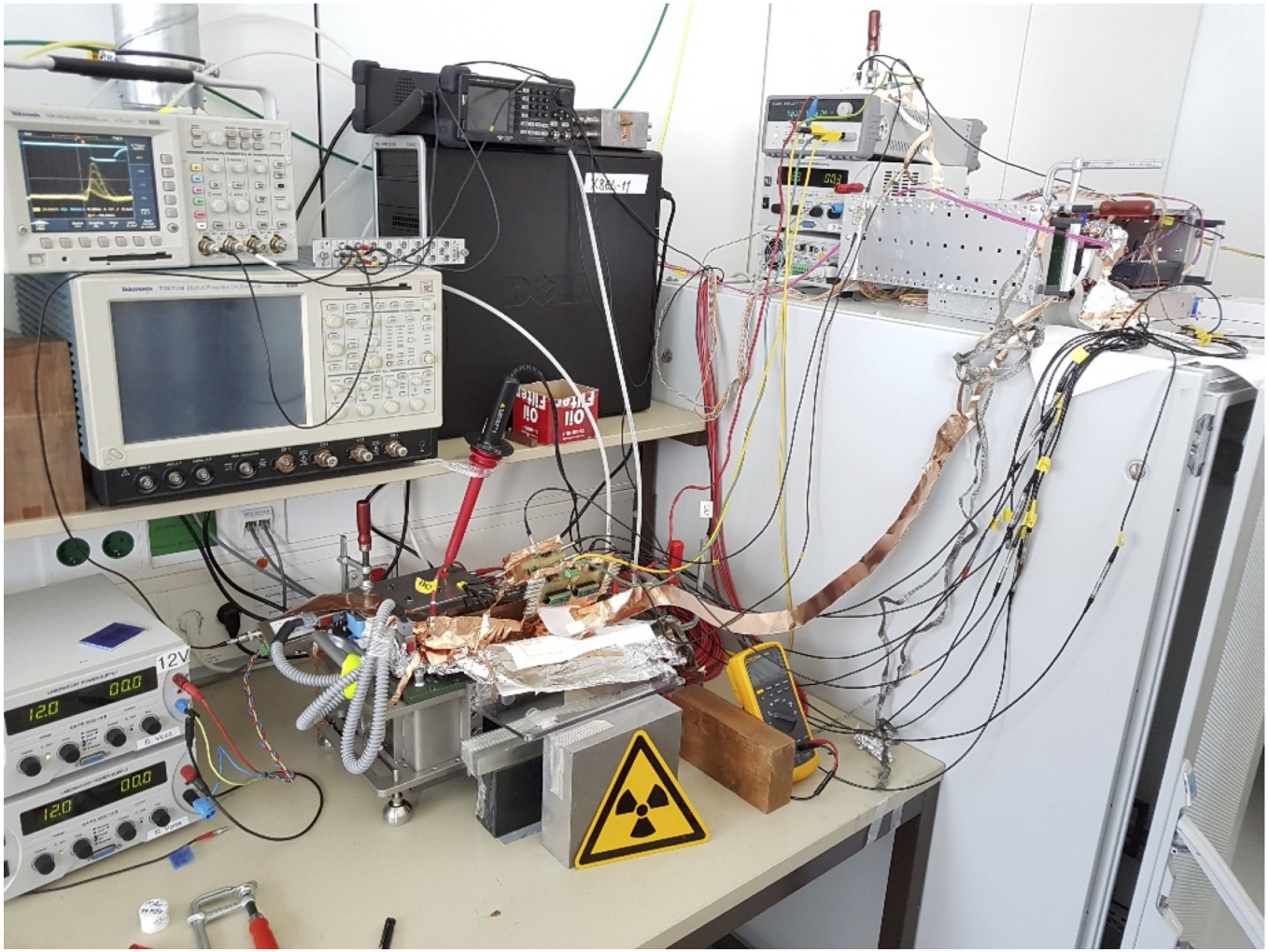
- GEM - Detector
- Read out of eight channels
- FEBEX board as digitiser unit
- Go4 for data analysis (online/offline)
- Trigger unit

courtesy of Peter Wieczorek



- Subsection readout of the GEM detector
  - Combined 4 strips together to readout with one channel
  - Readout of 4 and later 8 channels in total
- Reference signal from GEM electrode

courtesy of Peter Wieczorek

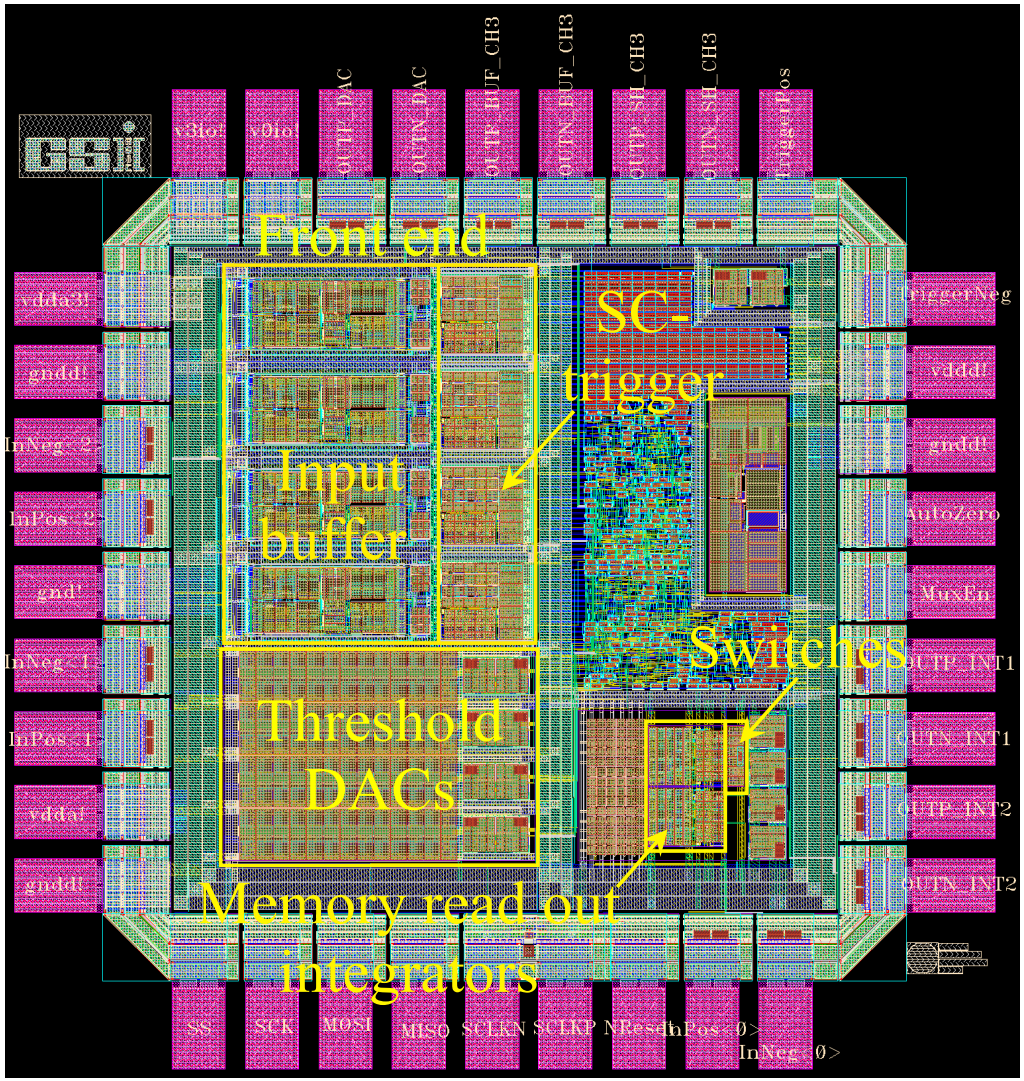


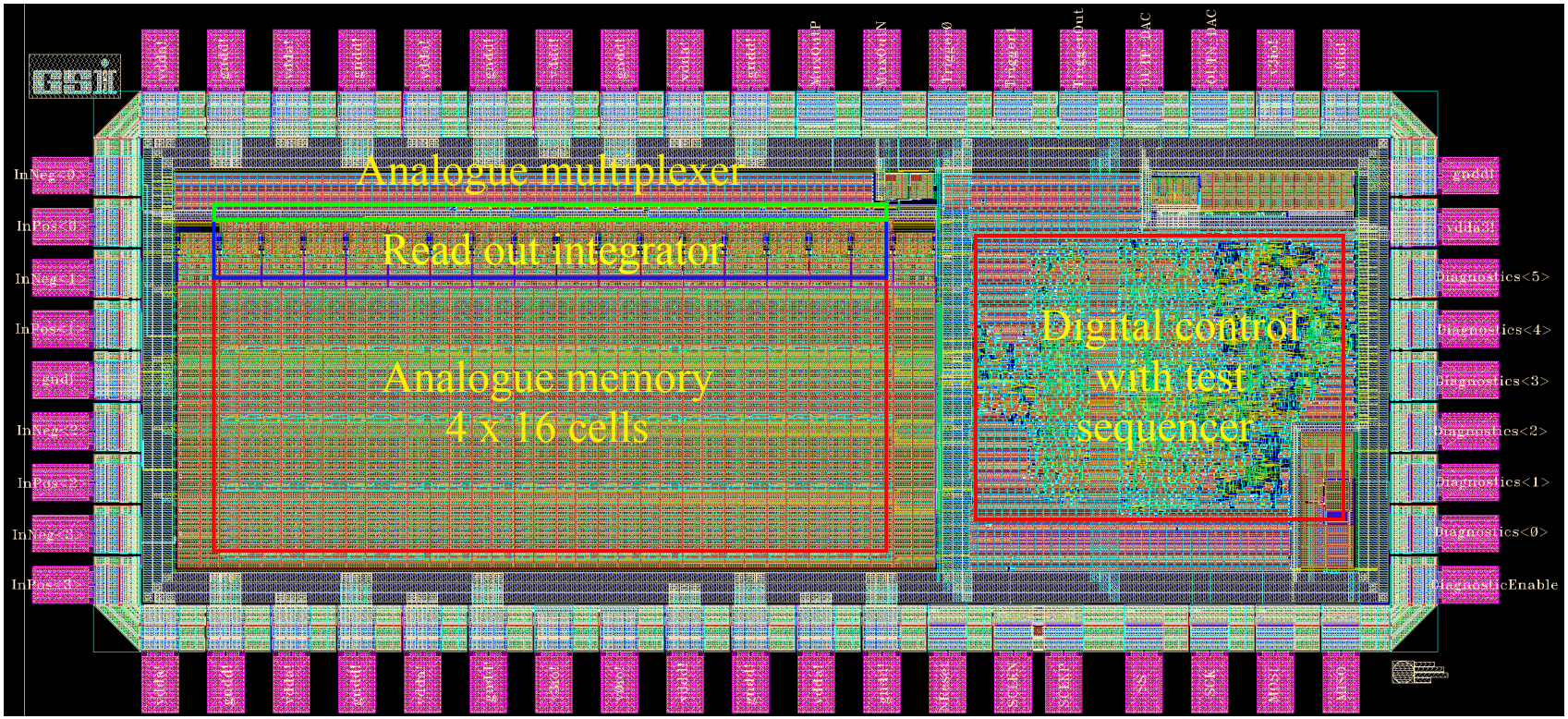
courtesy of Peter Wieczorek

- GSI CSA operates together with GEM detector!
- Measured noise level: $\approx 0.2 \ldots 0.4$ fC
- Beam time in December
  - Read out of 256 channels
  - Learning more about the detector and its read out
  - Input for GEM TDR
- In parallel a beam time with a SEM grid detector and the CSA will take place for FAIR beam diagnostics

Outline

- New analogue front end designed for APFEL-read out.[Fle19]
  - Bandwidth control by configurable input buffer feedback
  - Switched capacitor trigger stage to trigger on differentiated signal
- Enlarged analogue memory matrix
- Modified memory control interface
- Implemented on two test ASICs
- Aim: test and characterisation of individual analogue blocks
- Submitted in July, delivery of chips expected soon

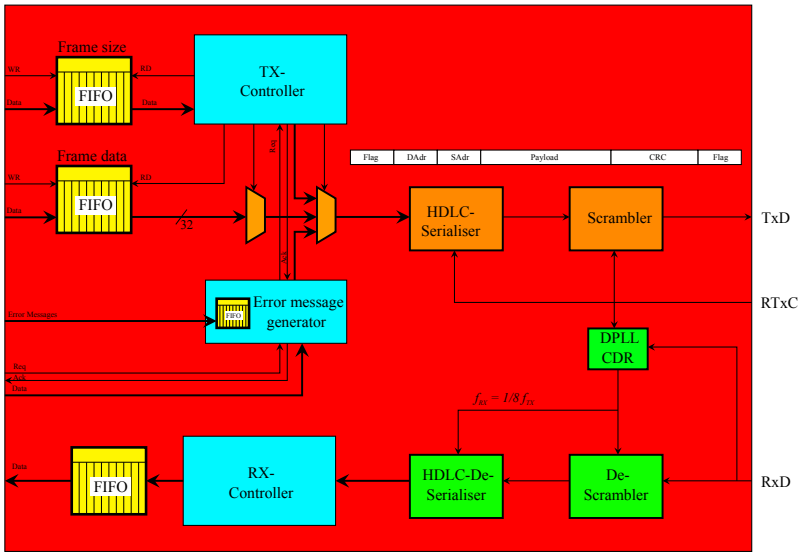

Front end
SC-
trigger
Input
buffer
Switches
Threshold
DACs
Memory read out
integrators


Analogue multiplexer
Read out integrator
Analogue memory
4 x 16 cells
Digital control
with test
sequencer

- Two similar ASIC needed
  - 16 channel HitDetection ASIC for EMC read out
  - 32 channel HitDetection + CSA for GEM read out
- Aim: obtain as much modularity as possible
- Core block: 4 channel analogue transient recorder block
  - Analogue memory, read out integrator, analogue multiplexer
  - Memory write and read out logic
  - Signal digitisation (12-bit Pipeline ADC)
  - Digital correction unit for memory cell characteristics
  - Event builder
- Design 90 % finished

- Two different Front end blocks
  - 4 channels
  - Input buffer and SC-trigger for APFEL-readout
  - CSA for GEM read out
  - Threshold-DACs
  - Digital interface for Threshold and Feedback control
  - In case of dynamically switched feedback: signalling of CSA amplification
- Determination of Analogue memory calibration constants on chip
  - Integration of a simple slow control CPU

Back end interface



- External clock used for transmitter (max. 500 MHz)
- Receiver clock fixed to $f_{RX} = 1/8 f_{TX}$

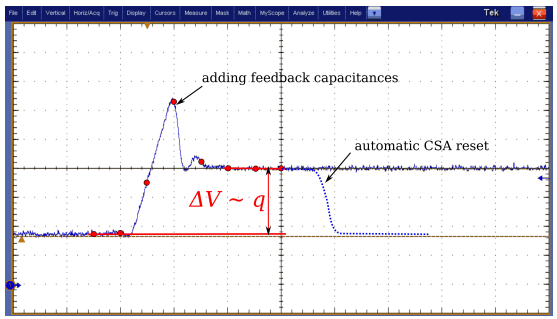
- Data sources:
  - Detector data frames
  - Status/Error messages
  - Wishbone bus access response
- Serialiser / Deserialiser based on HDLC standard[HDL02]
- Self synchronising scrambler to avoid DC components $x^{17} + x^{12} + 1$

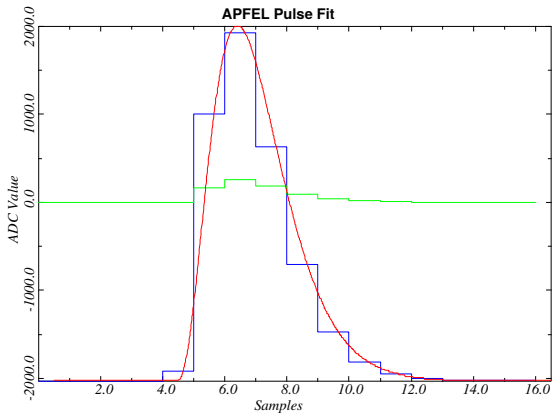
Open question

- Different DAQ architecture of experiments
  - PANDA EMC and GEM tracker: Trigger less DAQ
  - SFRS GEM-TPC: Triggered DAQ

→ Latency buffer with trigger selector which can be bypased

- On Chip Latency buffer requires data reduction → feature extraction
- Two completely different pulse shapes: Is it possible to handle this by a configurable feature extraction unit?





Assuming the current test ASICs work as expected:

- Design of full size prototypes can be completed
  - 16 channel HitDetection for APFEL readout
  - 32 channel HitDetection + CSA for GEM readout
- Expected prototyping costs for each ASIC: $\approx$ 30 k€

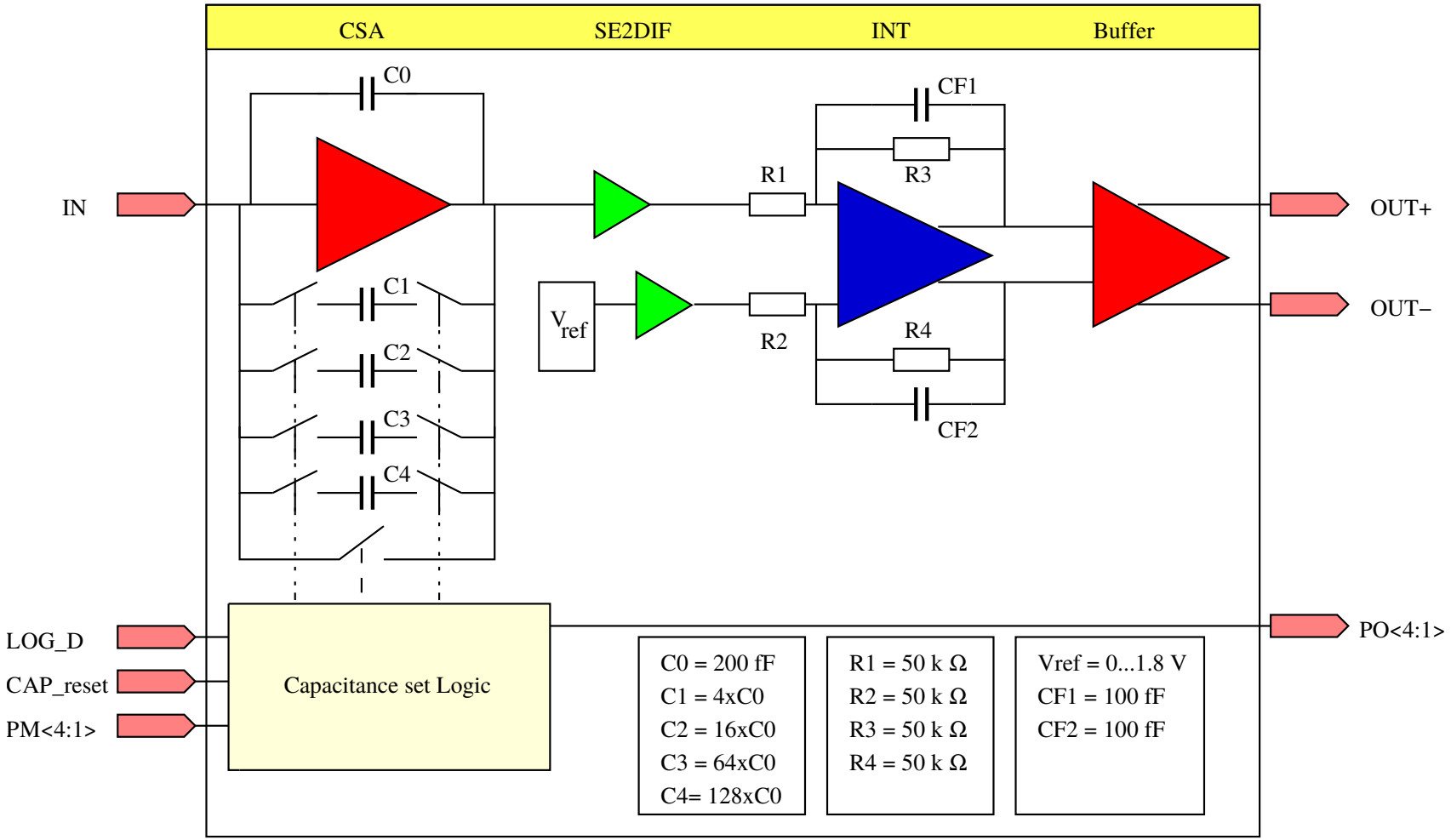
Thank you for your attention

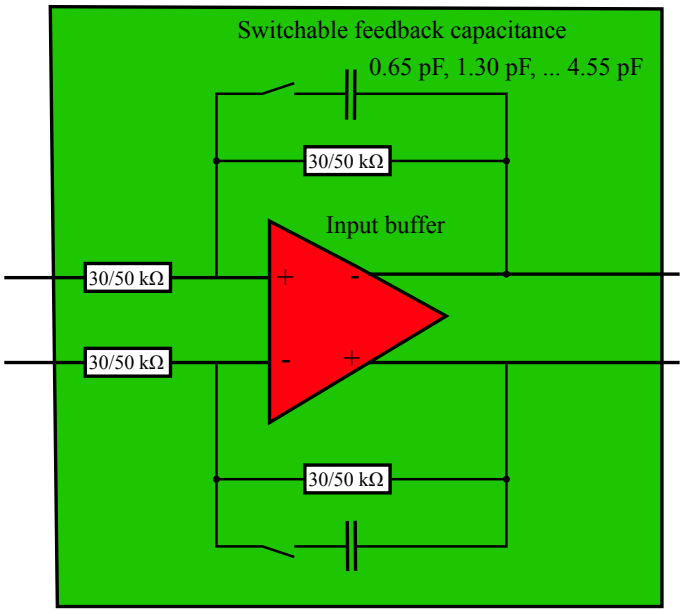

FLEMMING, H.: *HitDetection – Current Activities*, 05 2019
URL https://indico.gsi.de/event/8891/session/0/contribution/9/material/slides/0.pdf


High-Level Data Link Control specifications, 2002


WIECZOREK, P.: *Readout Chain for the GEM Detector -Setup Version 0.1-*, May 2019
URL https://sf.gsi.de/f/97ca5e77dc3a4c7c8abb/?dl=1

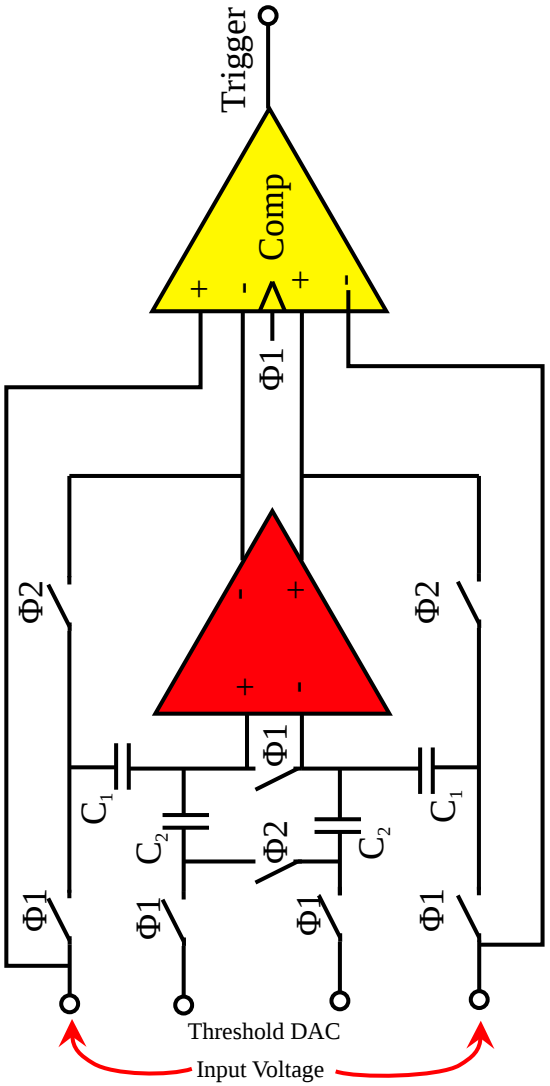
Backup


CSA
SE2DIF
INT
Buffer
C0
CF1
R3
R1
IN
OUT+
C1
Vref
R2
R4
OUT−
C2
C3
CF2
C4
LOG_D
CAP_reset
PM<4:1>
Capacitance set Logic
PO<4:1>
C0 = 200 fF
C1 = 4xC0
C2 = 16xC0
C3 = 64xC0
C4= 128xC0
R1 = 50 k Ω
R2 = 50 k Ω
R3 = 50 k Ω
R4 = 50 k Ω
Vref = 0...1.8 V
CF1 = 100 fF
CF2 = 100 fF



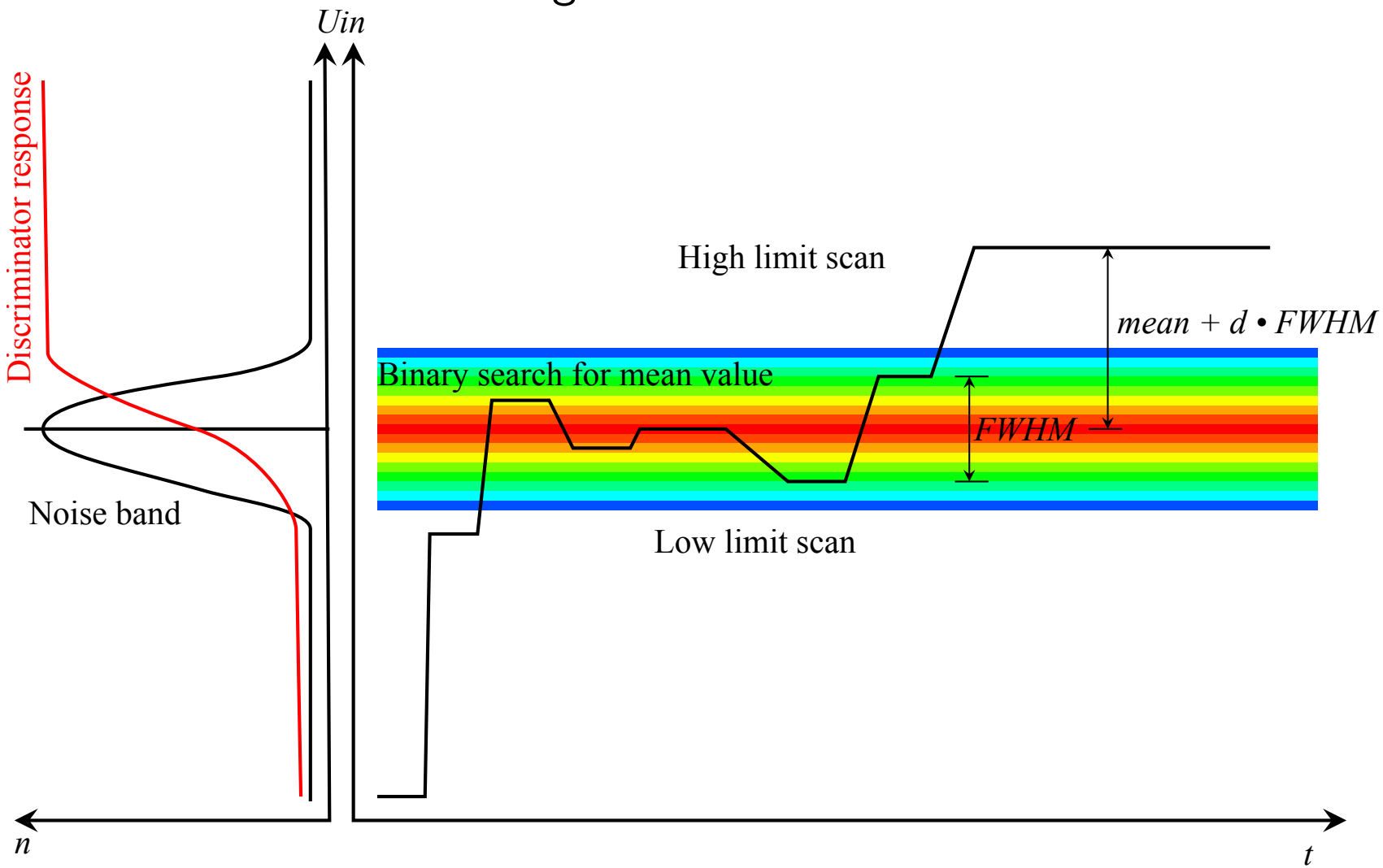
C	$R = 30$ kΩ	$R = 50$kΩ
0	> 50 MHz	> 50 MHz
0.65 pF	8.16 MHz	4,90 MHz
1.30 pF	4,08 MHz	2,45 MHz
4.55 pF	1.17 MHz	0,70 MHz

- Fully differential, gain 1
- Modifications:
  - Input and feedback resistor configurable:
    30 kΩ / 50 kΩ
  - Low pass characteristic by switchable feedback capacitances
    - Anti aliasing
    - Suppression of high frequency pick-up
    - Noise reduction

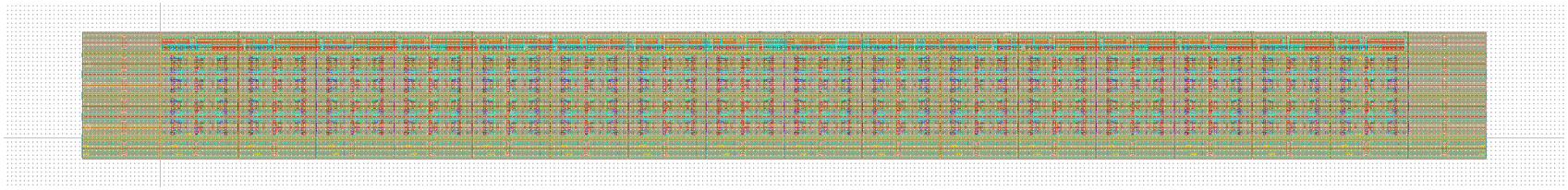


- Φ_1
  - Storing input voltage in C_1
  - Storing threshold voltage in C_2
- Φ_2
  - Switching C_1 into feedback
  - Transferring charge from C_2 to C_1
  - Output voltage: $U_{in} - C_2/C_1 U_{thres}$
  - Used as comparator threshold
- Leading edge of Φ_1
  - Taking comparator decision $U_{in}(t) > U_{in}(t-\Delta t) - \frac{C_2}{C_1} U_{Thres}$ $\Rightarrow \frac{\Delta U_{in}}{\Delta t} < \frac{C_2}{C_1} U_{Thres}$

Automatic threshold setting

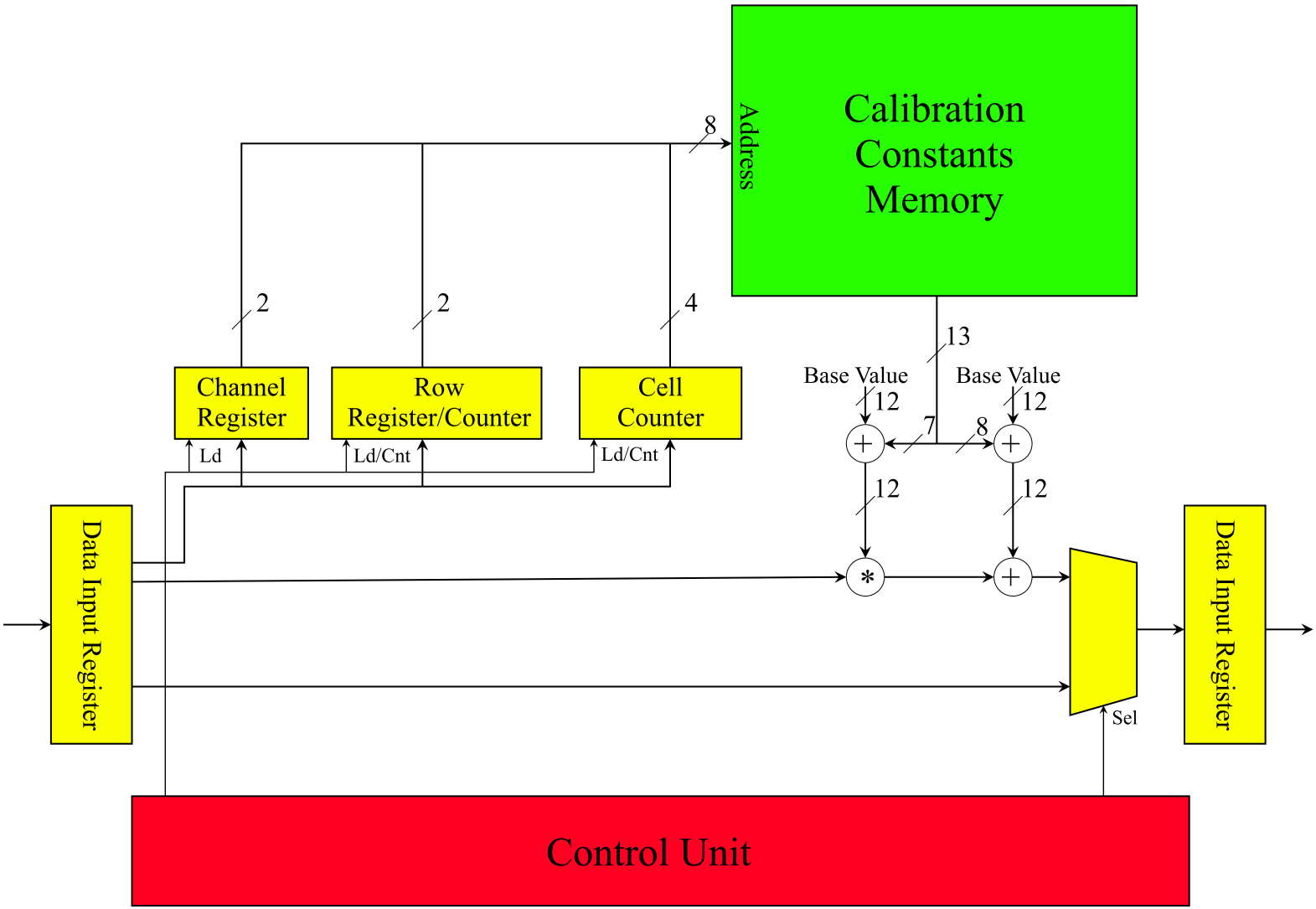


Analogue Memory

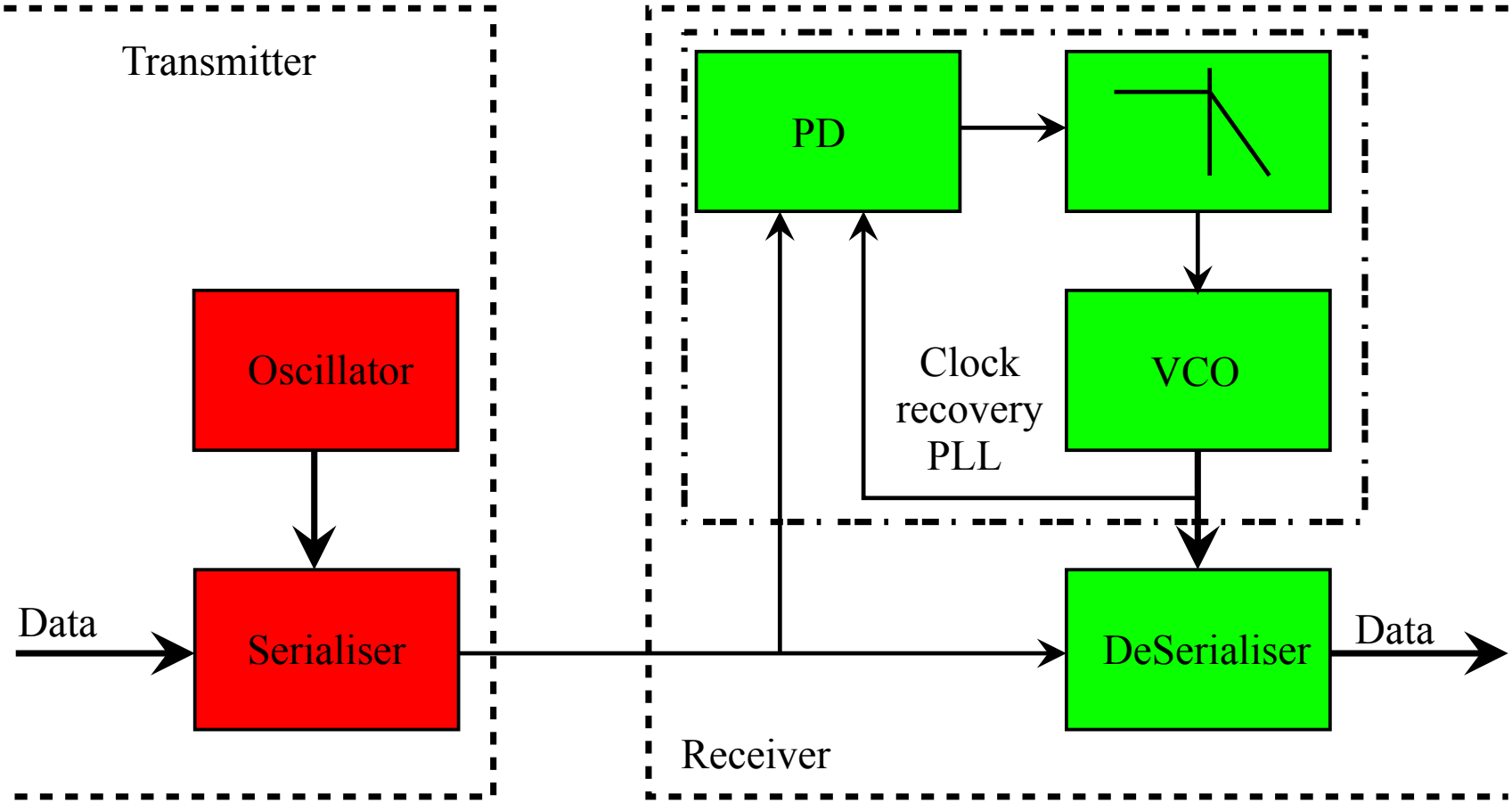


- Number of columns is increased from 8 to 16
- Four Rows / channel for derandomisation
- Cell to cell variations observed in 4 channel prototype: $\frac{\Delta S}{\bar{S}} = 0.022$, $\frac{\Delta Y}{\bar{Y}} = 0.060$
- On chip correction implemented
- Inputs can be connected to on chip DAC controlled reference voltage for parameter determination

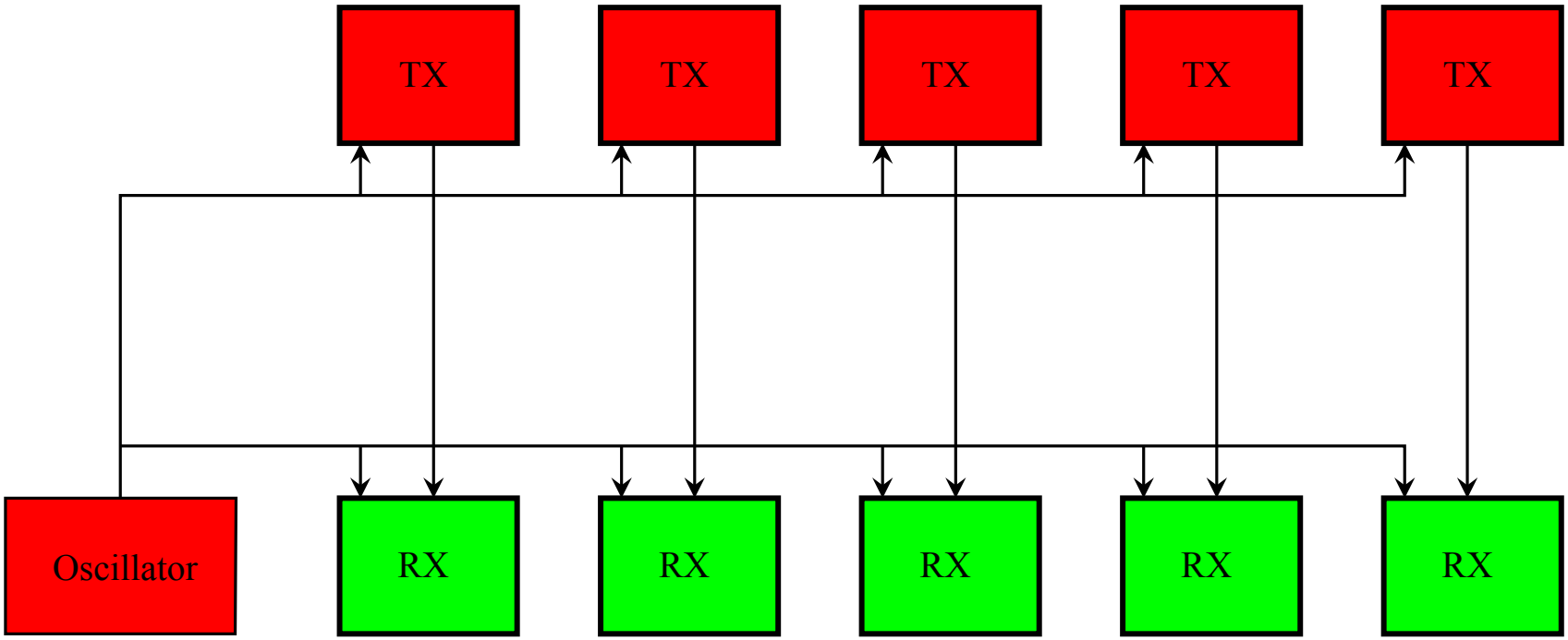
Digital Memory Correction



Serial communication requires clock recovery in receiver

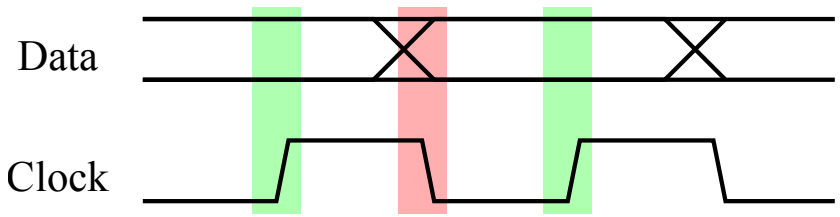


Common external clock

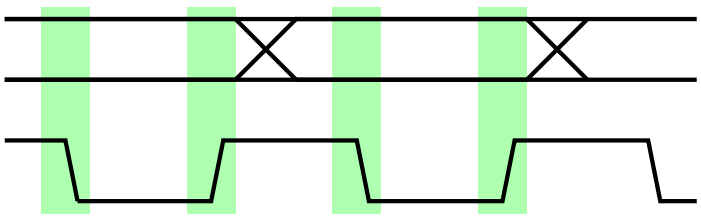


- pro: No clock recovery PLL required in receiver
- con: Additional clock distribution

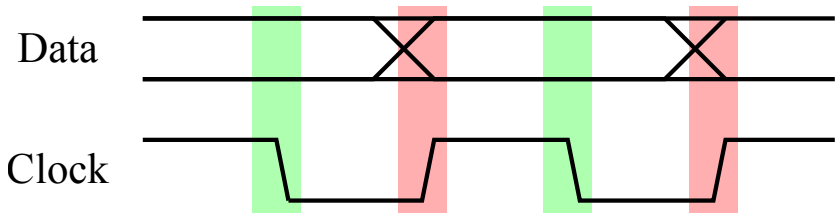
- Clock phase fixed but unknown
- Experience from CBM GET4 readout:
  For reasonable data rates at least one clock edge samples the open eye
- Clock edge determination by bit error rate test



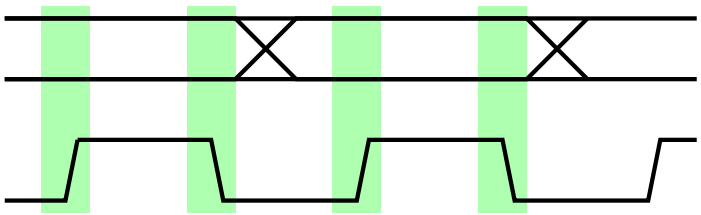
Data sampling on rising clock edge



Data sampling either on rising or falling clock edge



Data sampling on falling clock edge



Data sampling either on rising or falling clock edge