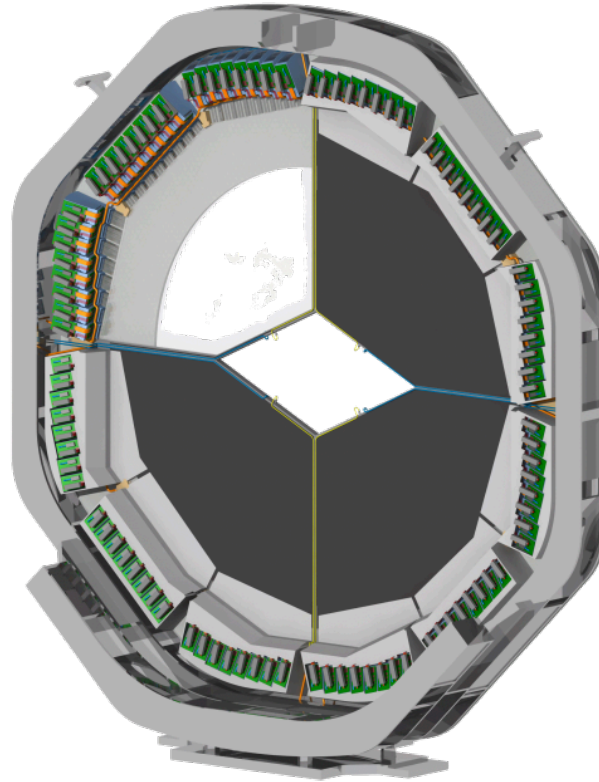


Endcap Disc DIRC Frontend Electronics



Simon Bodenschatz, Lisa Brück, Michael Düren, Avetik Hayrapetyan, Jan Hofmann, Sophie

Kegel, İlknur Köseoğlu-Sari, Jhonatan Pereira de Lira, Mustafa Schmidt, Marc Strickert

PANDA Collaboration Meeting 19/3 - 2019/11/05

Existing Design (2018 - 2019)

ToFPET 2 PETsys

Analog signal (MCP-PMT)

Digitized signal (FEM)

FEB_D_v2 (FPGA)

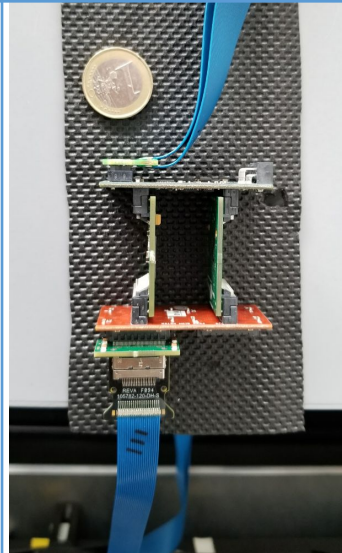
Fan-out box

DAQ board

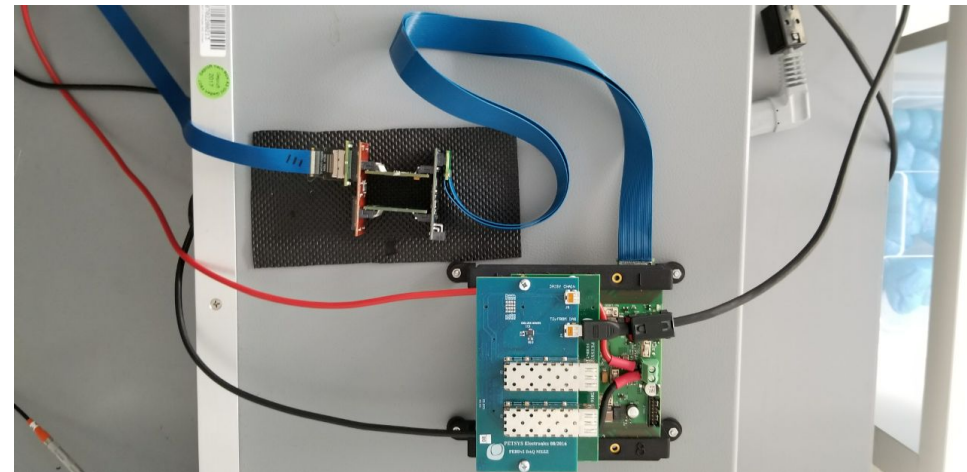
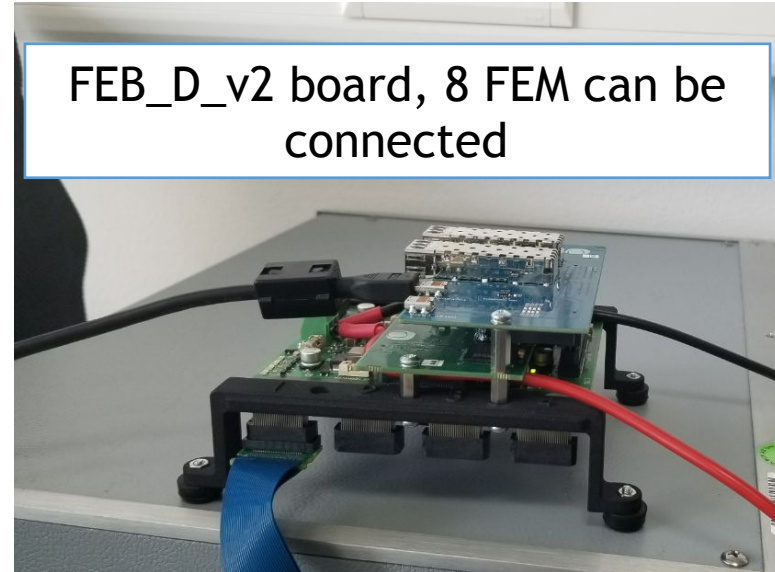
System clock (200MHz)
Synchronization signals

Max data rate 250
Mevents/s

FEM with 2
ASICs, 128 ch



FEB_D_v2 board, 8 FEM can be connected

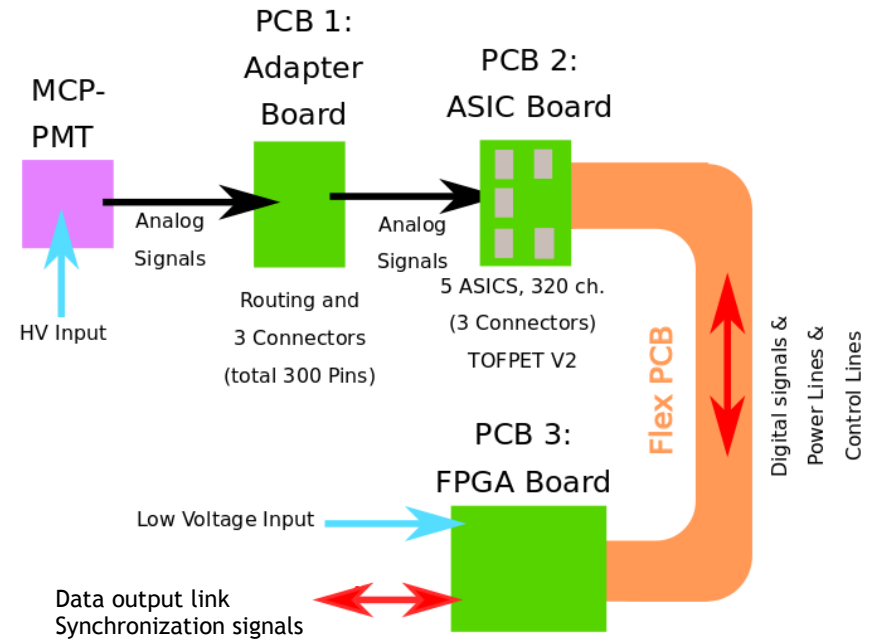
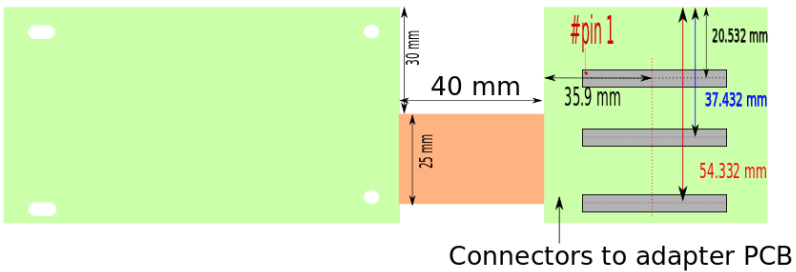
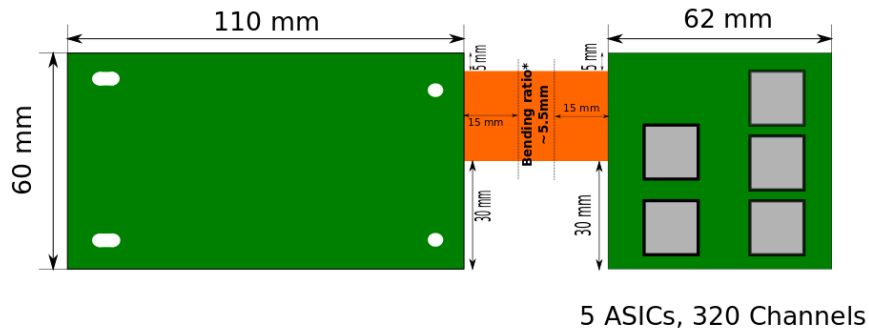


Test beam 2018

✗ Negative polarity

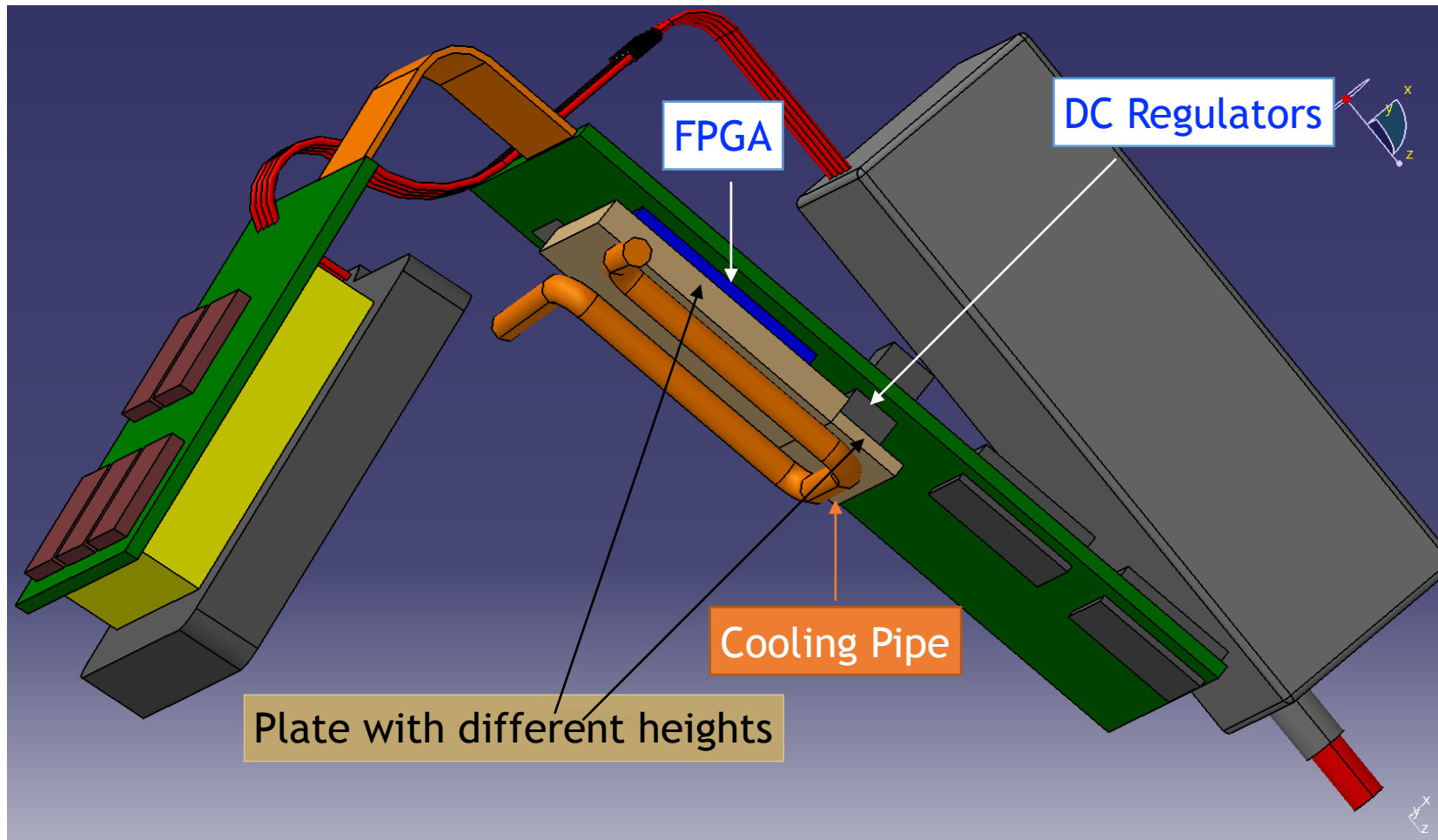
✓ Positive polarity

Design for Prototype & Phase 1

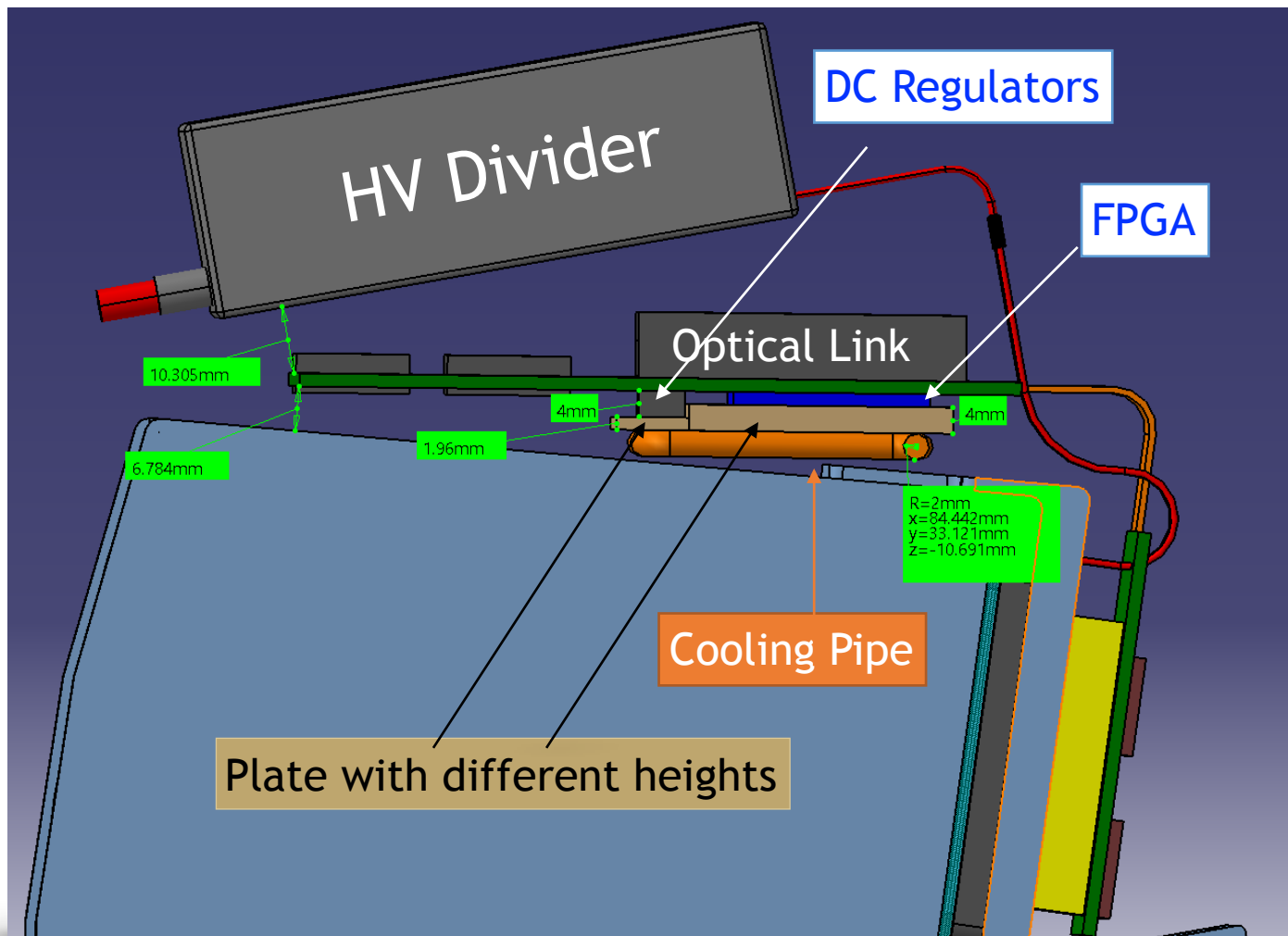


- Design will be done by PETsys company.
- ☑ ASICs are going to be compatible both negative and positive polarity.
- ☑ New ASICs and 2 FE-Board will be delivered in few months.
- uHDMI - HDMI cable will be used.
- For phase 1, uHDMI cable might be changed to optical (versatile) link.

Design for Prototype & Phase 1

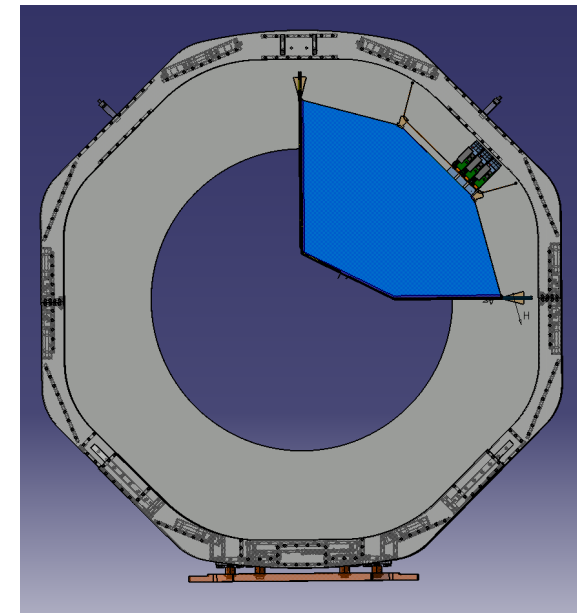
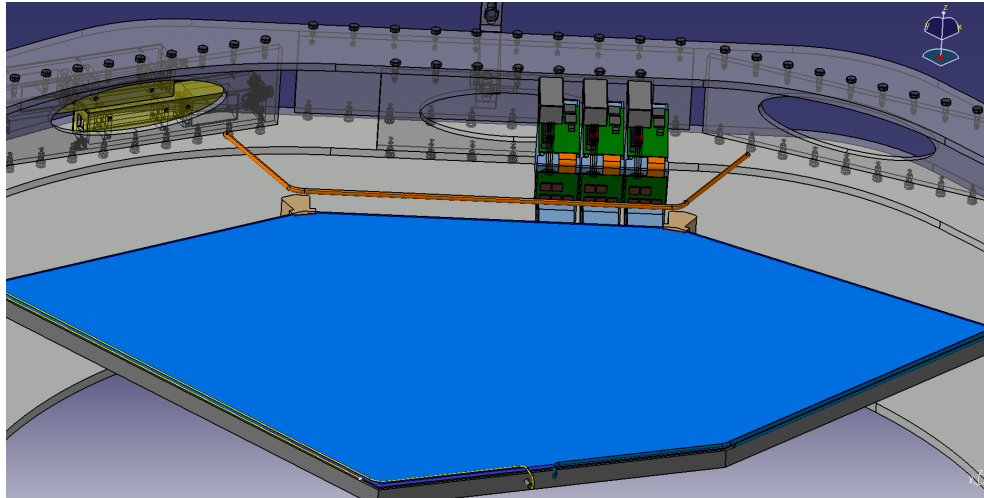
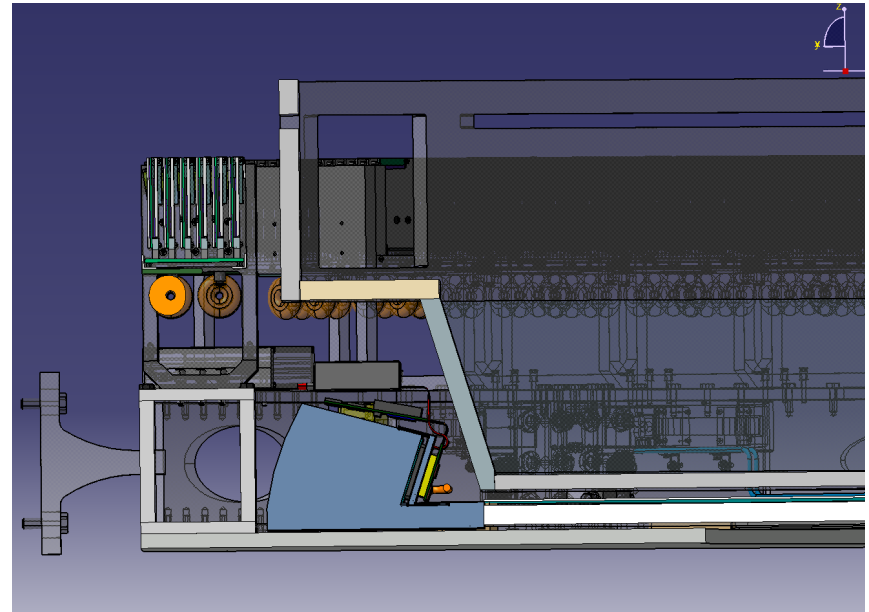


Design for Prototype & Phase 1

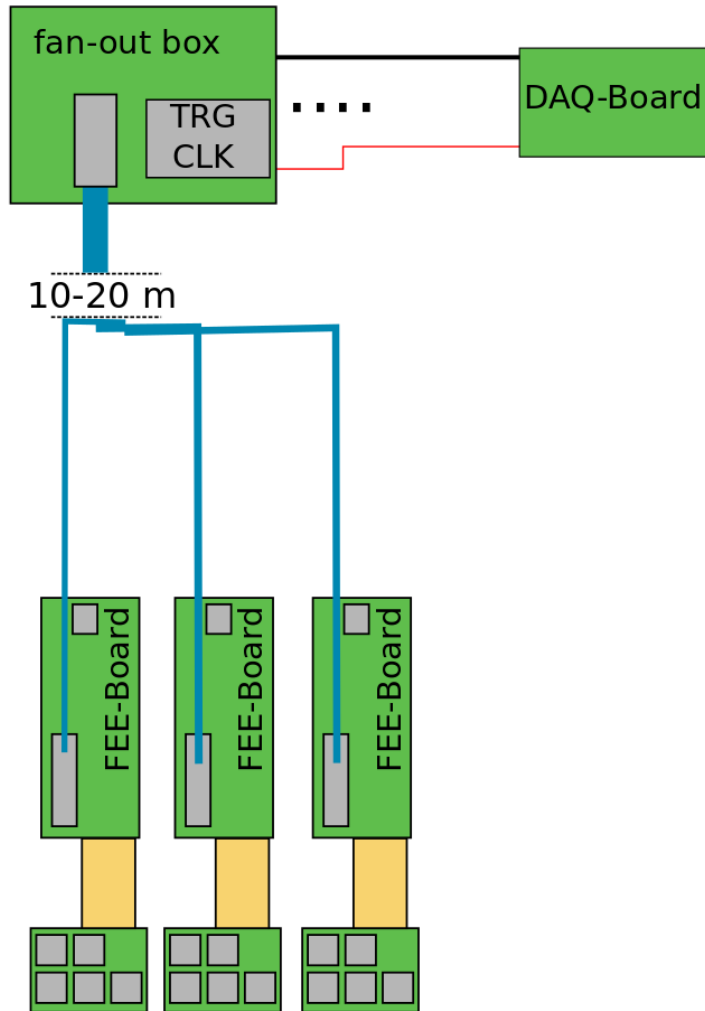


Design for Prototype & Phase 1

- ➔ We need additional funding for a more complete setup during Phase-1.
- Our desire is to have one full quadrant for Phase-1
 - 24 ROMs, 24 MCP-PMTs
 - 72 FEE-board
- We can install our prototype for phase 1 with 3 ROMs if we will not have an additional funding.



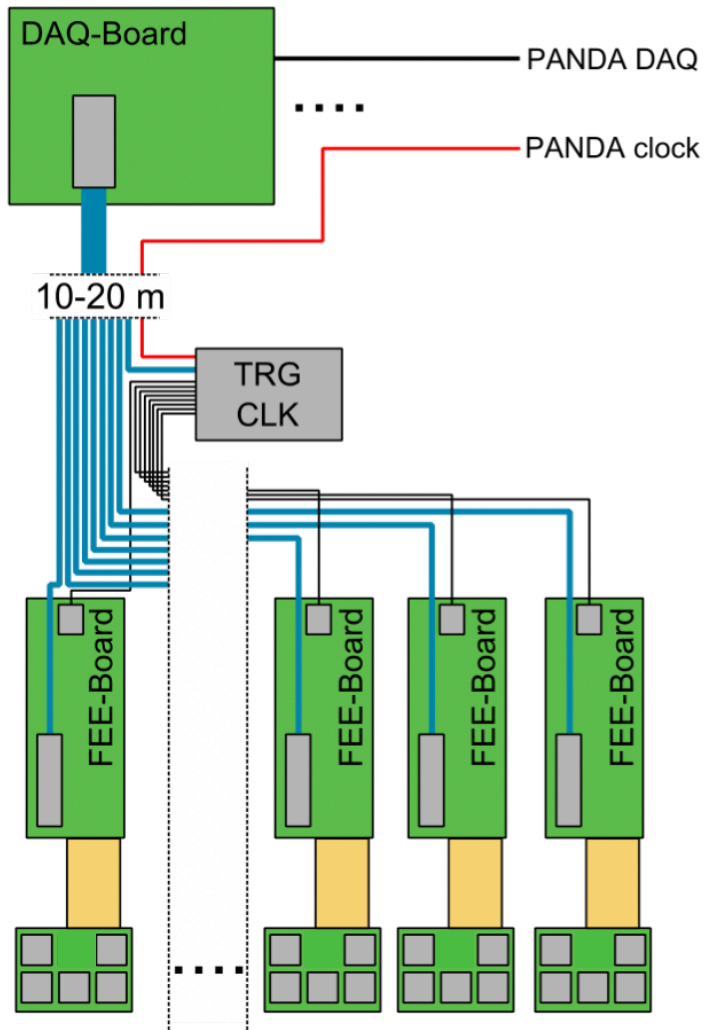
Design for Prototype & Phase 1



- 3 ROMs, 3 MCP-PMT
 - 1 DAQ-Board for Prototype & Phase 1
- Data will send via uHDMI cable to fan-out box (8 connections)
- Clock & Synchronization will be provided by DAQ-Board

Design for Phase 2

12 DAQ-Boards in total



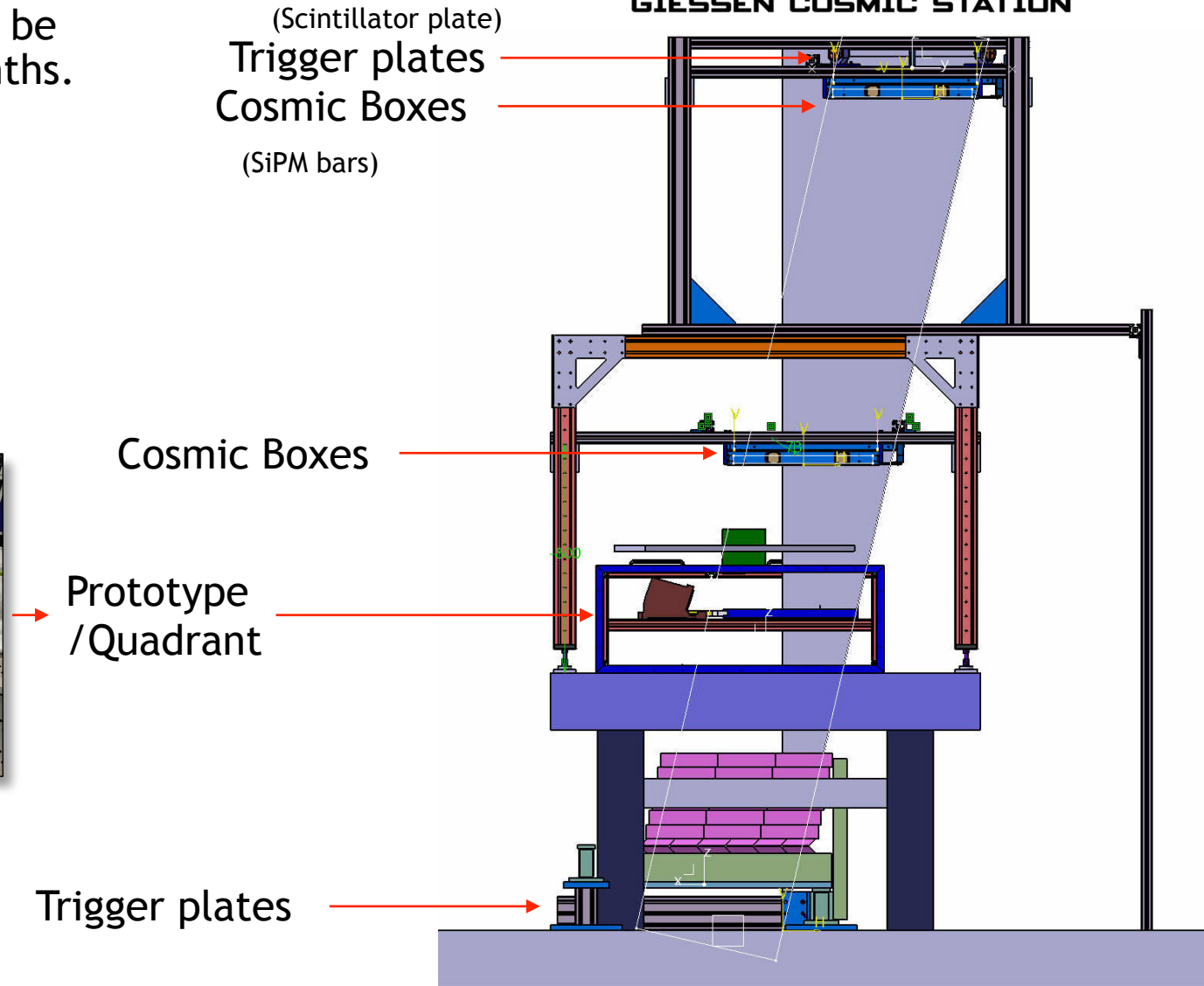
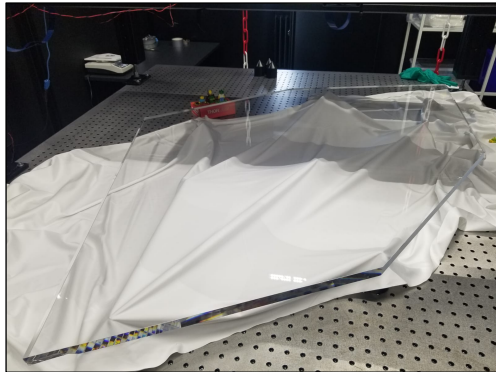
- Depending on the results from Phase-1, FEE design can be changed.
- ASICs board can be combined by DAQ-group design according to their suggestions.

Requirements:

- at maximum 100 kHz per channel
 - converts to 30 MHz per ROM
 - FEB/D allows up to 10^8 events/s
 - ✓ DAQ-Board allows up to $2.5 \cdot 10^8$ events/s
 - 8 ROMs per DAQ-Board
 - 3 DAQ-Boards per Quadrant
 - 12 DAQ-Boards in total
- (96 FEE-Boards)

- New 2 FE-Boards will be delivered in few months.
- Tests will be done in GCS.

Radiator plate in full size



- Thanks for your attention!