Faul Tolerant Local and Monitoring Control Board
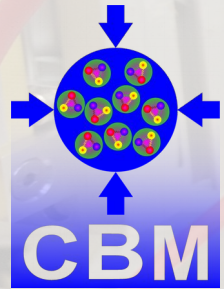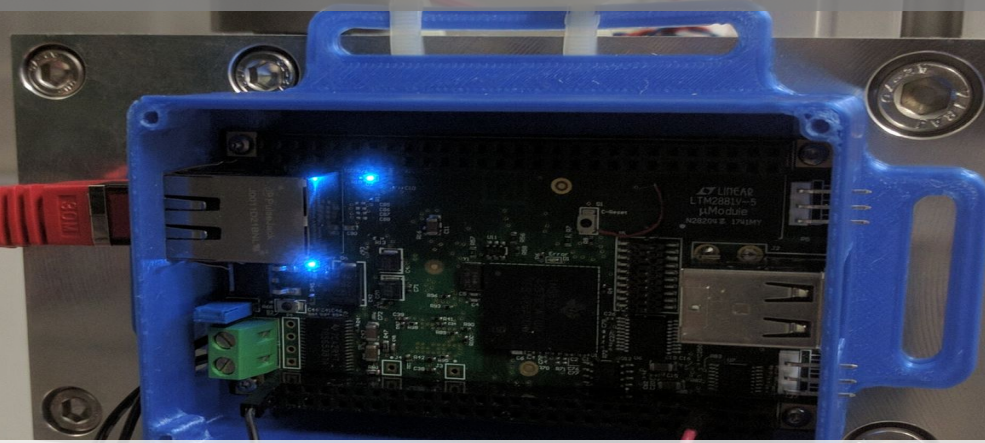
Research group Prof. Udo Kebschull
José Antonio Lucio Martínez

Infrastructure and Computer Systems in Data Processing
Goethe Universität Frankfurt

CBM

IRI

Status of the hardware

- FTLMC V1 is operational
  - I2C
  - Ethernet
  - GPIOs
  - RS-232
- FTLMV V1 Traces errors
  - CAN (Still usable)
  - RS-485 (Still usable)
- Traces errors corrected in FTLMC V2

Status of the hardware

	FTLMC V1			FTLMC V2		
Manufacturer	Name	Job	Result	Name	Job	Result
	Contag	PCB & assembly	Good	SAFA2000	PCB	untested
				Berentzen	assembly	
Design errors	CAN and RS485 traces error			Not found yet		
Status	3 boards operating			18 pcb's, not assembled yet		

PCB Tool chain

- FTLMC Layout was made with a Student licensed Altium

- Schematics/PCB review in any computer with Altium license

- The farbication (gerber & pick and place) files

  - can be reviewed in any computer

  - normally used by manufacturer

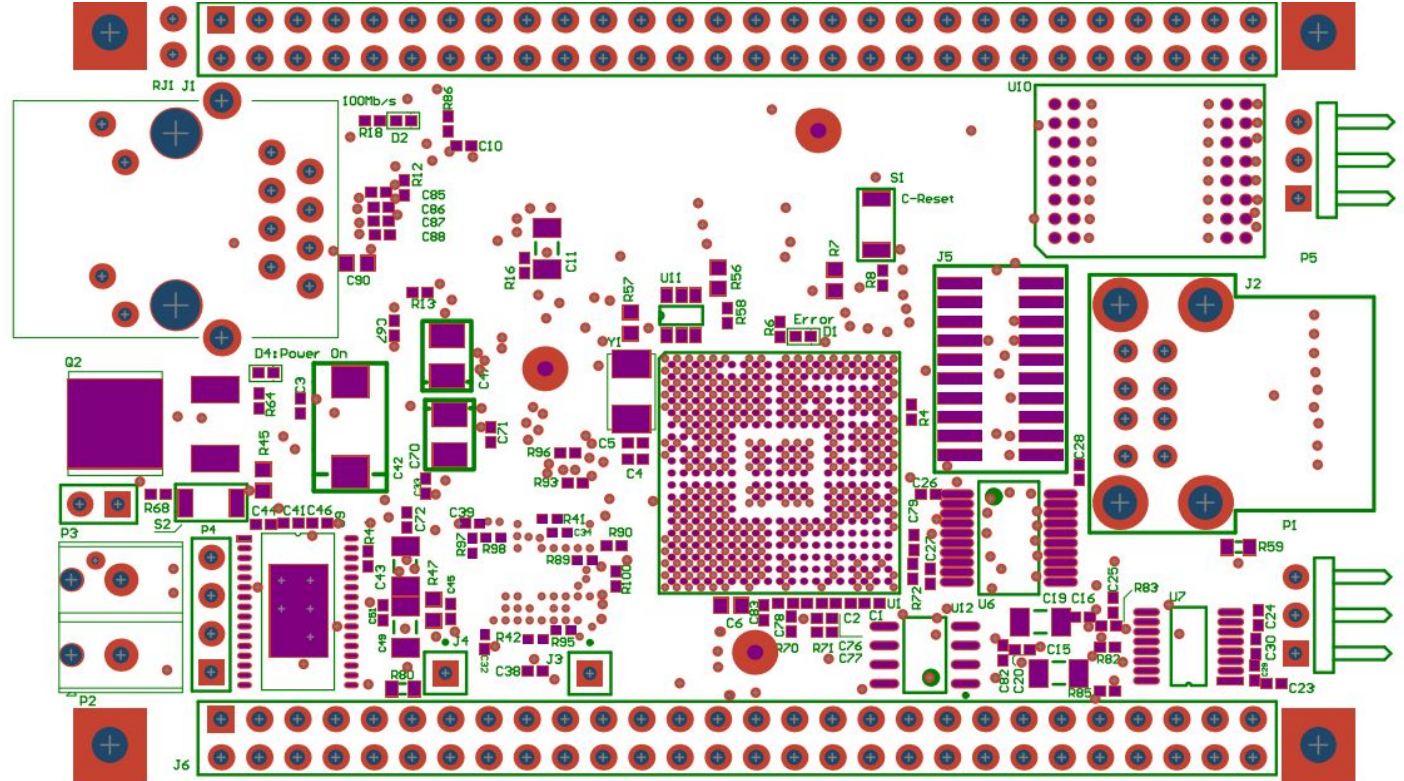- Modifications have to be done in schematics and PCB layout Altium

PCB Tool chain

- 11 schematics sheets
  - Power Supply
  - PC104
  - Jtag &RS485
  - 4 x TMS570
  - 2 x Ethernet
  - CAN + RS232
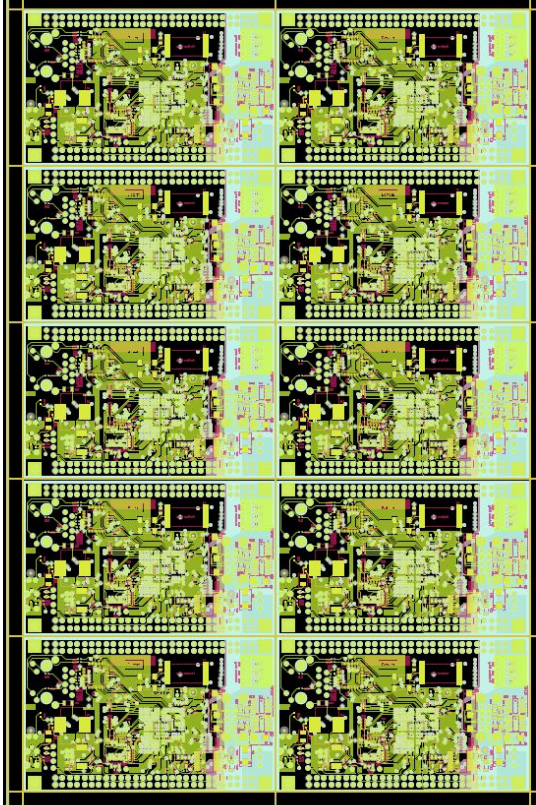 - SDRAM
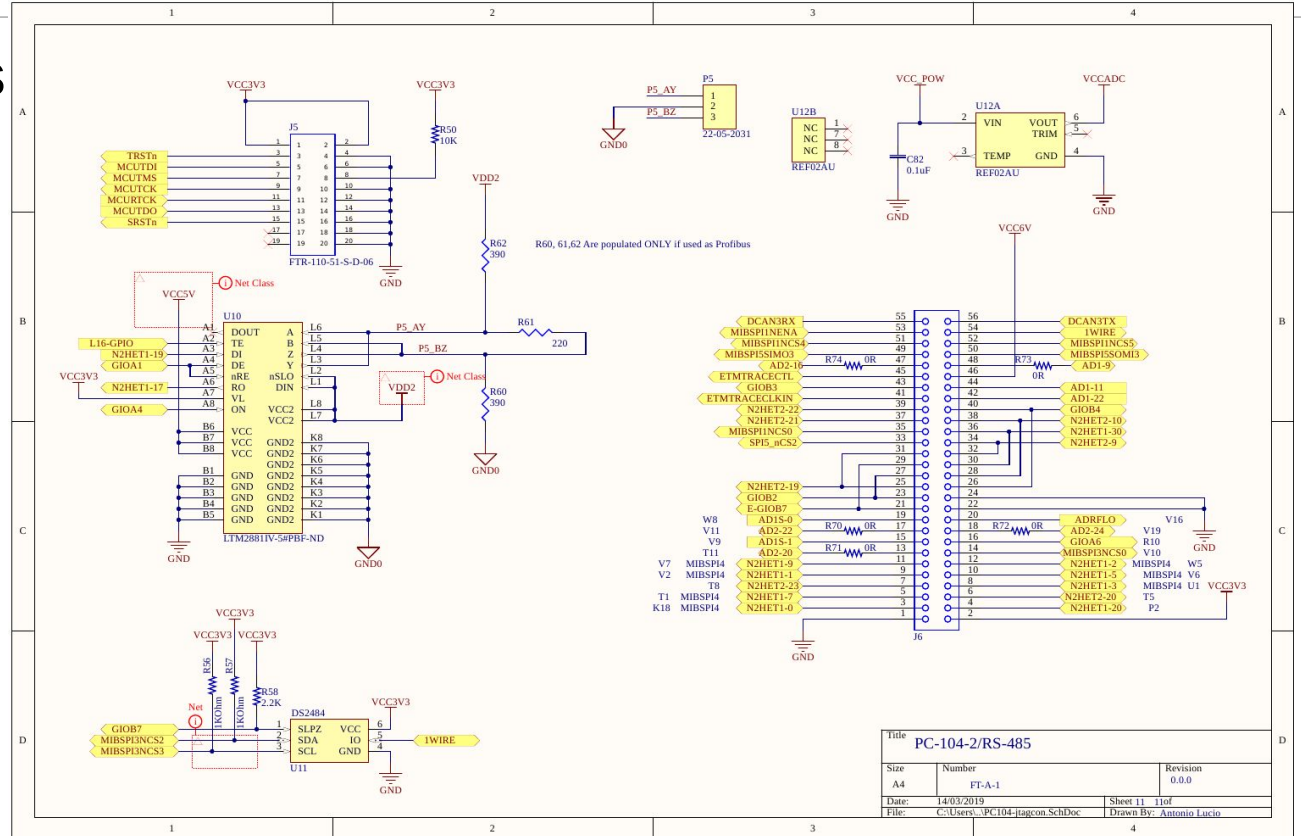
PCB Tool chain

- Defines board
  - Layers
  - Shape
  - Size
  - Traces
  - Electric rules
- Fabr. Data:
  - Pick place
  - Gerber
  - Drill

PCB Toolchain

- Made with Altium
  - Panel made from design with Altium layout tool
  - Grooved lines for easy split after assembly
  - 2 x 5 For better stability in assembly
  - Needed if assembly is made separately (not CONTAG)
- Manufacturer needs
  - Layer stack: dielectric and layer thickness (PCB)
  - Panel gerber files (PCB)
  - Pick and place for such panel (assembler)

Top Layer	35μm
Dielectric	100μm
Signal Layer 1	35μm
Dielectric	100μm
Power Plane 3V3	35μm
Dielectric	100μm
Signal Layer 2	35μm
Dielectric	100μm
Signal Layer 3	35μm
Dielectric	100μm
Signal Layer 4	35μm
Dielectric	100μm
Power Plane 1V2	35μm
Dielectric	100μm
Signal Layer 5	35μm
Dielectric	100μm
Ground Plane GND	35μm
Dielectric	100μm
Bottom Layer	35μm

Abmessungen/Dimensions	88,59x54,34	
Lagen/Layer count	10	
Material	FR4	
Kupfer/Copper	35μm Cu	
Oberfläche / Surface	HAL leadfree	-----
Lötstopplack / Solder Mask	top + Bottom	green
Bestückungsdruck / Silkscreen	top + Bottom	white
Zusatzdrucke / Additional Prints	no	
Via Technology	Standard (PTH)	
Kantenmetallisierung / Edge metalization	no	
Nutzen (Panel)		
Abmessungen/Dimensions	187,57x282,55	
Menge/Quantity	10	
Anordnung/Orientation	2x5	
Nutzenrand/Panel Frame	gerber files include panel drawing	
Nutzentrennung/Panel Separation	V-Cut	

Status of RTEMS

- Cross compiler building tools
  https://github.com/RTEMS/rtems-source-builder
- Board Support Package (BSP) Code that is Board dependent
  - RTEMS official repository supports TMS570 Development kit
  - Changes made for FTLMC
    - Ethernet driver RMII @ 50Mhz instead of MII @ 25Mhz
    - Cortex-R5F instead of Cortex-R4F
   - Larger external memory

Status of RTEMS

- FTLMC BSP's changes implemented with pre-processing directives

```
#ifdef TMS570_LC43X
 #define TMS570_I2C1 (*(volatile tms570_i2c_t*)0xFFF7D400)
 #define TMS570_I2C2 (*(volatile tms570_i2c_t*)0xFFF7D500)
 #define TMS570_IOMM (*(volatile tms570_iomm_t*)0XFFFF1C00)
 #define TMS570_PINMUXOt (*(volatile tms570_pinmux_t*)0xFFFF1D10)
 #define TMS570_PINUMXSp (*(volatile tms570_pinmux_20_t*)0xFFFF1F90)
 #define TMS570_PINUMXIn (*(volatile tms570_pinmux_20_t*)0xFFFF1E50)
#else
 #define TMS570_I2C (*(volatile tms570_i2c_t*)0xFFF7D400)
 #define TMS570_IOMM (*(volatile tms570_iomm_t*)0XFFFFEA00)
#endif
```

- OpenOCD (modified for FTLMC) Open Source debugging tool

Status of RTEMS

- Code loaded with blackhawk emulator
    - Used until now for jtag debugging
    - Additional standalone solution needed
- Options for standalone bootloading (BL)
    - Flash with embedded epics binary (done)
    - Ethernet BL, works for binaries < 300kb (to be adapted for EPICS)
    - SPI BL (to be done)
    - CAN BL (to be done)
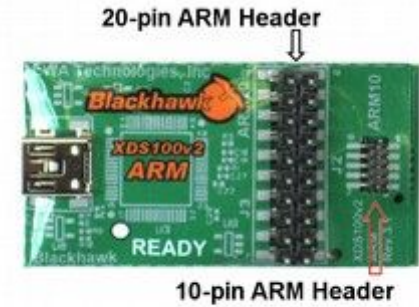
Status of RTEMS

- Tested on External SDRAM execution
- Internal non-volatile memory execution → to be done
- Only BSP code changed, RTEMS mainline remains as is
- FTLMC BSP available in git repository

  – Ethernet driver is working

  – I2c driver working

  – Pending: CAN-Bus and SPI

- BSD compiled separately in RTEMS 5 => drivers have to be ported

Status of EPICS

- EPICS only supports RTEMS <= 4.10

- Changes to API code needed for 4.11 compatibility

```
base/src/libCom/osi/os/RTEMS/osdEvent.c
base/src/libCom/osi/os/RTEMS/osdMessageQueue.c
base/src/libCom/osi/os/RTEMS/osdMutex.c
base/src/libCom/osi/os/RTEMS/osdPoolStatus.c
base/src/libCom/osi/os/RTEMS/osdSock.h
base/src/libCom/osi/os/RTEMS/osdSpin.c
base/src/libCom/osi/os/RTEMS/osdThread.c
base/src/libCom/osi/os/RTEMS/osdTime.cpp
```

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EPICS adaption example

```
RTEMS 4.10
(epicsThreadId)semaphore.Core_control.mutex.holder_id
```
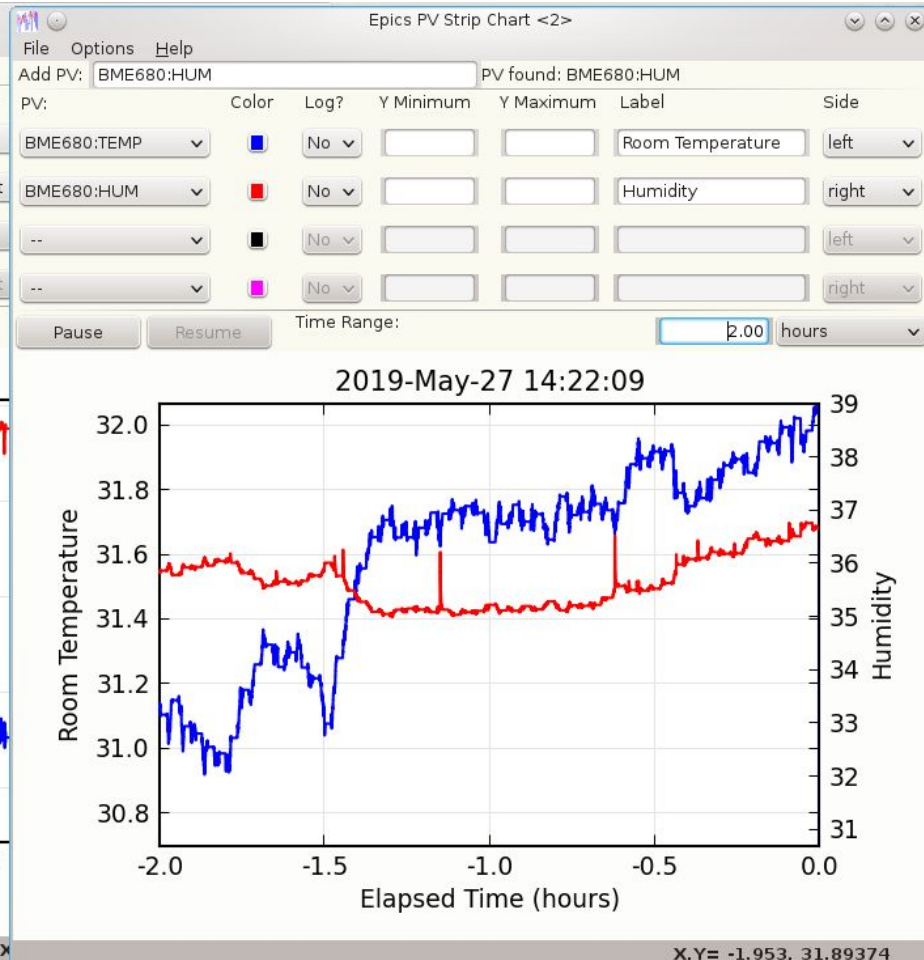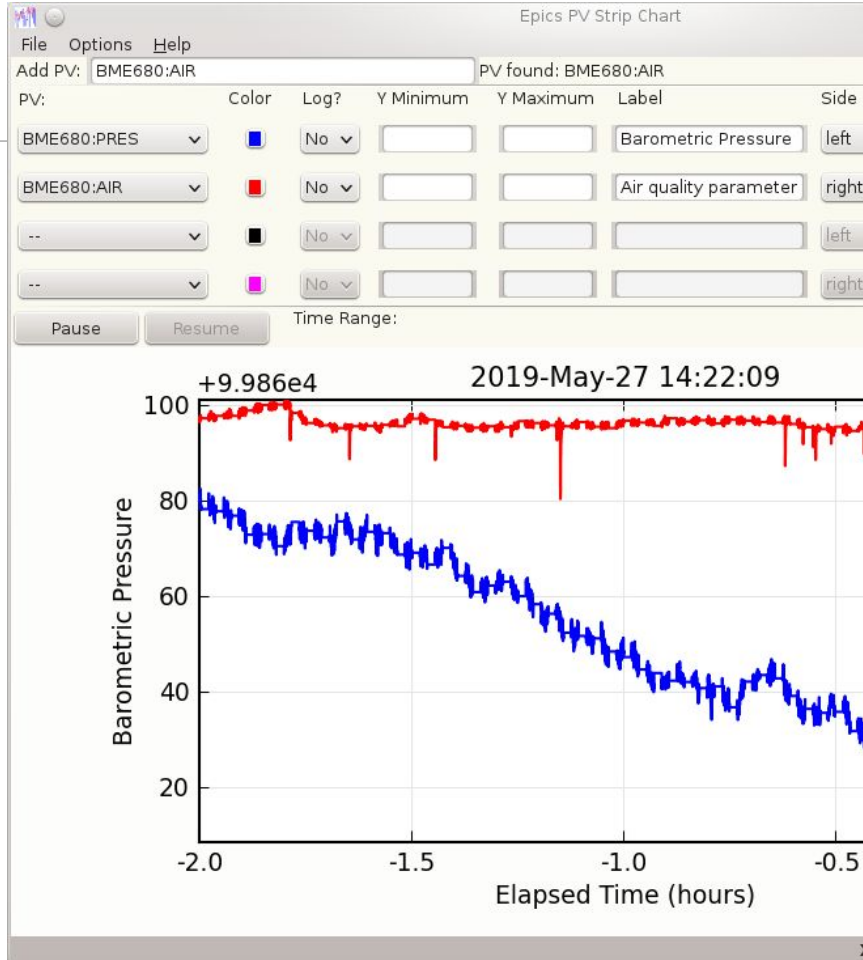
```
RTEMS 4.11
(epicsThreadId)holder->Object.id
```

```
RTEMS 4.10
_Thread_Executing->Wait.return_code == 0
```

```
RTEMS 4.11
executing = _Thread_Get_executing();
executing->Wait.return_code == 0
```

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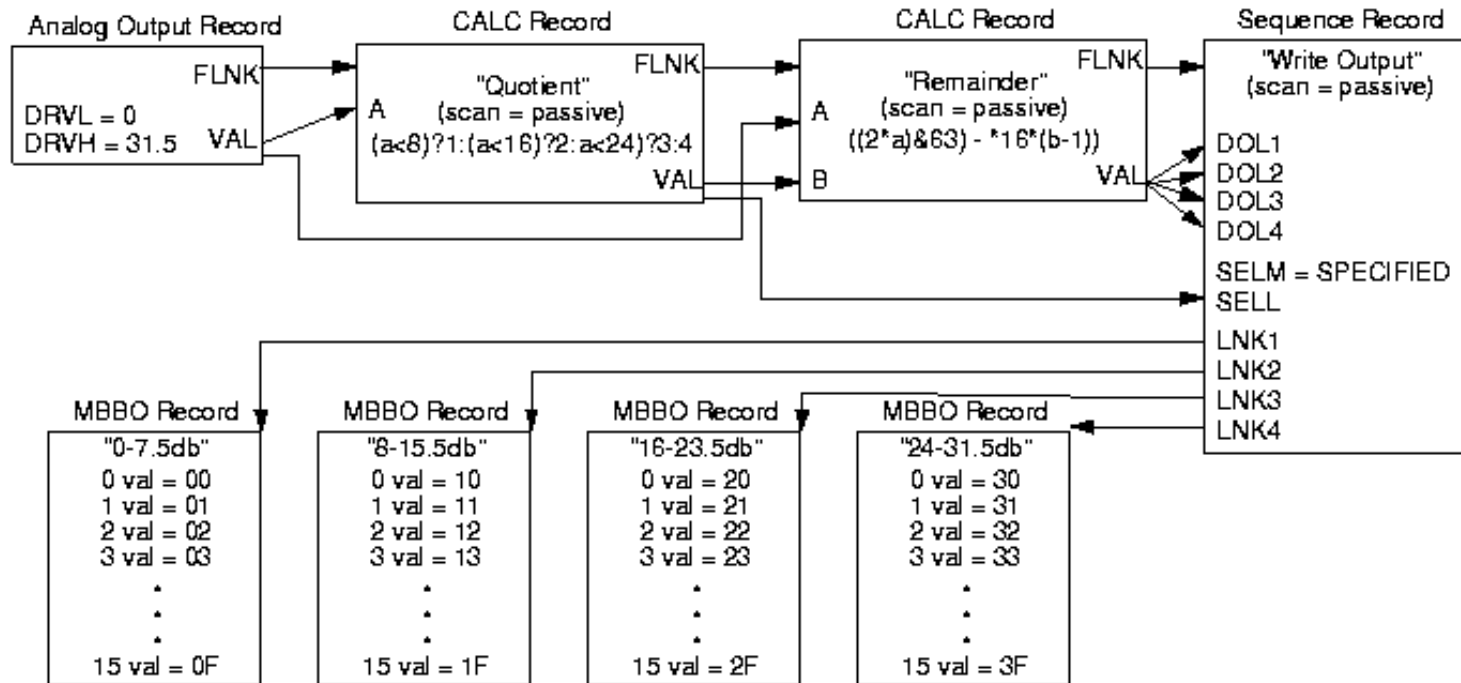# FTLMC V1

Galvanic isolated UART RS-485

Galvanic isolated 2 x CANBUS

1Mb/s UART → RS-232

I^2C, SPI, 7 ADC Inputs, 85 GPIO's

Ethernet capability
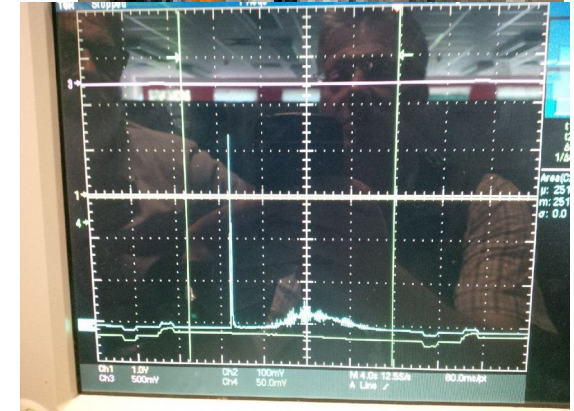
EPICS database example

Support for a 6 bit programmable attenuator from an AO record. No custom device support required.

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Radiation tolerance studies

- Only the MCU has been tested in beam

- Only SEU's were considered for FTLMC

- Strong magnetic field was not considered for FTLMC V1 and V2

  - A working board was priority

  - Solution tests need to be done beforehand

  - Footprints are included for air-core coils in FTLMC V1-2

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Beam test of the Cortex-R (TI-TMS570)

- Exposed MCU directly to beam during: 13 hours
- Beam: 2Gev Protons
  - In spike: 7×10^7
  - in normal extraction: 2×10^8
  - spill: 20s
  - Pause: 10s
- Total detected and corrected SEU's:
  - in Bank A: 718
  - In Bank B: 686
- No unrecoverable errors
- Failure registers continuously monitored
- Database with error time-stamp
- No errors during beam off times detected

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Thank you!