Synchronization of MuPix and Front-End Board for the Luminosity Detector

PANDA Collaboration Meeting 19/2

Florian Feldbauer

Ruhr-Universität Bochum - Experimentalphysik I AG

Front-End Boards

- MuPix read out via LVDS
- External reference clock defines data rate
- Data is 8b/10b encoded

$\Rightarrow$ Clock embedded in data stream

$\Rightarrow$ Clock and Data Recovery (CDR) on FPGA necessary

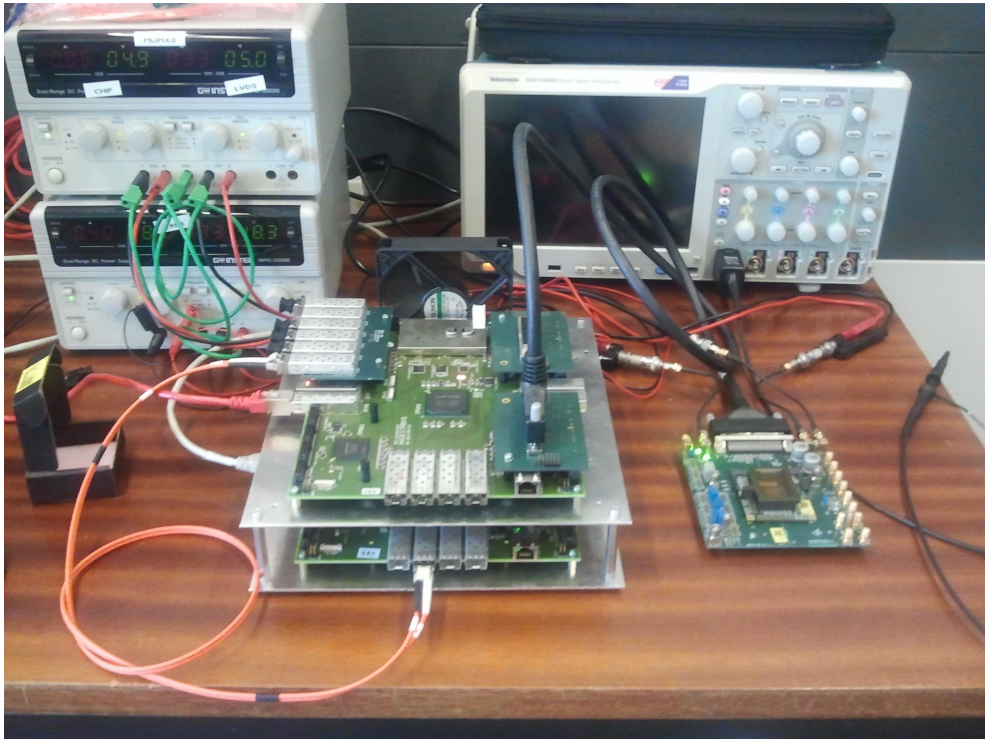
- No final solution for front-end boards

Front-End Board: Option 1

- Currently using TRBv3
- Lattice ECP3M
- One Mupix per Side FPGA (SERDES link)

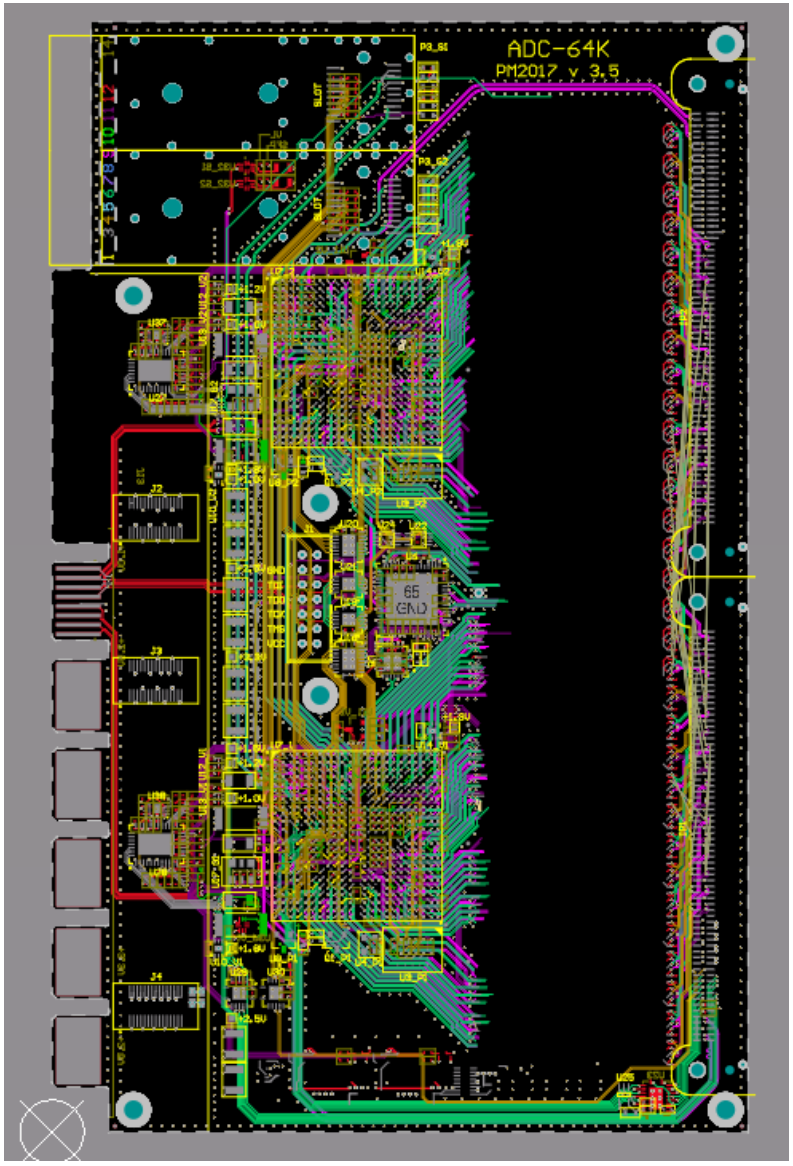
$\Rightarrow$ 80 TRBs needed

- Too slow for Full Luminosity Mode(?)



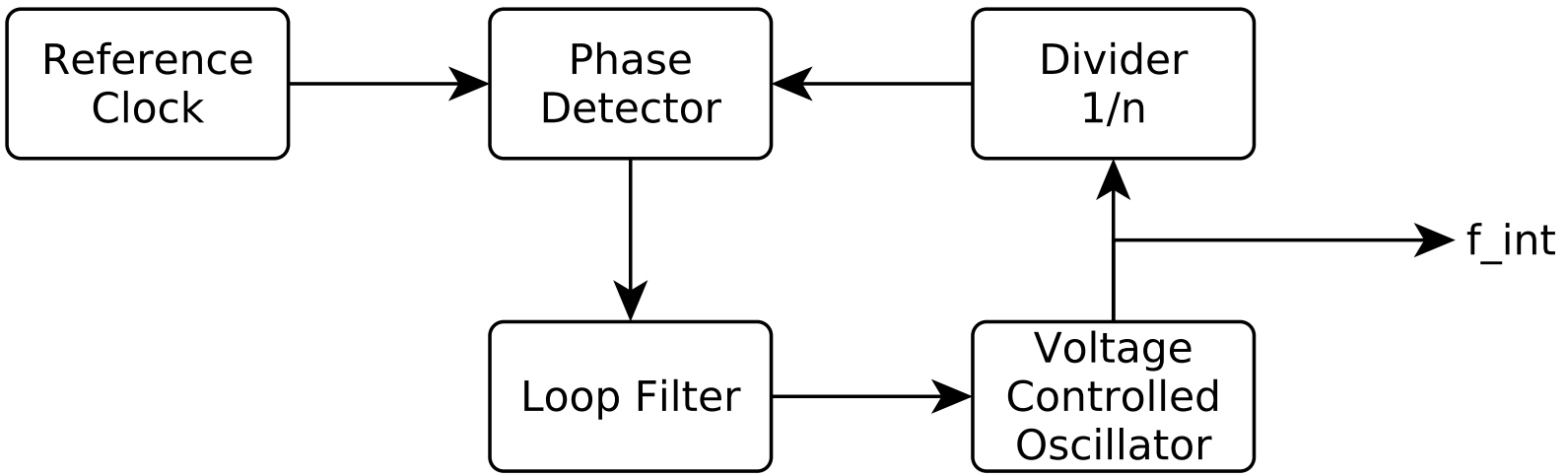
Front-End Board: Option 2

- Readout Board from Pawel Marciniewski
- Based on EMC digitizer
- Two Xilinx Kintex7 fpgas
- SODAnet support
- $\sim$ 108 LVDS links (no SERDES)
- Need to implement Clock and Data Recovery (CDR)



Timing of MuPix

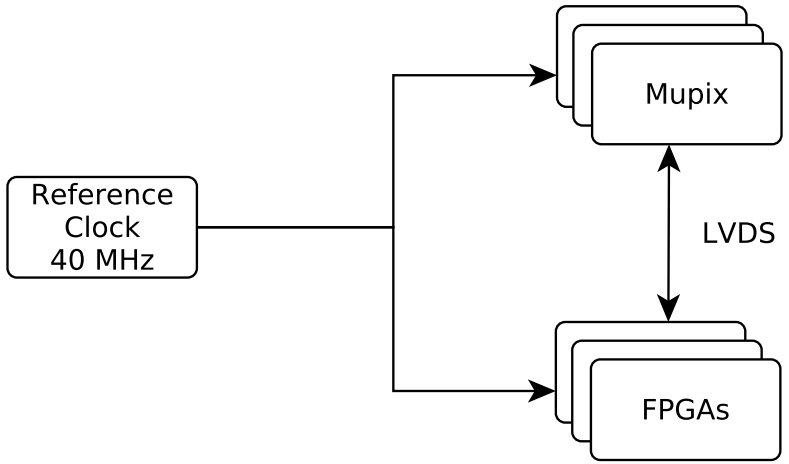
- MuPix get's external reference clock ($f_{ref} = 40\,\text{MHz}$)
- Internal Clock synthesized from ref clock ($n = 5$)



- Serializer pushes data at both flanks of internal clock

$\Rightarrow$ Data rate is 10 times higher than reference clock ($400\,\text{Mbit}\,\text{s}^{-1}$)

Idea for Synchronization



- Use a central 40 MHz crystal oscillator as reference clock for all FPGAs and MuPix
- FPGAs use same mechanism to synchronize internal clock for CDR ($n = 10$, $f_{int} = 400\,\text{MHz}$)
- Need to keep signal path for clock distribution equal for all end devices

Backup

Data Concentrator

Use EMC Data Concentrator (Pawel Marciniewski)