ToASt readout ASIC status

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Strip detector readout status

- Readout architecture partially based on a previous design (TOFPET) has been proposed (PASTA)
  - 64channel readout ASIC
  - TDC-based ToT measurement with 50 ps time bin
  - Technology : CMOS 0.11 μm
  - Received on Sep 2015
- Results were not satisfying - analog front-end looks ok but
  - 31% working channels at 160 MHz
  - 88% working channels at 80 MHz
- *Redesign of the chip required*

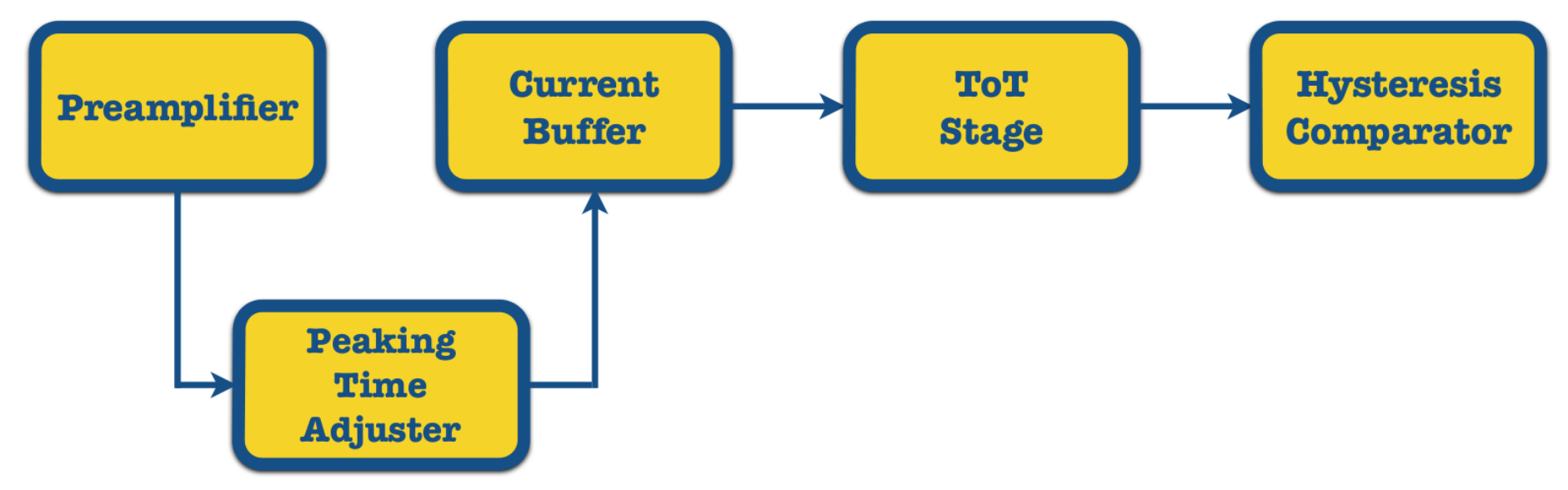
ToASt development background

- Developed for the PANDA MVD strip detector readout
- Possible use in COMPASS under investigation
- Analogue front-end from the PASTA ASIC
- Digital back-end derived from the ToPiX ASIC
- Technology : CMOS 0.11 μm

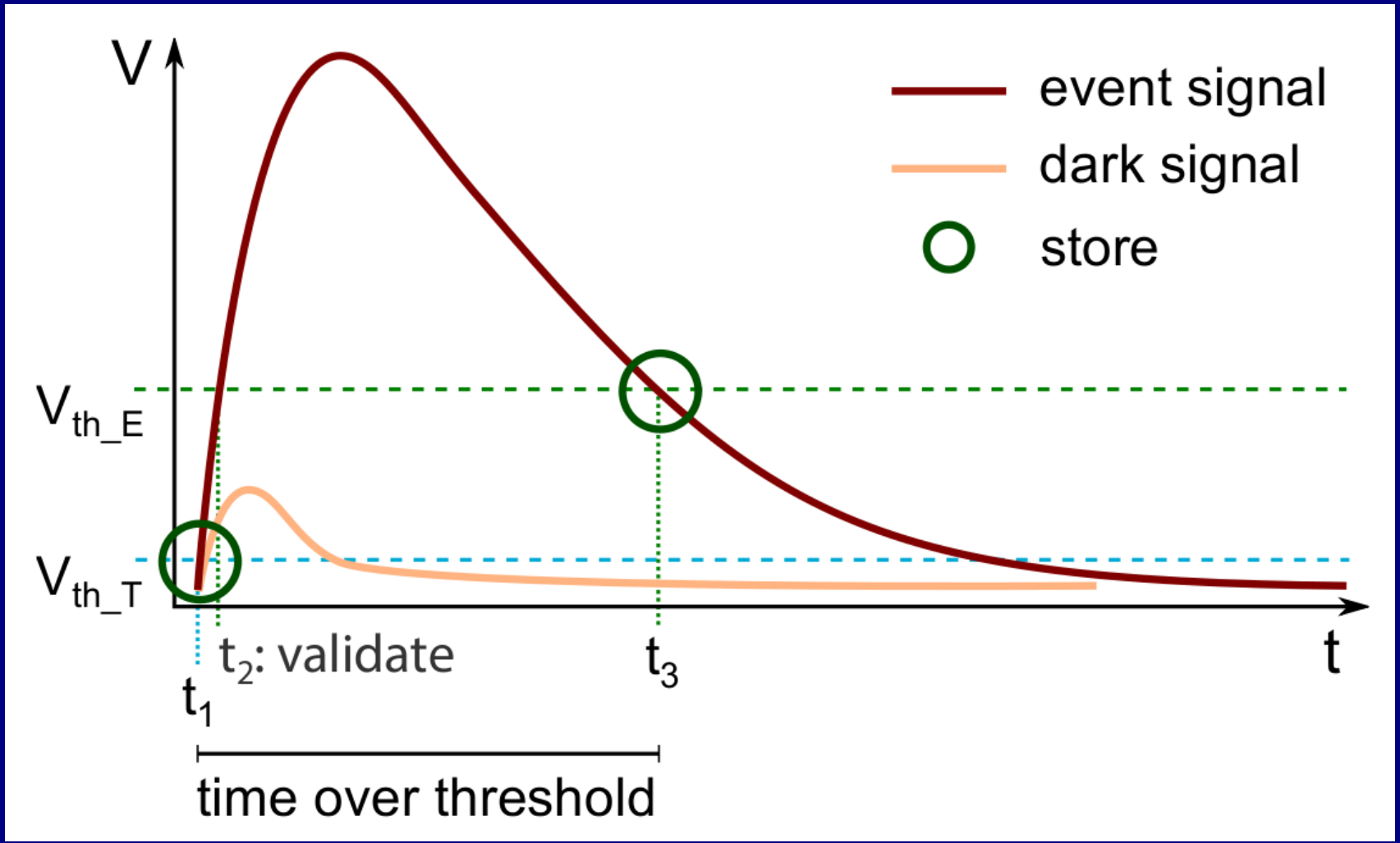
Specifications

Specification	Min	Max	Unit
Input capacitance	2	17	pF
Max rate per strip		40	kHz
Input charge	1	40	fC
Noise		1500	e^-
Preamp peaking time	50	100 (?)	ns
Channels per chip	64		
Reference clock		160	MHz
Charge resolution	8		bits
Time resolution (pk-pk)		6.25	ns
Time resolution (r.m.s.)		1.8	ns
Power consumption		256	mW
Chip dimensions	4.2×3.5		mm^2
Pads position	On two sides only		

ToASt analog FE



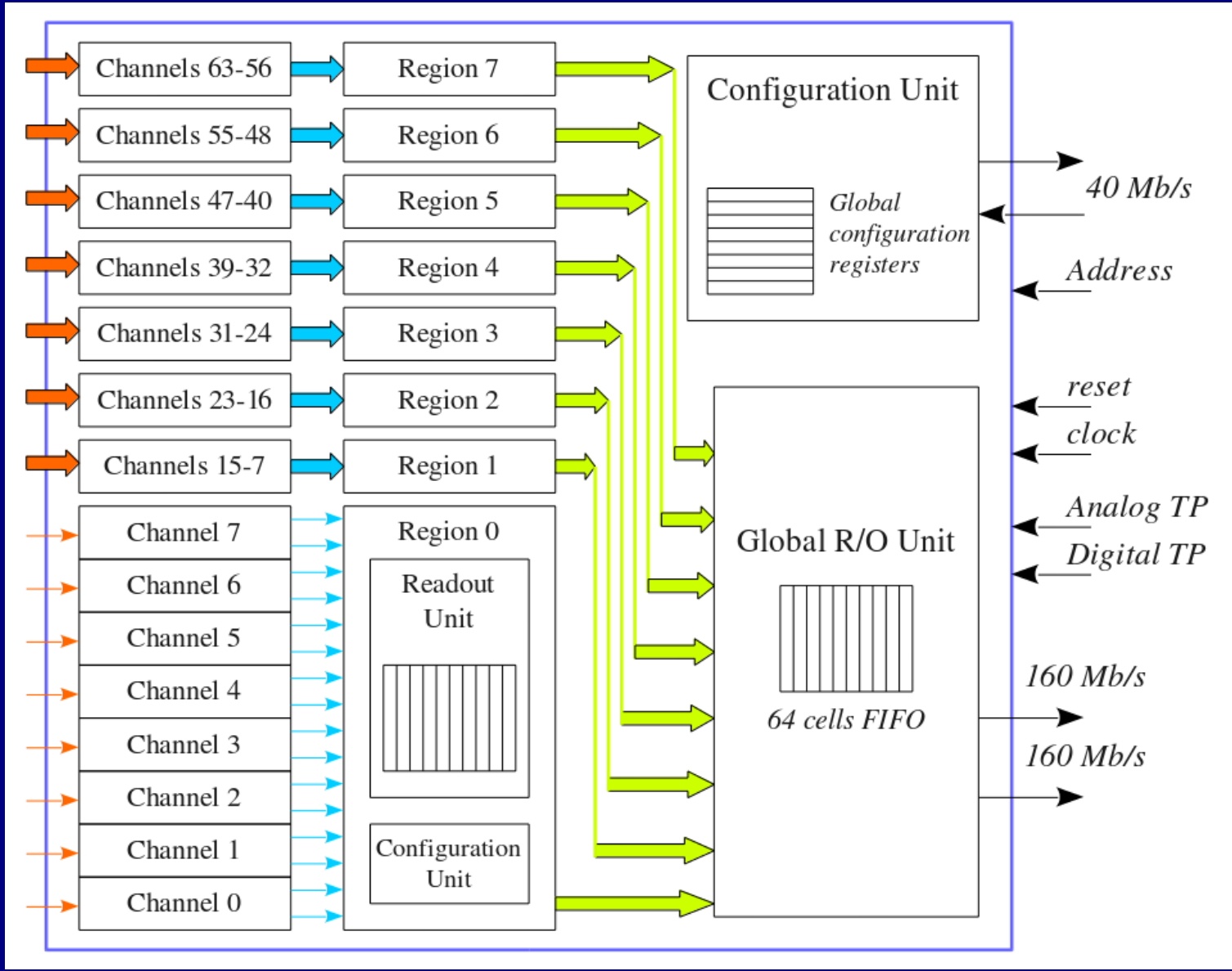
Double threshold logic



ToASt main characteristics

- 64 input channel channels
- Time of Arrival (ToA) and Time over Threshold (ToT) measurements
- Master clock frequency : 160 MHz
- Region : groups of 8 channels with local FIFO
- Second level FIFO buffering for the 8 regions
- Two output serial links at 160 Mb/s
- Serial configuration protocol at 40 Mb/s
- SEU protection for registers and FSM
- CMOS 0.11 μm technology

ToASt architecture



ToASt preliminary pinout

Pin name	Direction	Description
in[63:0]	In	Analog inputs
SyncReset	Rx	Synchronous reset
ChipAddr[6:0]	In	Chip address
TestPulse	In	Digital test pulse
CfgRx	Rx	Configuration receiver
CfgTx	Tx	Configuration transmitter
TxOut_0	Tx	Data serial output 0
TxOut_1	Tx	Data serial output 1

Channel configuration - *Preliminary*

Register	Bits	Function
0	11:8	*Reserved for future use*
0	7	Channel mask
0	6	Delay enable
0	5	Calibration enable
0	4:0	ToT discharge current calibration DAC
1	11:10	*Reserved for future use*
1	9:5	Energy threshold calibration DAC
1	4:0	Time threshold calibration DAC

WARNING ! This is not the final assignment - Work in progress...

Global configuration - *Preliminary*

Register	Name	Function
GCR0	11	*Reserved for future use*
GCR0	10	detector polarity
GCR0	9	leading edge-only mode
GCR0	8	single threshold mode
GCR0	7:6	*Reserved for future use*
GCR0	5	Tx 1 enable
GCR0	4	Tx 0 enable
GCR0	3:2	*Reserved for future use*
GCR0	1	Time stamp counter Gray mode
GCR0	0	Time stamp counter enable
1	11:8	*Reserved for future use*
1	7:0	Region disable

Global configuration for analogue bias 1/2 - *Preliminary*

Register	Bit	Function
GCR2	11:10	*Not used*
GCR2	9:5	CSA Ibias
GCR2	4:0	CSA source followers Ibias
GCR3	11:10	*Not used*
GCR3	9:5	Preamp feedback pMOS Ibias
GCR3	4:0	Preamp feedback nMOS Ibias
GCR4	11:10	*Not used*
GCR4	9:5	Preamp Ishift
GCR4	4:0	PTA Ibuf
GCR5	11:10	*Not used*
GCR5	9:5	PTA pMOS Ibias
GCR5	4:0	PTA nMOS Ibias

CSA : Charge Sensitive Amplifier
PTA : Peak Time Adjuster

Global configuration for analogue bias 2/2 - *Preliminary*

Register	Bit	Function
GCR6	11:10	*Not used*
GCR6	9:5	CB Ibias 1
GCR6	4:0	CB Ibias 2
GCR7	11:10	*Not used*
GCR7	9:5	CB Vcas
GCR7	4:0	ToT Ibias
GCR8	11:10	*Not used*
GCR8	9:5	BLR Ibias
GCR8	4:0	BLR Vcas
GCR9	11:10	*Not used*
GCR9	9:5	HC Ibias 1
GCR9	4:0	HC Ibias 2

CB : Current Buffer
BLR : BaseLine Restorer
HC : Hysteresis Comparator

Simulation files - Barrel, sensor 190

Chip #	0	1	2	3	4	5	6	7	8
# of events	343	361	313	242	341	373	6	0	0
Events above 40 fC	20	26	6	0	24	12	0	0	0
Avg charge [fC]	13.26	20.44	9.30	10.10	14.89	15.09	7.10	0	0
Max charge [fC]	149.93	343.46	138.15	38.04	14.89	15.09	11.49	0	0
Avg ToT [ns]	530.6	817.6	372.1	404.0	595.5	603.5	283.8	0	0
Max ToT [μs]	6.0	13.7	5.5	1.5	13.4	13.7	0.5	0	0
Rate per channel [kHz]	4.33	4.56	3.95	3.06	4.31	4.71	0.08	0	0

- 128 channel per chip are assumed
- No events on chips 7,8 (barrel), 8 (forward)
- Rate $<$5 kHz (maximum expected is 40 kHz)
- Max charge above 300 fC (i.e. ToT $>$ 12 μs w/o clipping)
- Most hits are on more than one strip

Note : ToT Gain 40 ns/fC in the simulations (to have 1.6 μs at 40 fC)

Simulation files - Barrel, sensor 190

Chip n.	Channel range	Input events	Output events	Lost events	Synch words
0	0-63	208	206	2	4200
0	64-127	135	133	2	4335
1	0-63	192	192	0	4126
1	64-127	169	165	4	4294
2	0-63	164	164	0	4277
2	64-127	145	149	4	4299
3	0-63	140	133	7	4314
3	64-127	102	102	0	4309
4	0-63	179	179	0	4287
4	64-127	162	162	0	4287
5	0-63	207	196	11	4255
5	64-127	166	165	1	4241
6	0-63	6	6	0	4324
6	64-127	0	0	0	4627

Lost events example : Barrel, sensor 190, chip 0

Channel 9 : $\Delta T = 1$ ns

```
164791 190 4 4 0.000221017
164791 190 4 5 0.000221017
165206 190 0 9 0.000151042
165206 190 0 8 0.000151042
165206 190 5 15 0.000151042
165206 190 5 16 0.000151042
165206 190 5 17 0.000151042
165206 190 5 18 0.000151042
165206 190 5 19 0.000151042
165207 190 0 9 0.000137269
165207 190 0 10 0.000137269
165207 190 5 103 0.000137269
165207 190 5 104 0.000137269
```

Channels 66-67 : $\Delta T = 0$ ns

```
22296.1 190 0 66 0.000253243
22296.1 190 0 67 0.000253243
22296.1 190 5 32 0.000253243
22296.1 190 0 68 0.000253243
22296.1 190 0 69 0.000253243
22296.1 190 0 70 0.000253243
22296.1 190 0 66 7.99529e-06
22296.1 190 0 67 7.99529e-06
22296.1 190 5 31 7.99529e-06
```

Channel 27 : $\Delta T = 0$ ns

```
372854 190 2 87 0.00023847
372854 190 2 88 0.00023847
372854 190 2 89 0.00023847
372854 190 4 3 0.00023847
374957 190 0 27 0.000170951
374957 190 0 29 0.000170951
374957 190 0 30 0.000170951
374957 190 0 31 0.000170951
374957 190 4 2 0.000170951
374957 190 4 3 0.000170951
374957 190 4 4 0.000170951
374957 190 0 27 0.000176699
374957 190 0 23 0.000176699
374957 190 0 24 0.000176699
374957 190 0 25 0.000176699
374957 190 0 26 0.000176699
374957 190 4 81 0.000176699
```

Data loss due to pile-up events

Project status

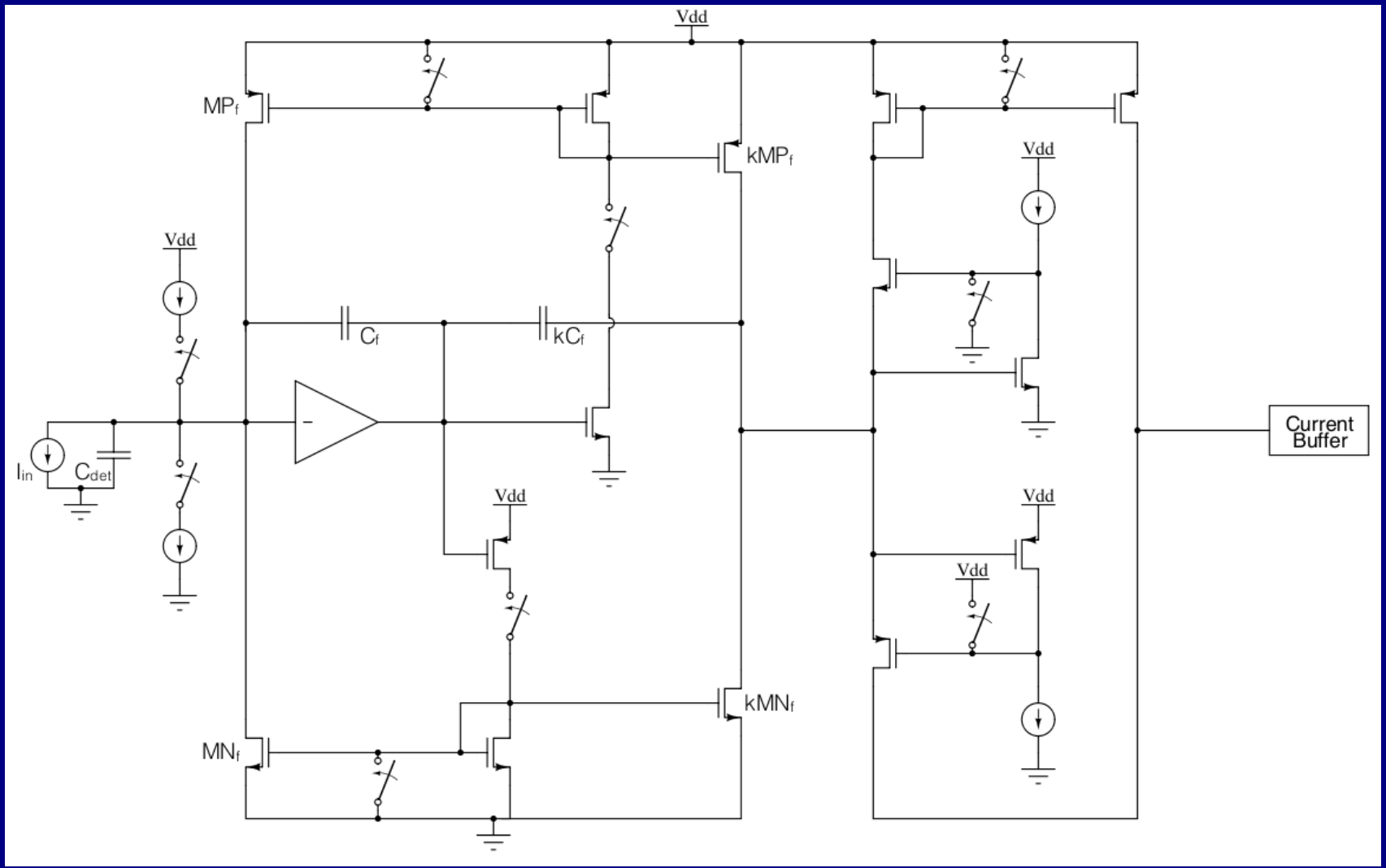
Task	Status
Analogue FE optimization	ongoing
HDL code of the channel logic	done
HDL code of the region logic	done
HDL code of the chip readout logic	done
HDL code of the chip configuration logic	done
HDL code of the TMR protected serializers	done
SEU protection of registers, counters and FIFOs	done
8b10b encoding	to be done
Header and trailer insertion with CRC calculation	done
Synthesis	done
P&R	almost done

Summary

- Development for the MVD pixel detector (ToPiX) :
  - Reduced size prototype in CMOS 0.13 μm technology tested
  - Re-design in CMOS 0.11 μm started
  - *Design freezed due to political problems*
- Development for the MVD strip detector (ToASt) :
  - 64 channel ASIC
  - Configurable for both input signal polarities.
  - Time of Arrival measurement with system clock resolution
  - Charge measurement via Time over Threshold
  - Local FIFOs for data de-randomization
  - 2$\times$160 Mb/s serial outputs
- ToASt FE and BE design in advanced status
- ToASt submission foreseen in fall 2019
  $\rightarrow$ *to be confirmed - delays in CAD license renewal are delaying the design.*

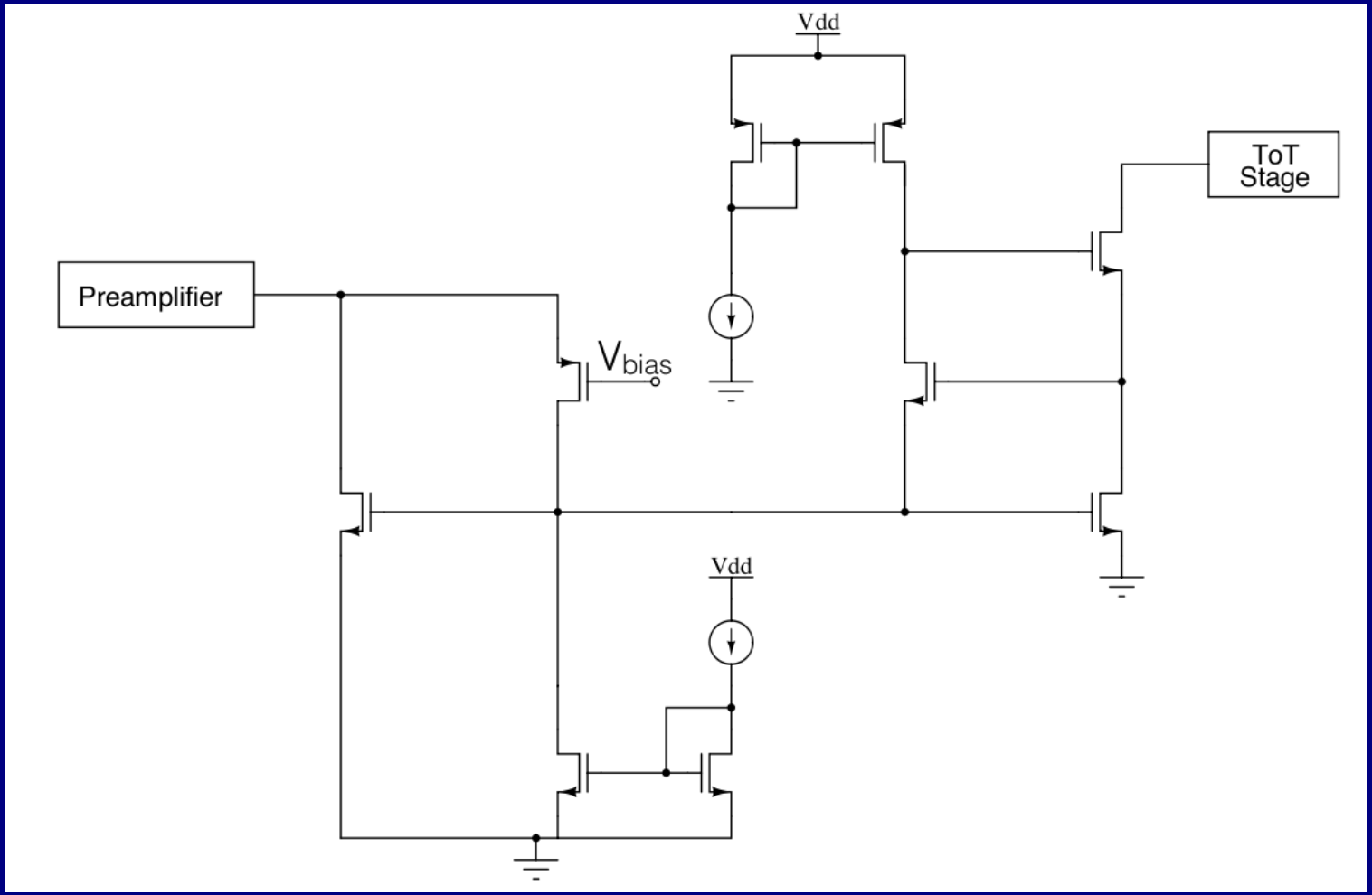
Spare slides

Preamplifier

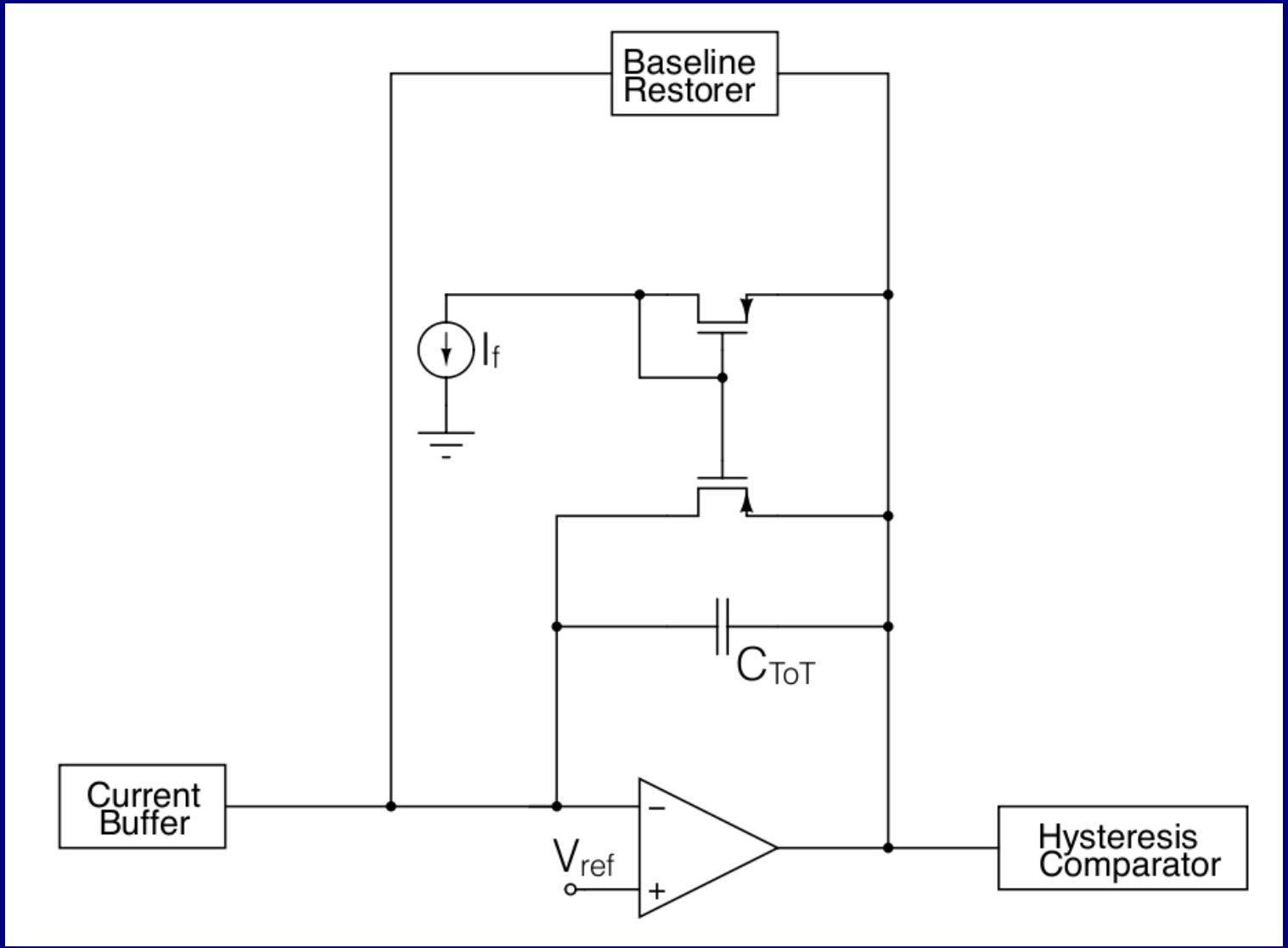


Switches control the input signal polarity.

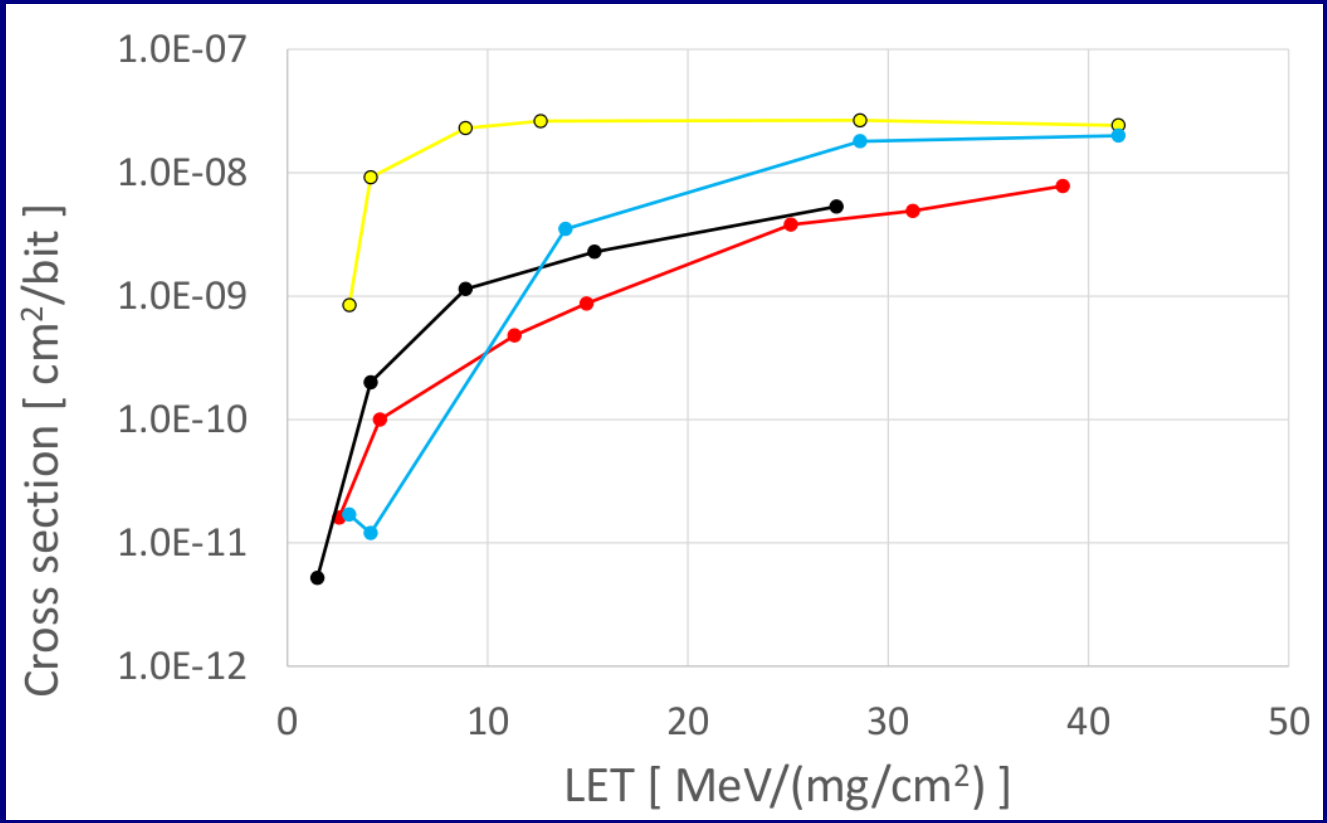
Current buffer



ToT stage


Baseline Restorer
I_f
C_{ToT}
Current Buffer
V_{ref}
−
+
Hysteresis Comparator

SEU tests : PASTA *vs* ToPiX



110 nm UMC (PASTA-TMR&Hamming encoding)
130 nm I-DM (ToPix4-TMR&Hamming encoding))
130 nm I-DM (ToPix3-TMR)
130 nm I-LM (ToPix2-DICE)

- PASTA configuration registers : 64×42 bits
- Expected SEU rate with $5 \cdot 10^6$ p/(s·cm^2) : $3 \cdot 10^9$ SEU/(s·bit)
- *Note : this is the rate for the pixel 1st disk*