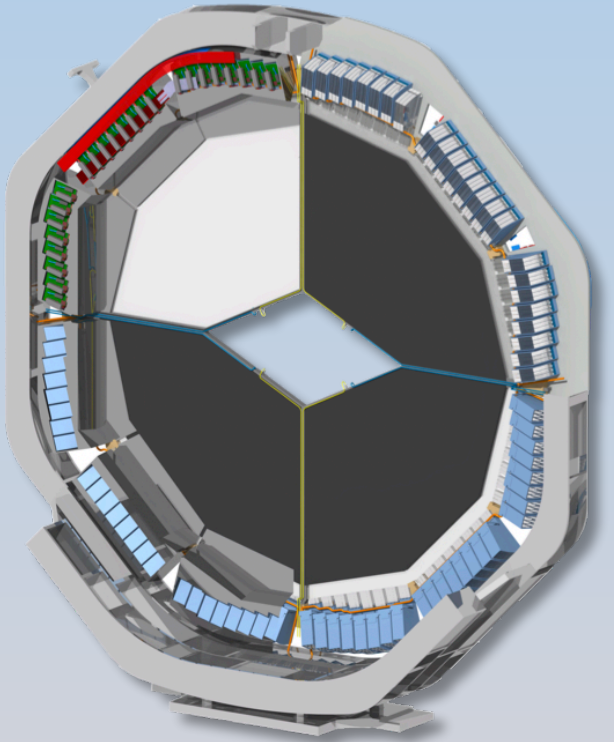
# Endcap Disc DIRC-Mechanics Status

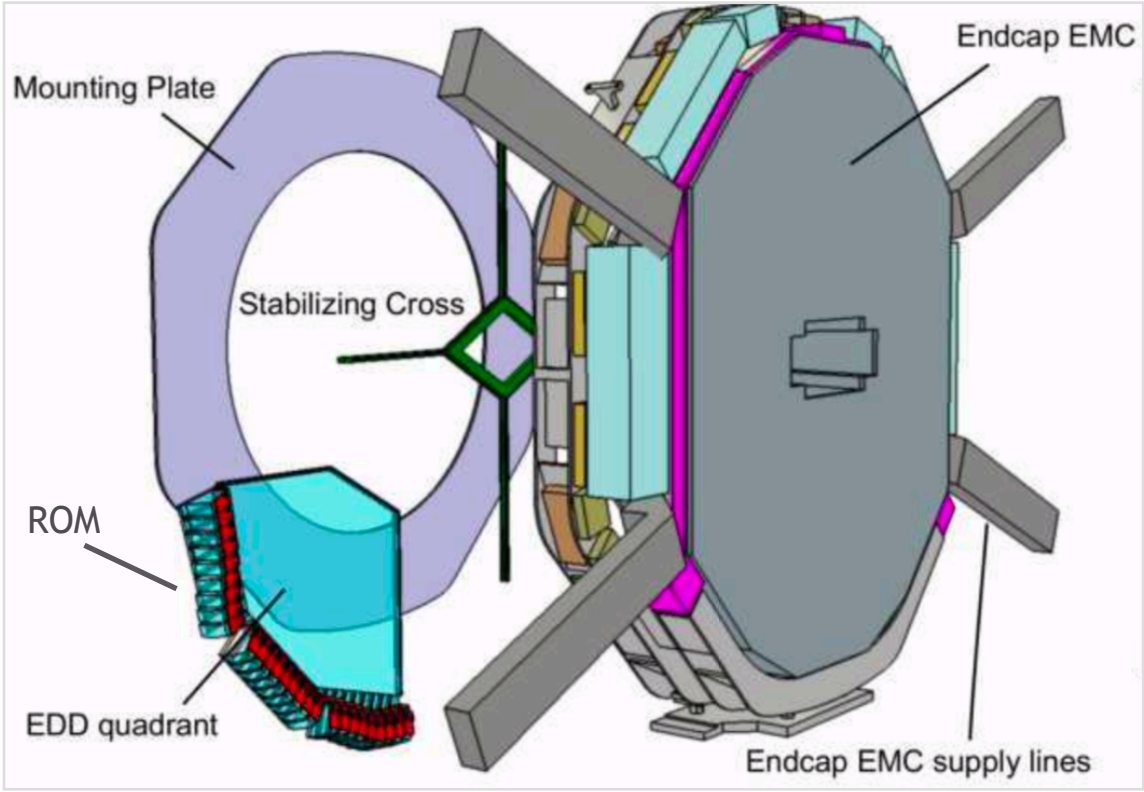


PANDA CM 19/2 – MEC Session - 2019/06/25

Ilknur Köseoğlu Sarı, Simon Bodenschatz, Lisa Brück, Michael Düren, Avetik Hayrapetyan, Jan Hofmann, Sophie Kegel, Jhonatan Pereira de Lira, Mustafa Schmidt, Marc Strickert

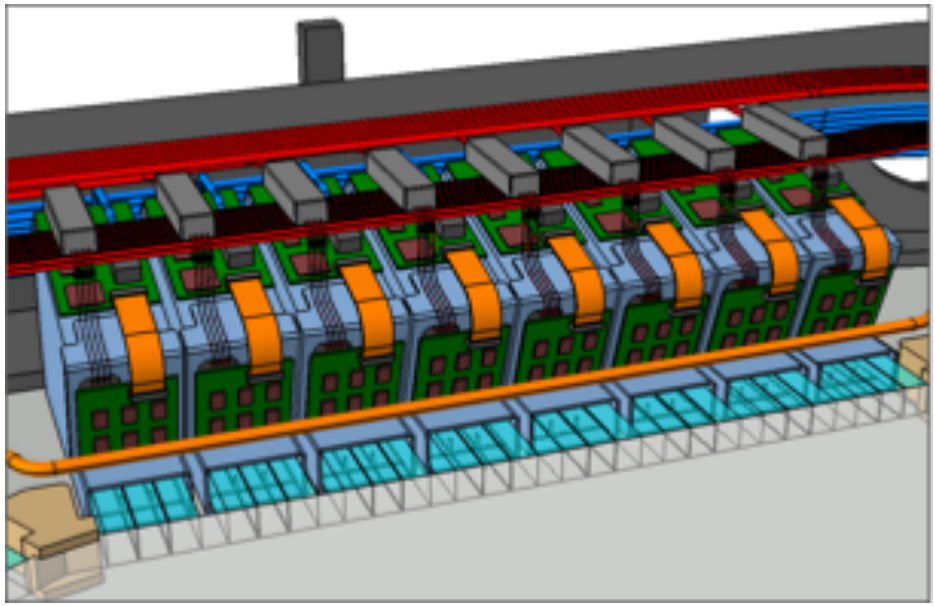
# EDD elements

- Quadrants
  - Light tight
  - Gas tight
- Mounting Plate, MP
- Stabilizing Cross
- Readout Modules, ROM
  - Light tight
  - Gas tight
  - 96 ROMs in total
  - 24 ROMs/Quadrant

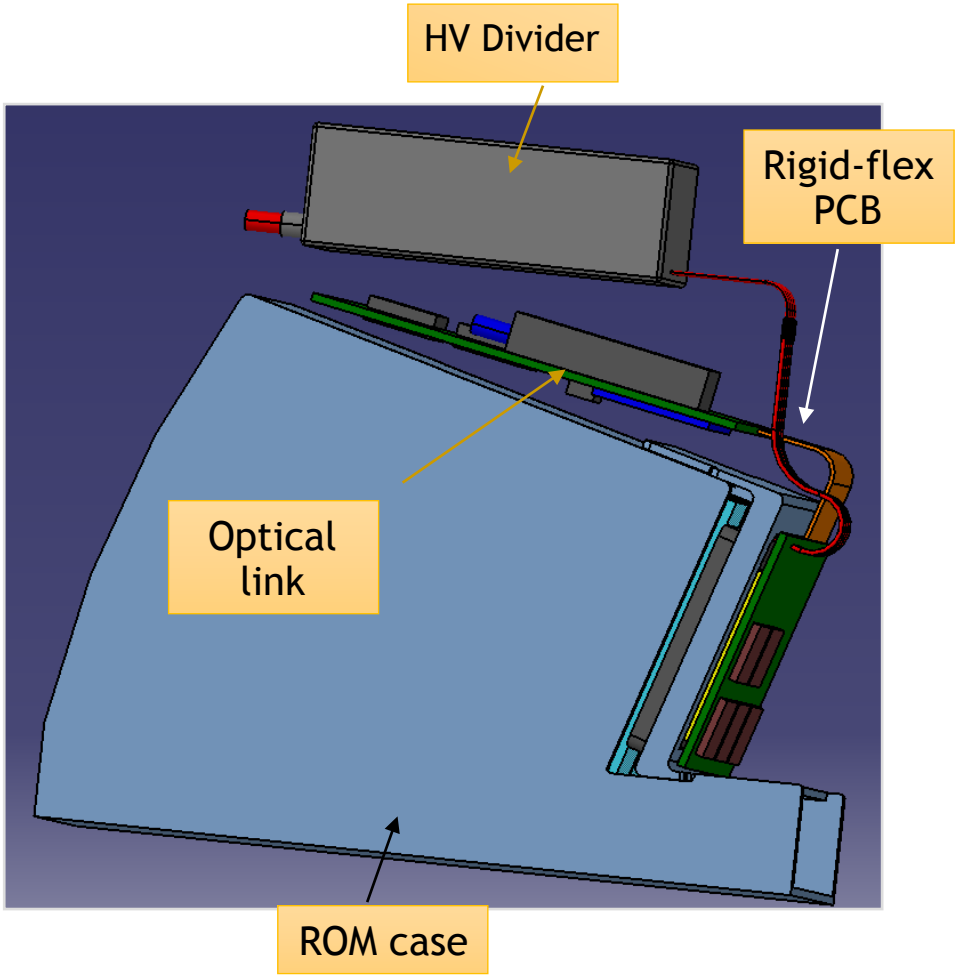


# Readout module (ROM)

- 3 Focusing elements
- 3 Bars
- ROM case
- Rigid-flex PCB
- HV divider

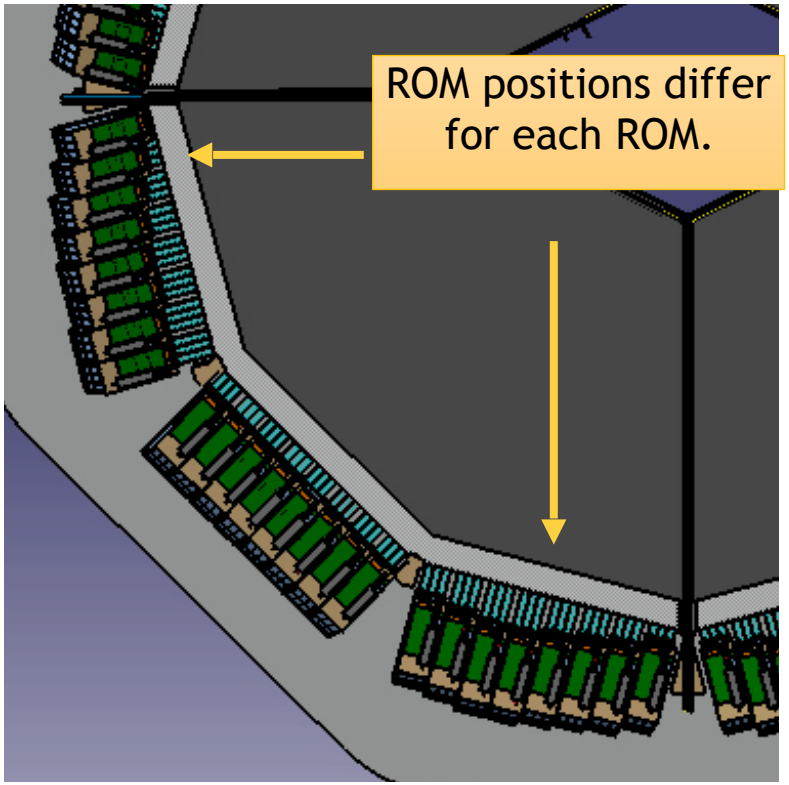


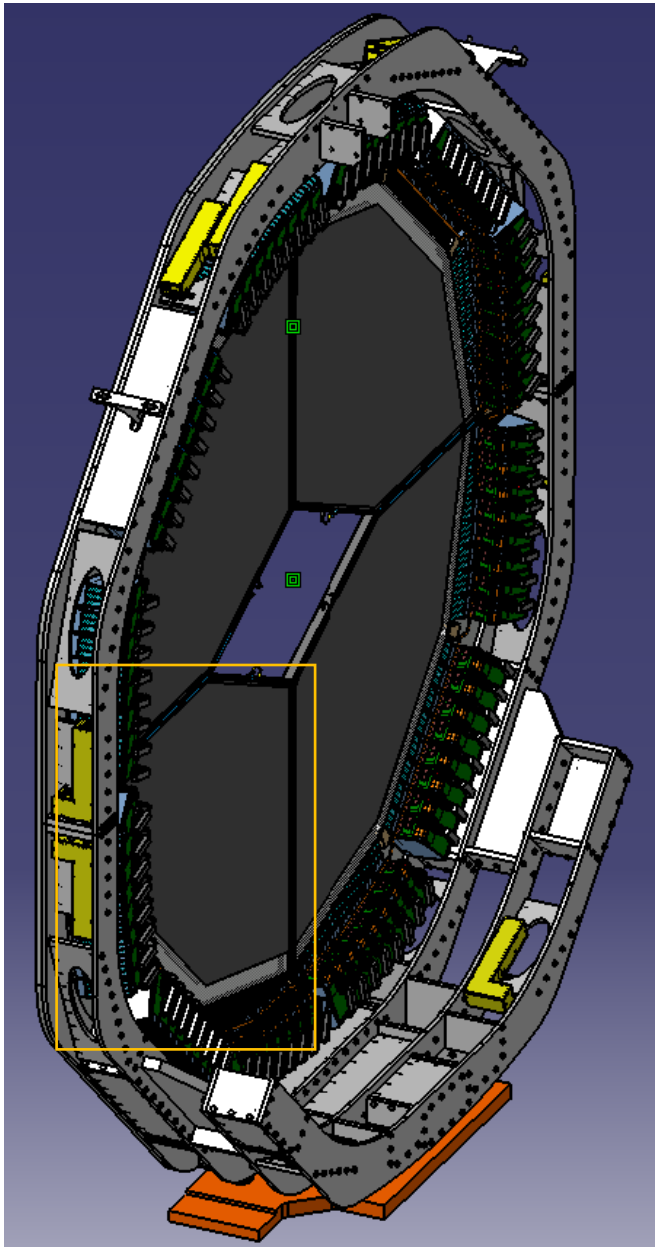
Alignment of 8 ROMs



# Mounting plate & Support frame

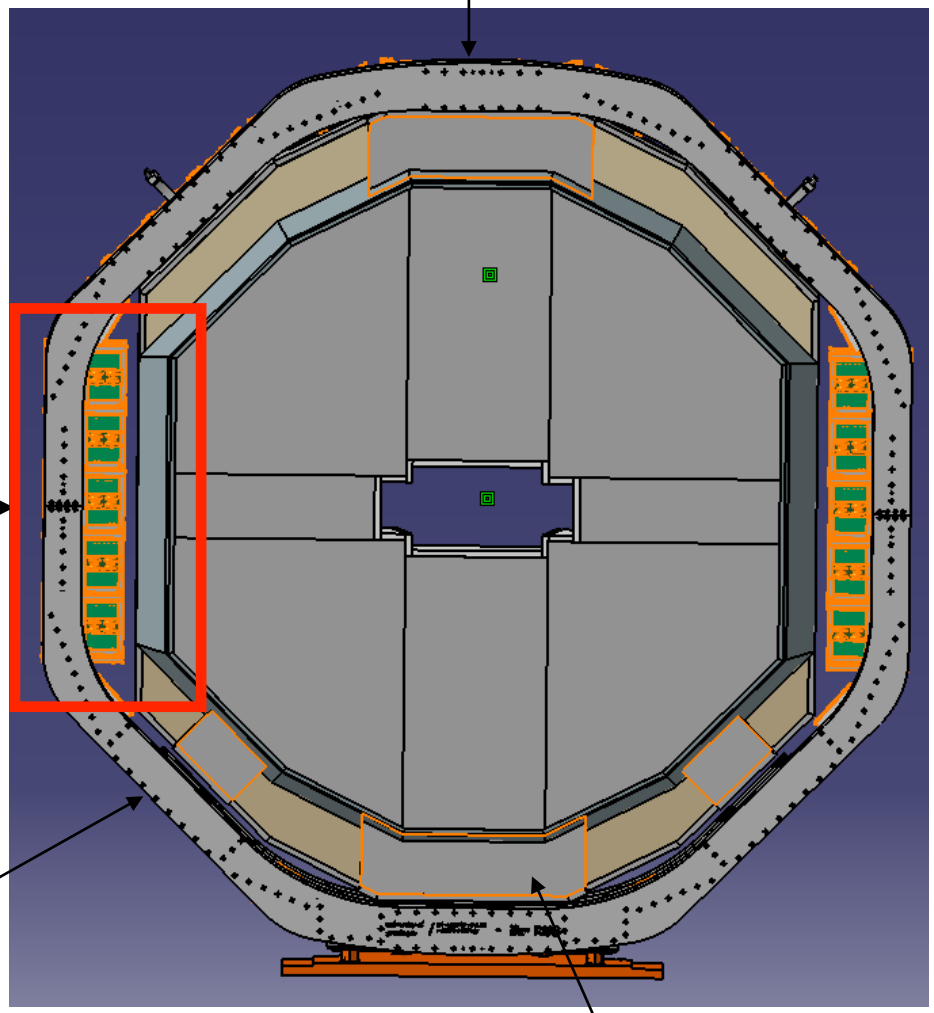
- 96 ROMs align around the EDD radiator
- Because of the EMC insulation, ROM position differs for each region.



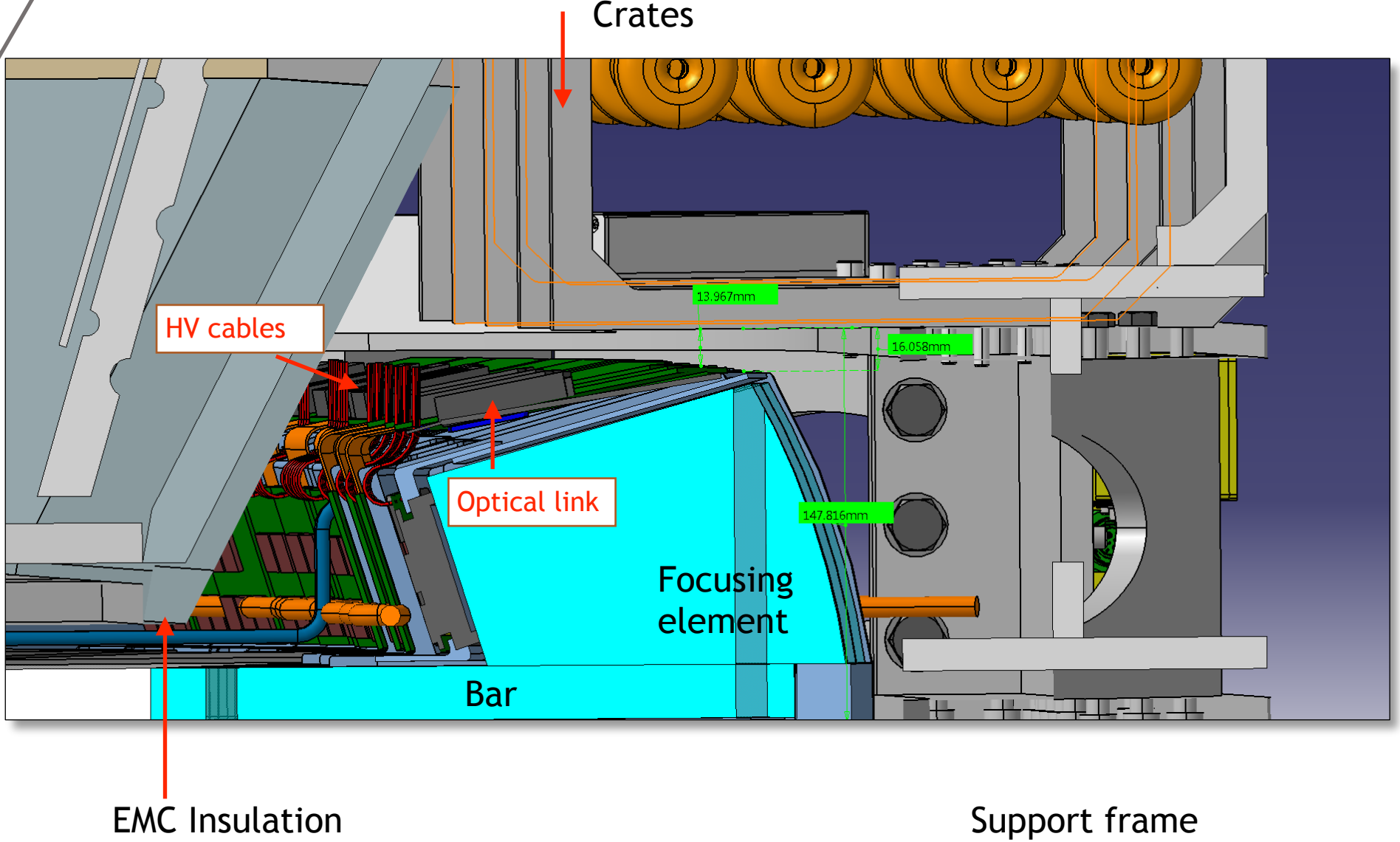



# Limited regions

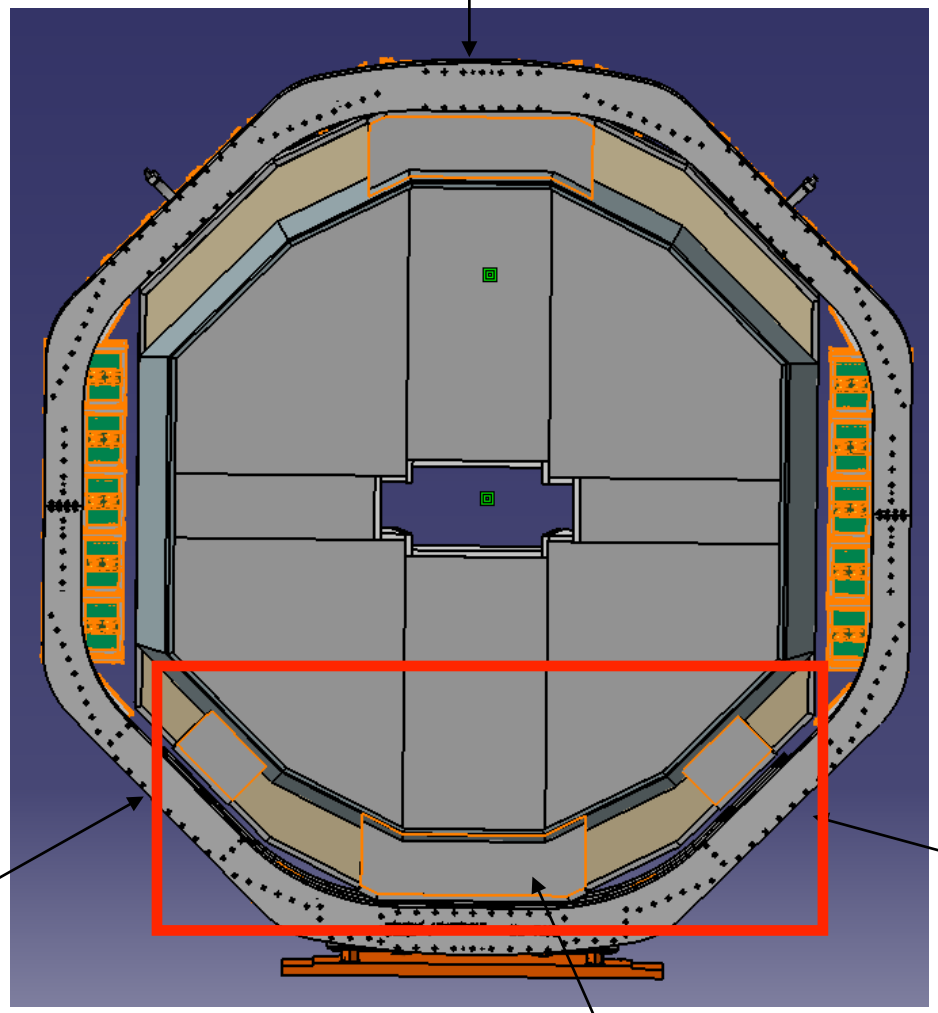
- Lightened areas are critical regions
- Spatial constraint changes depending on phi-angle.
  - Crate region at two sides
  - Leg region
  - Insulation at bottom



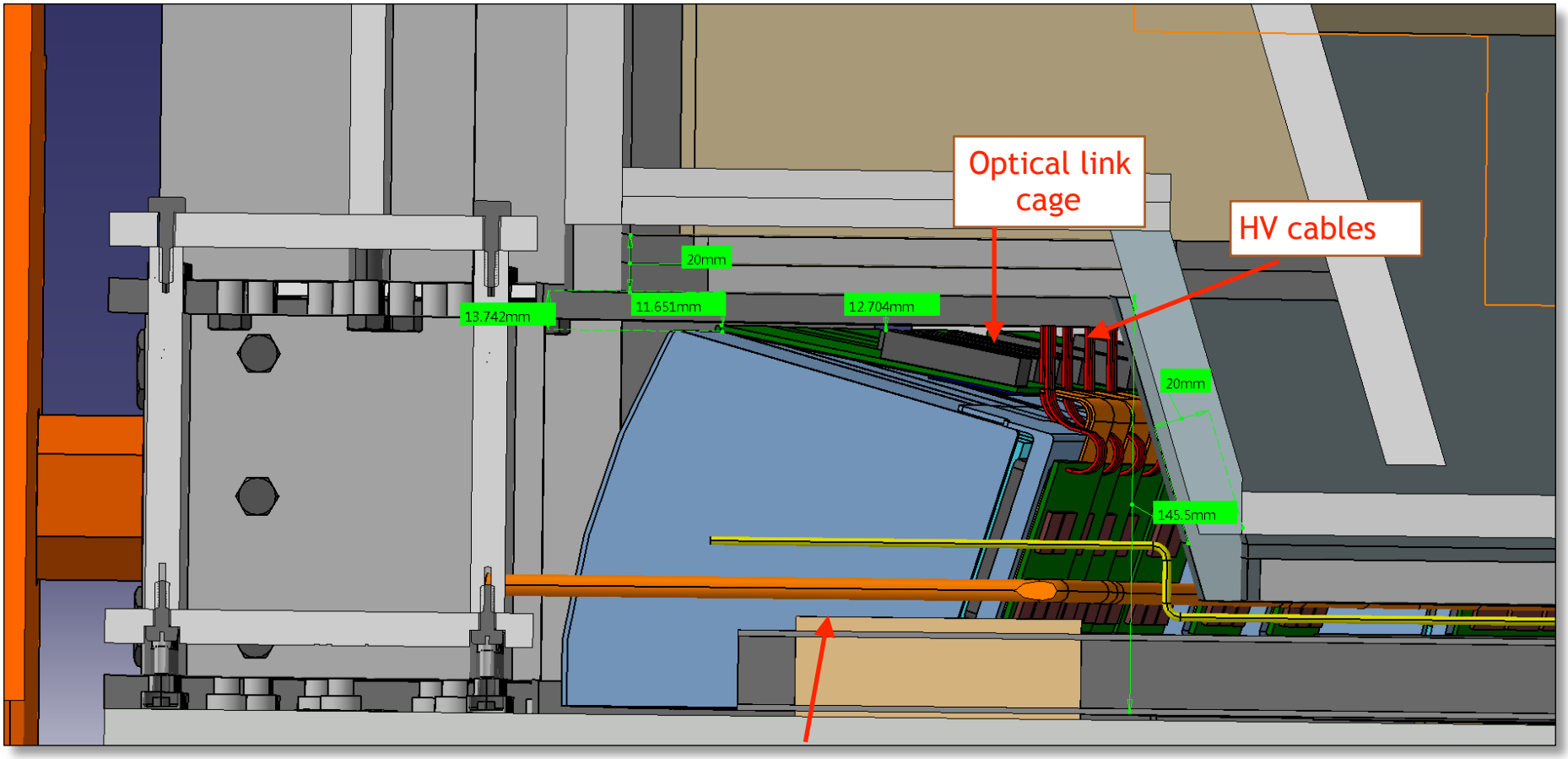
# Crate region



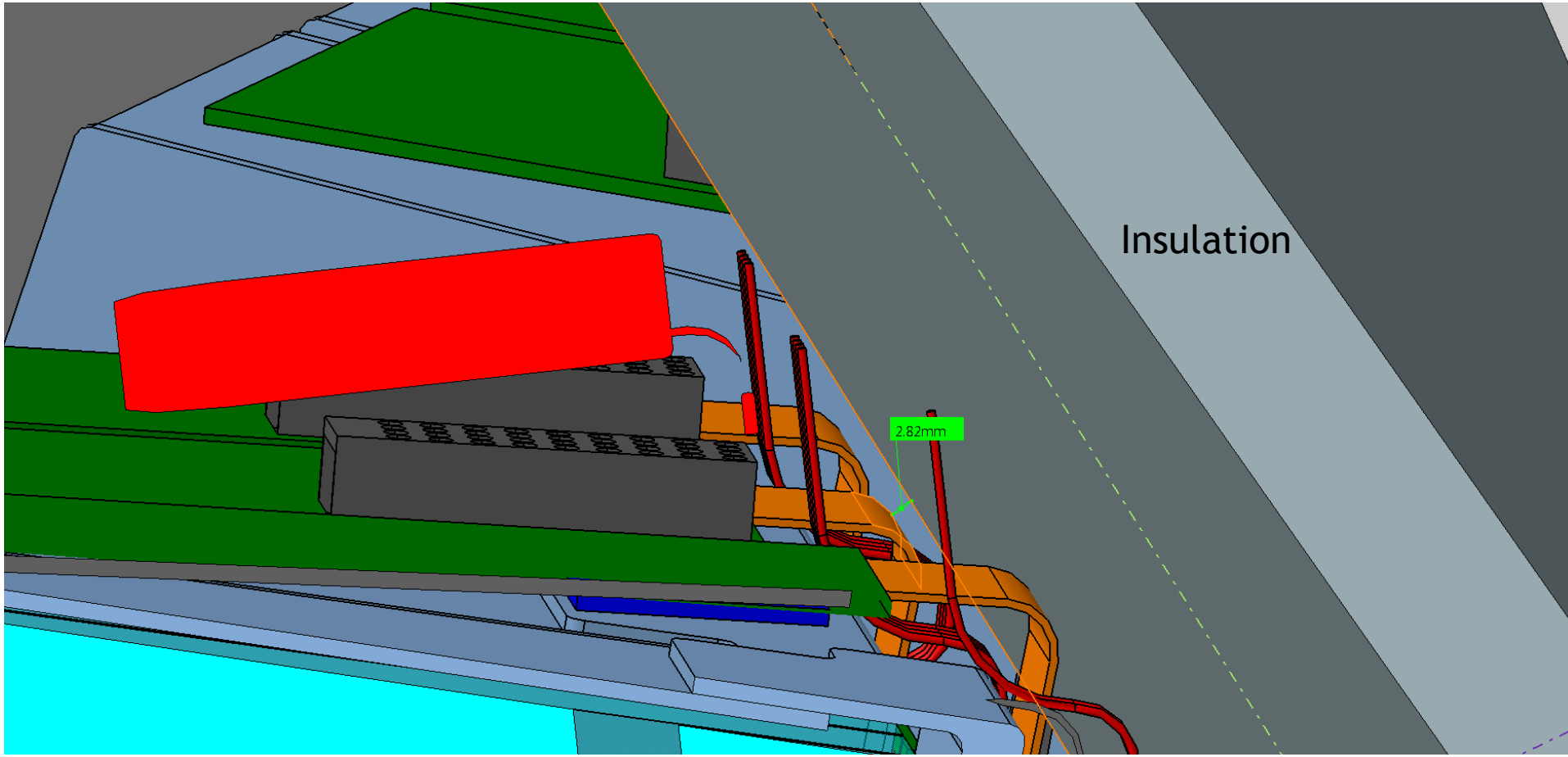
# Limited regions



# Leg region


Optical link cage
HV cables
20mm
13.742mm
11.651mm
12.704mm
20mm
145.5mm
Cooling pipe for ASICs

# Radial limit




- Distance between insulation and flex PCB is ~ 3mm in radial direction.

# Problems

- There are limits both z-direction and radial direction.
- No space for cable alignment
  - HV cables
  - LV cables
  - Optical link
- Cooling system for FPGA has not been implemented yet!
- No space for HV divider

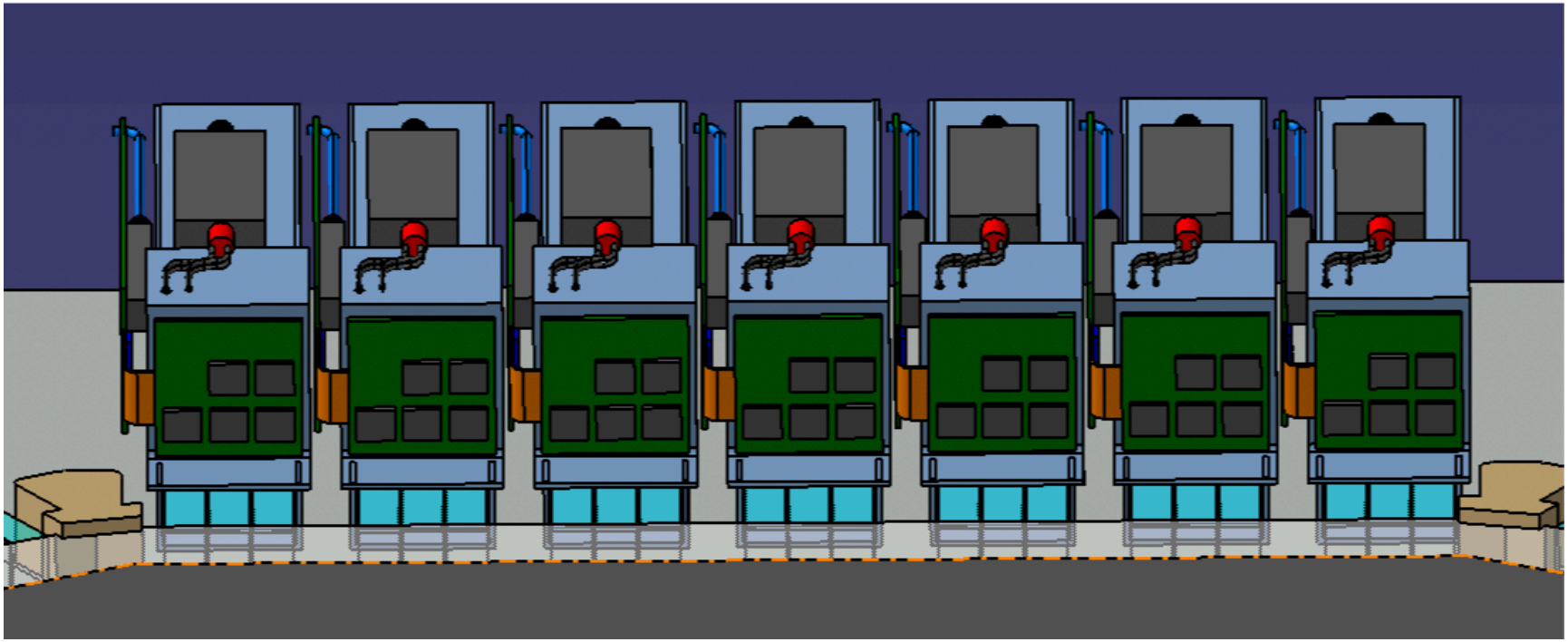
## Cable specifications

| type | connection | number | diameter [mm] | cross section [$mm^2$] |
|---|---|---|---|---|
| HV | 96 MCP-PMTs | 96 coaxial cables | 5 mm | 2,400 |
| LV | 96 ROMs | 192 cables | 2.5 mm | 1,200 |
| data | 96 ROMs | 96 optical fibers | 5 mm | 2,400 |
| gas | 4 quadrants | 8 pipes | 10 mm | 800 |
| cooling | 4 quadrants | 8 pipes | 60 mm | 28,800 |
| laser | 4 quadrants | 4 optical fibers | 5 mm | 100 |

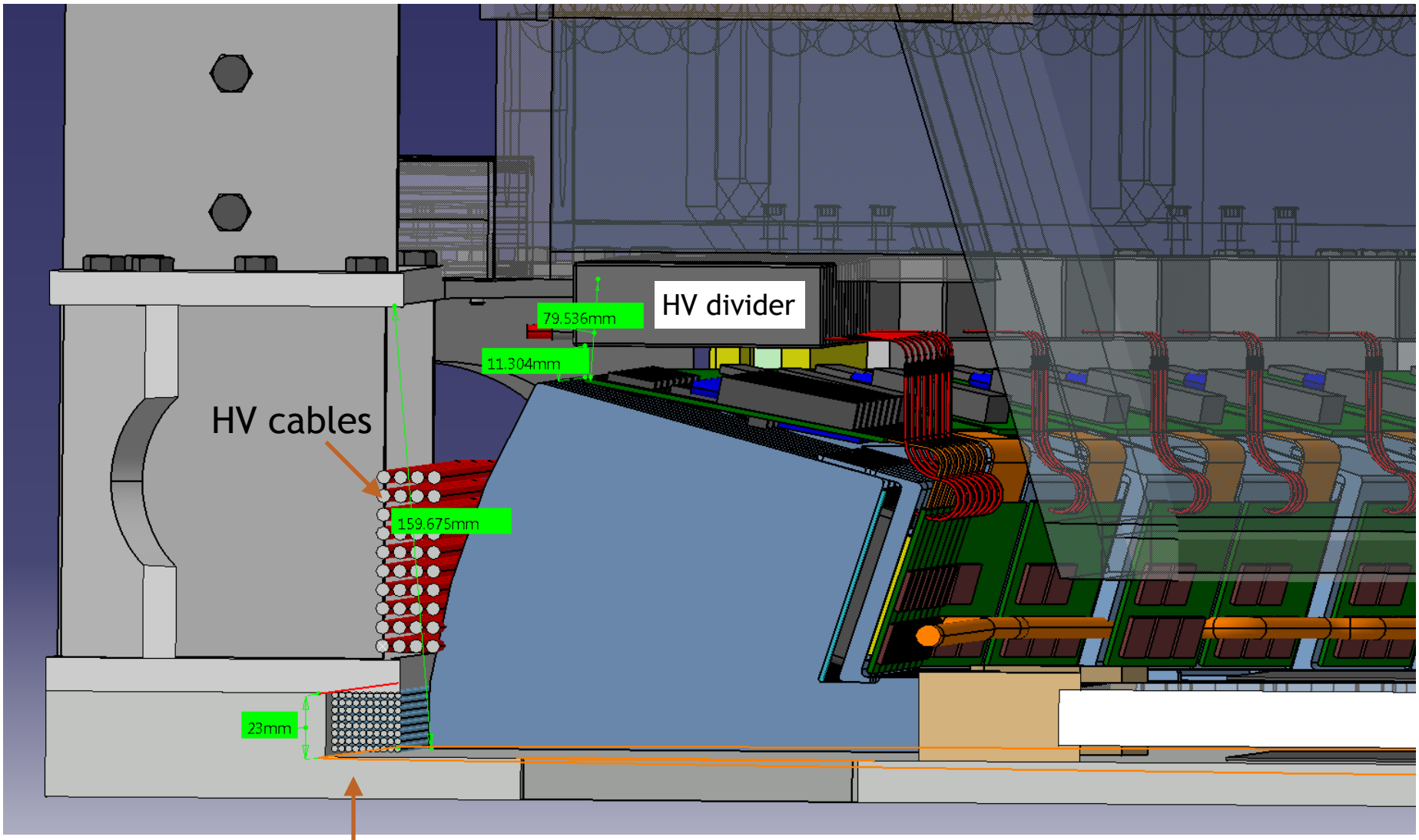
# Proposed solutions

1. Reduce number of ROMs in each quadrant, not preferable.
2. Moving EDD through the upstream direction. EDD is in-between GEM detectors and forward EMC.

7 ROMs design



# New design

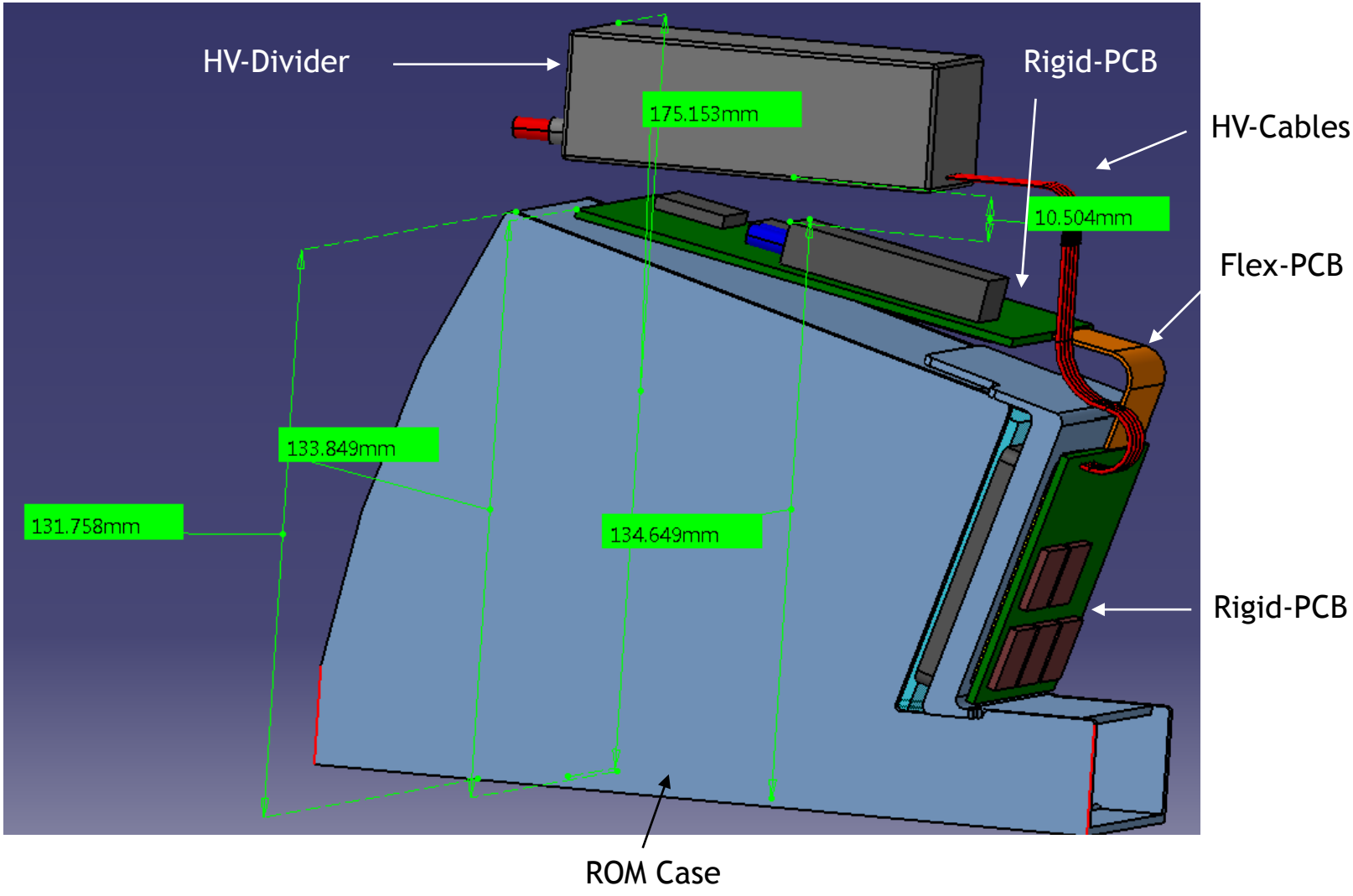

HV divider
79.536mm
11.304mm
HV cables
159.675mm
23mm
LV cables

# New design

- There will be one more frame between mounting plate and support frame.
- We can align HV-LV cables.
- There is a distance between EMC insulation and EDD electronics.
- HV divider can be implemented on top of the ROM.
- Cooling system can be designed also for FPGA.

Thanks for your attention!

# Backup


HV-Divider
Rigid-PCB
HV-Cables
Flex-PCB
Rigid-PCB
ROM Case
175.153mm
10.504mm
133.849mm
131.758mm
134.649mm