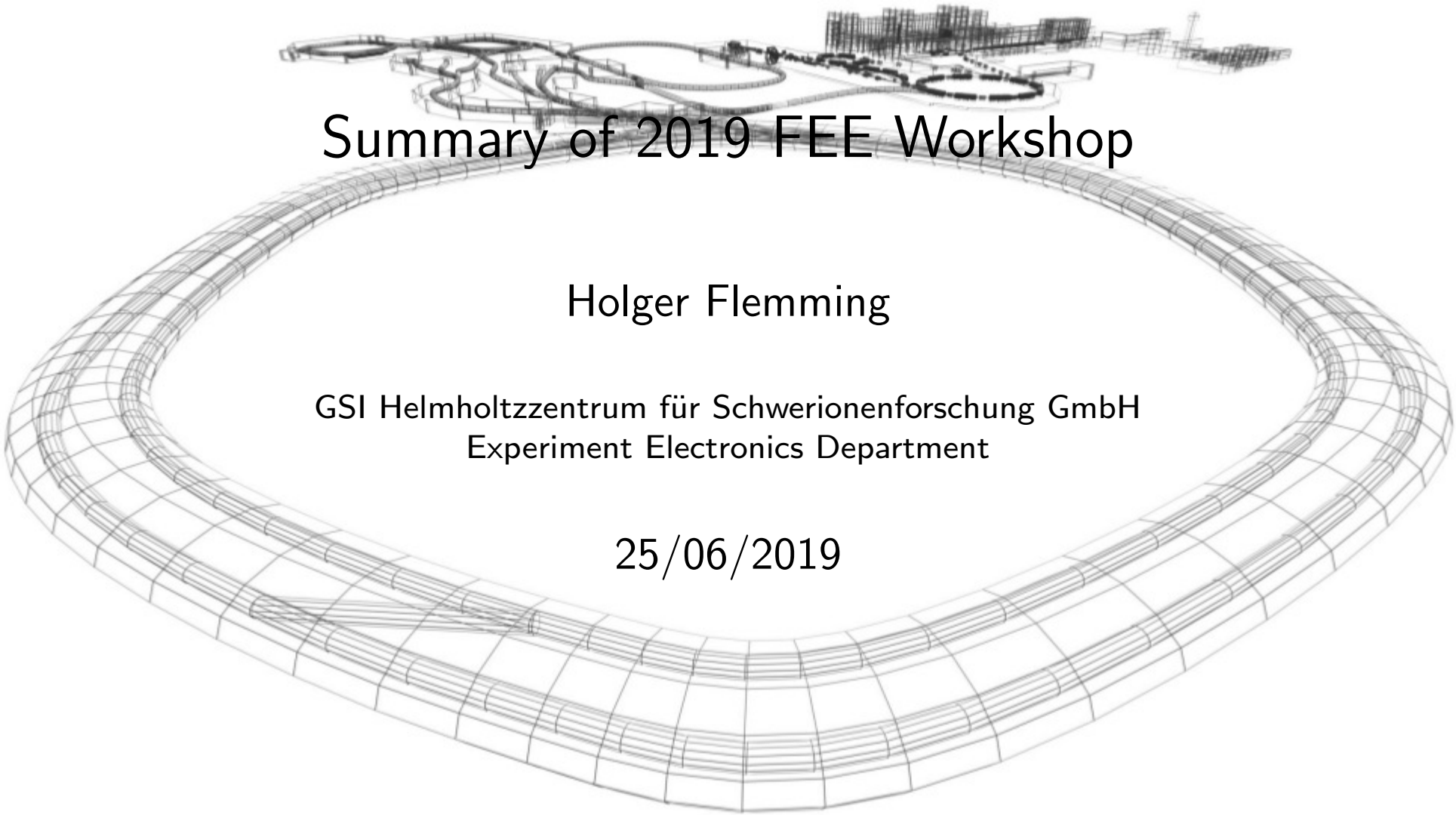


Summary of 2019 FEE Workshop

Holger Flemming

GSI Helmholtzzentrum für Schwerionenforschung GmbH
Experiment Electronics Department

25/06/2019

PANDA FEE/DAQ Workshop

- Held on May 27th to May 29th at GSI Darmstadt
- 24 Registrants
- Monday afternoon and Tuesday morning dedicated to FEE
- 7 Presentations
- Intensive Discussions

G. Mazza: MVD Electronics

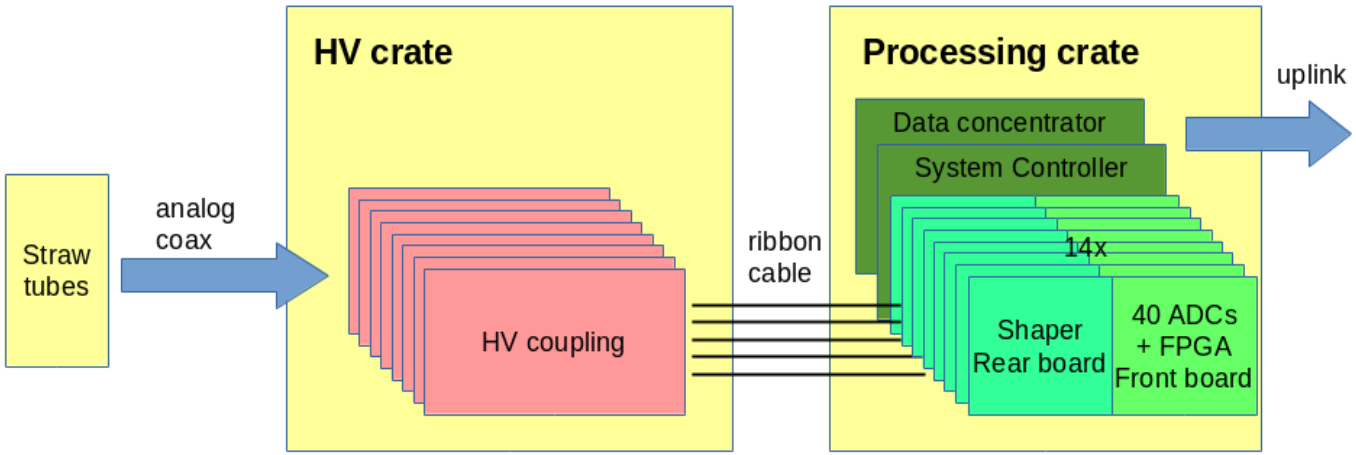
Summary

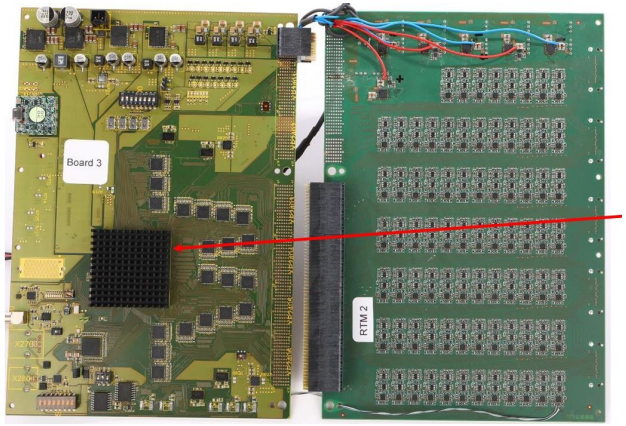
- Development for the MVD pixel detector (ToPiX) :
  - Reduced size prototype in CMOS 0.13 θm technology tested
  - Re-design in CMOS 0.11 θm started
  - Design freezed due to political problems
- Development for the MVD strip detector (ToASt) :
  - 64 channel ASIC
  - Conf gurable for both input signal polarities.
  - Time of Arrival measurement with system clock resolution
  - Charge measurement via Time over Threshold
  - Local FIFOs for data de-randomization
  - 2×160 Mb/s serial outputs
- ToASt FE and BE design in advanced status
- ToASt submission foreseen in fall 2019
  → to be conf rmed - delays in CAD license renewal are delaying the design.

P: Kulessa: ADC Based STT Readout

System overview:

JÜLICH FORSCHUNGSZENTRUM





Mitglied der Helmholtz-Gemeinschaft

C. Schwarz: Barrel DIRC

DIRICH

PANDA-DIRC/CBM-RICH and HADES-RICH

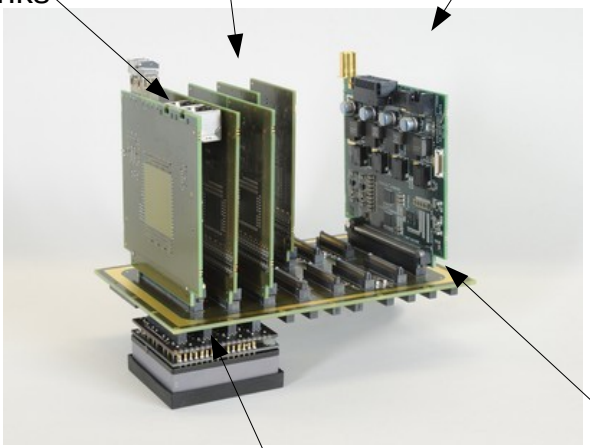
Successor of PADIWA3 + TRB3

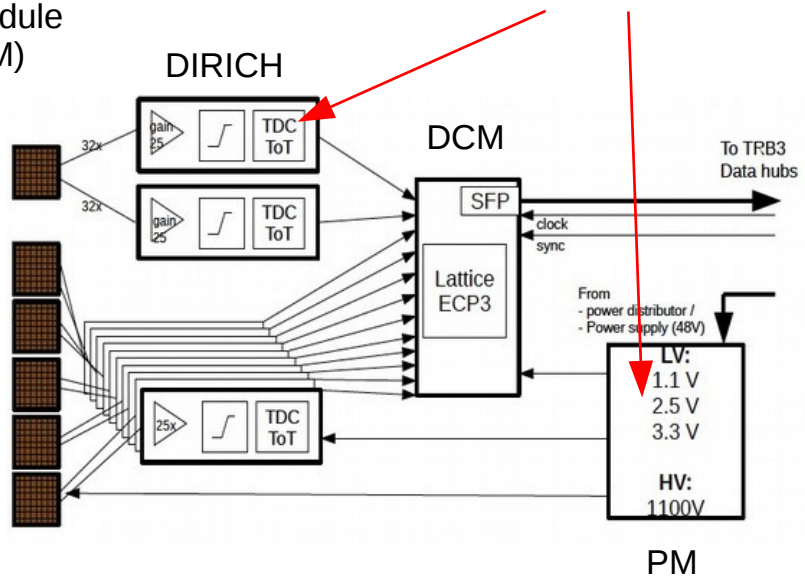
Voltages, currents, Temperature monitored by perl scripts via TRB-net.

12 DIRICH FPGA TDC

Power Module (PM)

1(2) 4.8 Gb/s links





Communication via back plane

Data Combiner Module (DCM)

Power into the detector: one voltage / many voltages?

128 MCP-PMTs:

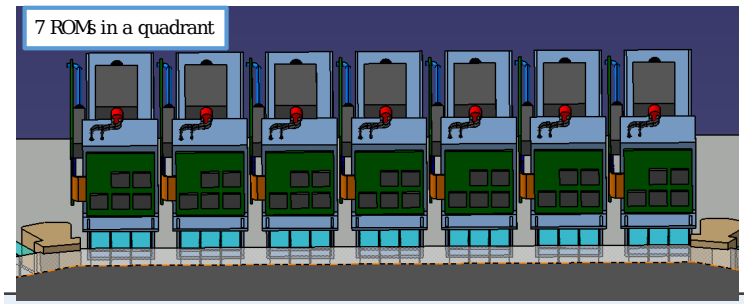
256 DiRICH
~400 A @ 1.1 V

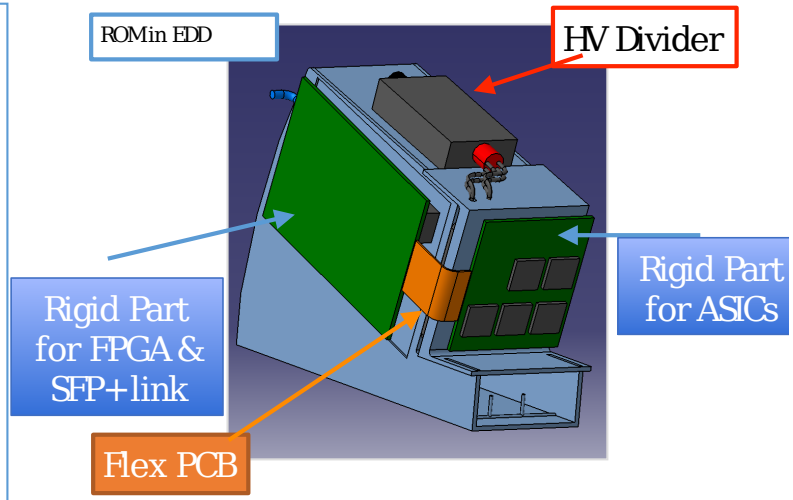
I. Koeseoglu: DISC-DIRC

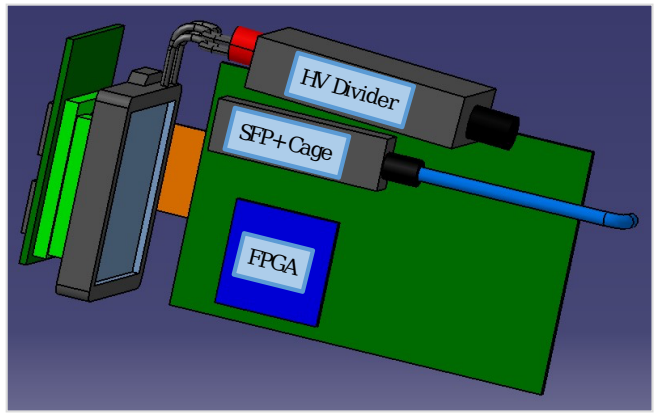
New Design

- 1 Quadrant:
  21 ROMs, 21 MCP-PMTs, 63 Focusing Elements (FELs)
- MCP-PMTs:
  Hamamatsu has 128 x 3, 384 pixels
  Photonis Aqua has 100 x 3, 300 pixels
- PCB design:
  2 rigid PCBs are connected via flex PCB.
  1Rigid-flex PCB
  - 5 ASICs
  - 1 FPGA
  - 1 Optical link

  FPGA is on the side PCB, ASICs are on bottom PCB.
  Flex PCB should be bended at least 4.5mm radius.
- Cables:
  HV, LV, Optical link (SFP+connection), Clock and Synchronization.
  Sensors will be powered separately by HV cables.
- Cooling System:
  Cooling system should be designed both FPGA and ASICs.





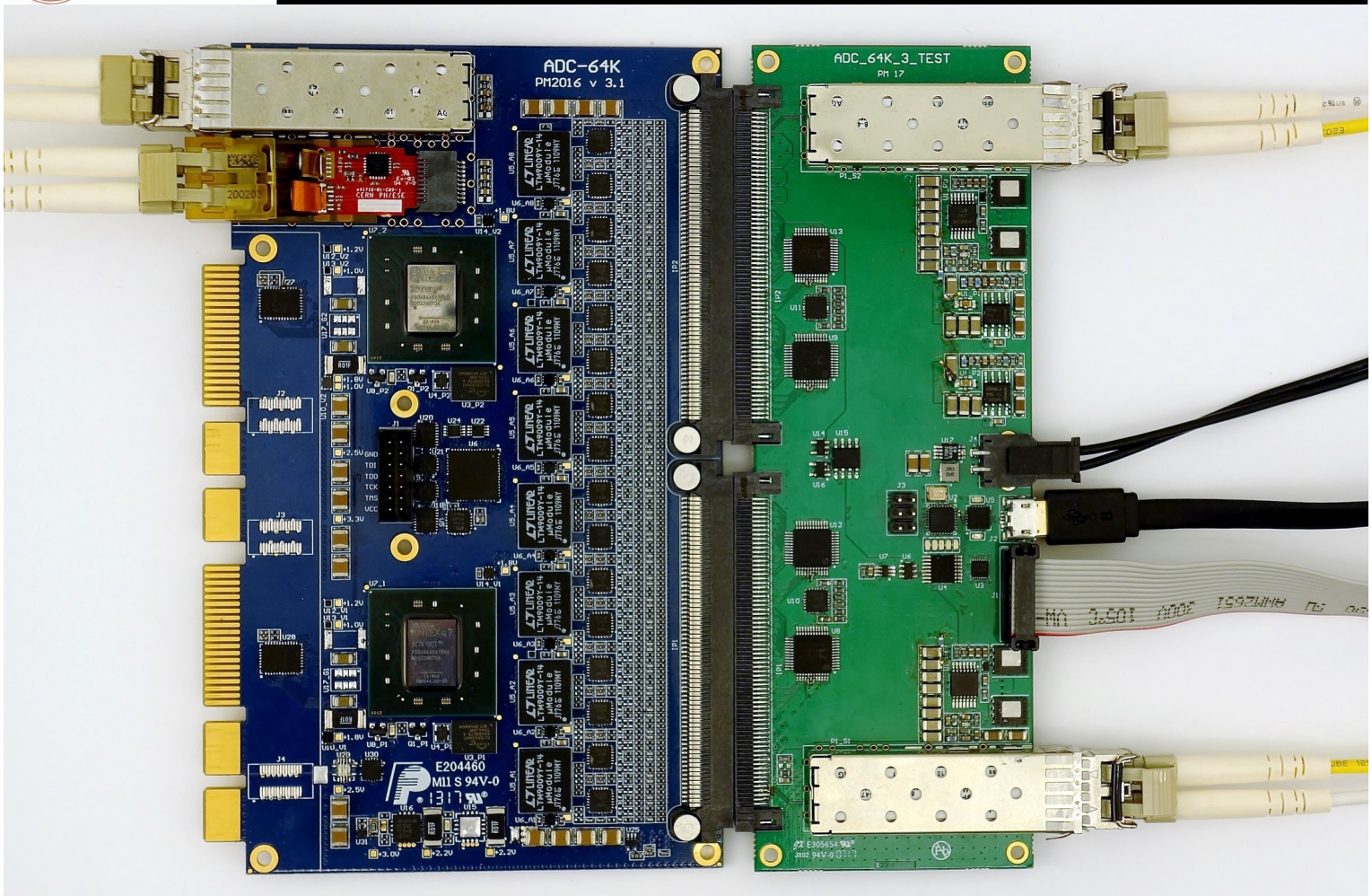


P. Marciniewski: Tests of EMC FEC ADC Boards

UPPSALA UNIVERSITET

ADC for EMC-Endcap

- Post-production functional tests



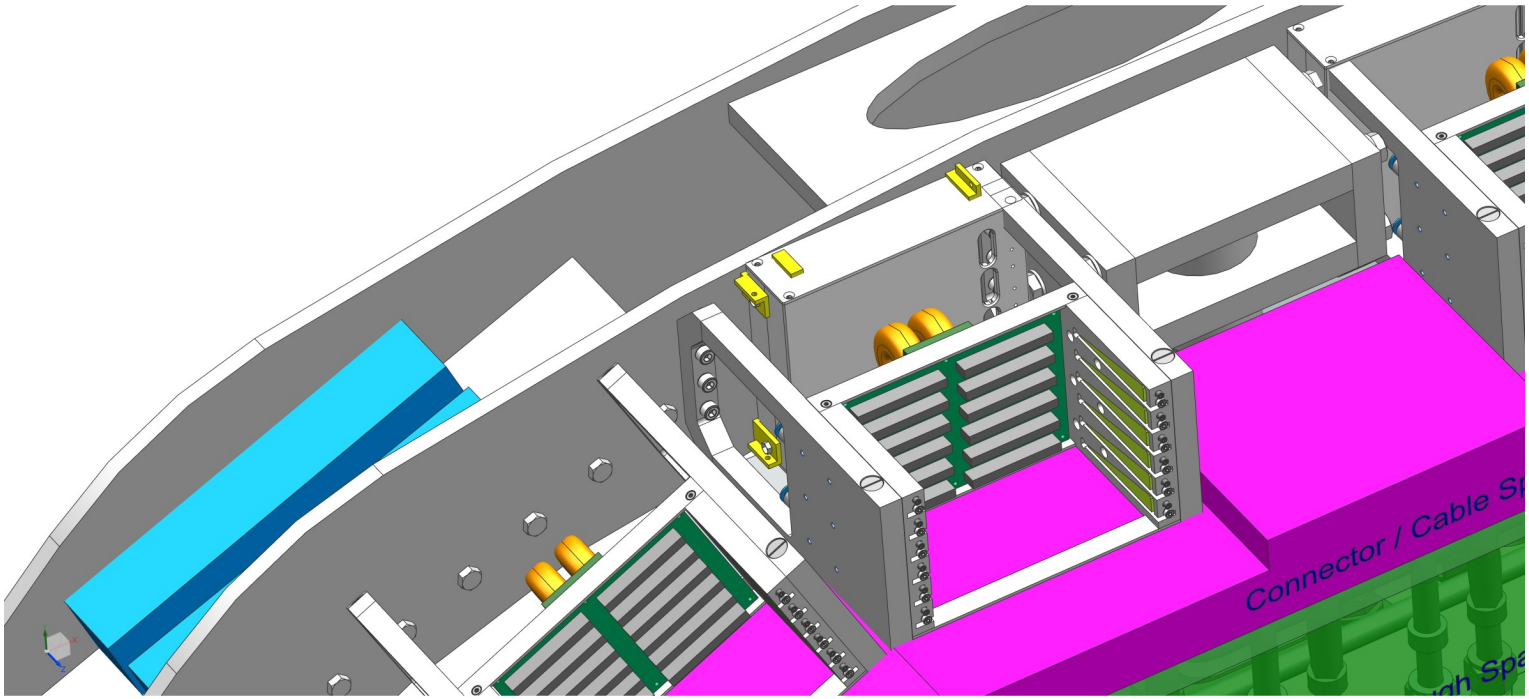
Pawel Marciniewski, PANDA FEE Meeting, GSI 28.05.19

P. Marciniewski: Crate Rear Components

UPPSALA UNIVERSITET

ADC for EMC-Endcap

- Encapsulation and Cooling



Courtesy KVI

Pawel Marciniewski, PANDA FEE Meeting, GSI 28.05.19

P. Marciniewski: LVDS Readout Boards

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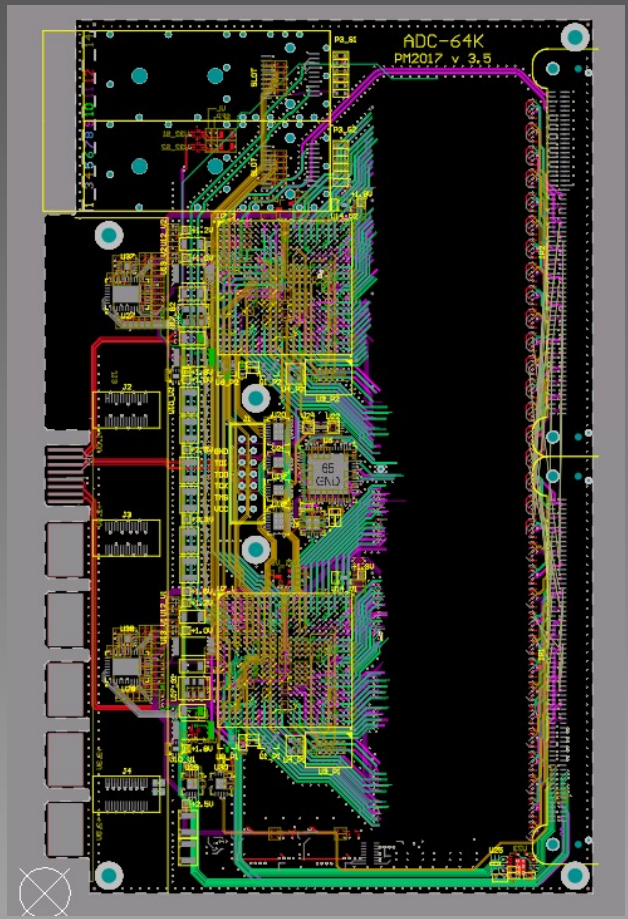
EMC Barrel Electronics

- LVDS ROB



Readout Board obtained from the 64-channel ADC for the EMC Forward Endcap

Status:

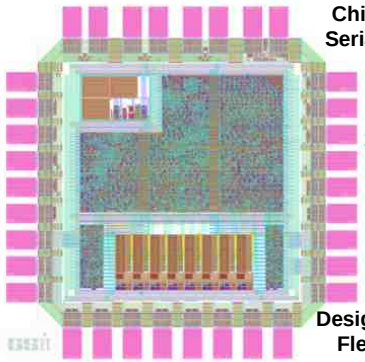
- Re-design started
- ADC and analog parts removed
- Data connector type needs to be decided
- Board placement and casing need to be decided

Pawel Marciniewski, PANDA FEE Meeting, GSI 28.05.19

C. Hahn: SerialAdapter ASIC

Motivation

- **Present design:** two different busses for FE and HV regulators
- **Idea**: integrated slow control ASIC with common interfaces (I2C, SPI and APFEL interface)
- Daisy chaining of Backend-Interface for 5 (10) backplane PCBs → Saves 4/5 of slow control cables (36 vs. 180**)**
- Use DACs for HV adjustment

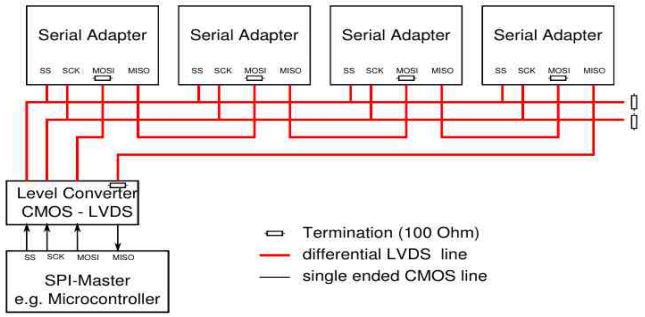


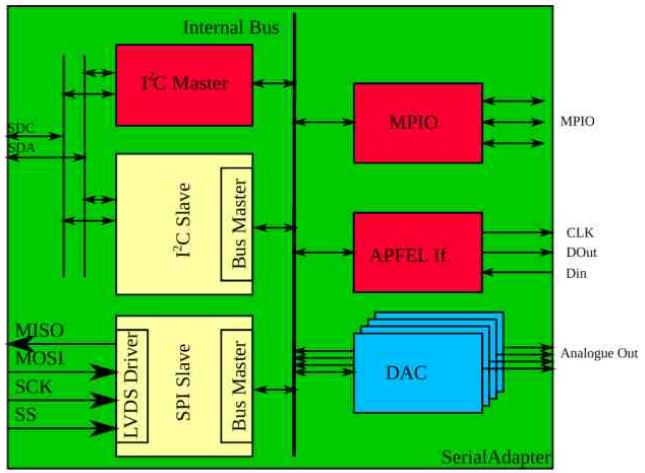
Chip layout of the SerialAdapter ASIC

1:5 × 1:5 mm Mini ASIC In UMC 180 nm CMOS technology

Designed by Holger Flemming (GSI)

Using a daisy chained SPI interface





H. Flemming: HitDetection ASIC