Faul Tolerant Local and Monitoring Control Board

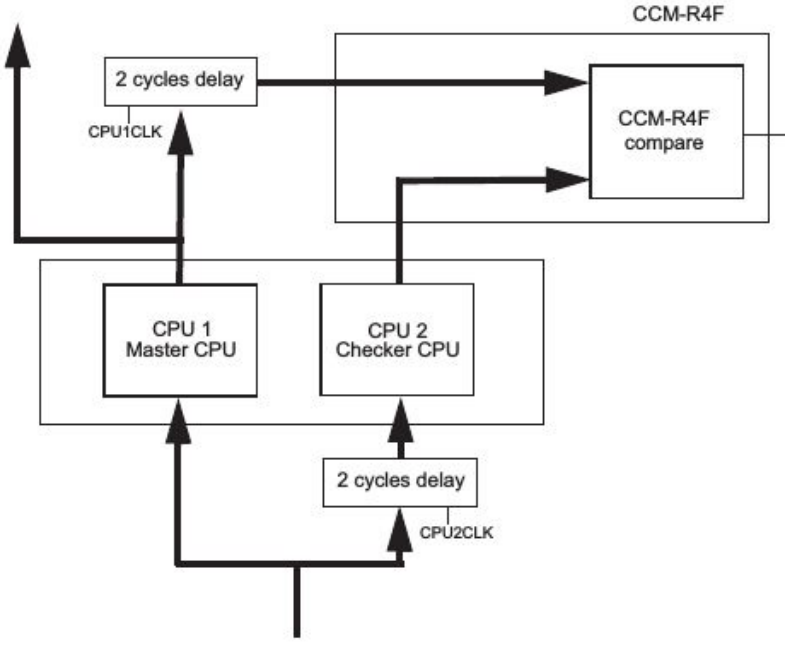
Research group Prof. Udo Kebschull
José Antonio Lucio Martínez

Infrastructure and Computer Systems in Data Processing
Goethe Universität Frankfurt

Reasons to develop FTLMC

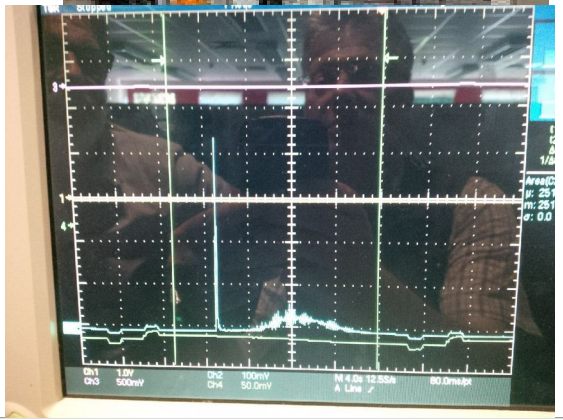
- Ionizing radiation causes Single Event Effects in semiconductors
- SEE’s are problematic and can result in serious malfunctions
- ARM produces intellectual property fault tolerant processors:
  - Safety and redundancy: arm7v4 **Cortex R5F**
  - Vendor that produces such a chip is: **TI- TMS570**
  - Build a control board based on that chip: **FTLMC**
- Robustness in detector environment

Cortex R5F


CCM-R4F
2 cycles delay
CPU1CLK
CCM-R4F
compare
CPU 1
Master CPU
CPU 2
Checker CPU
2 cycles delay
CPU2CLK

Beam test of the Cortex-R (TI-TMS570)

- Exposed MCU directly to beam during: 13 hours
- Beam: 2Gev Protons
  - In spike: 7 x 10^7
  - in normal extraction: 2 x 10^8
  - spill: 20s
  - Pause: 10s
- Total detected and corrected SEU's:
  - in Bank A: 718
  - In Bank B: 686
- No unrecoverable errors
- Failure registers continuously monitored
- Database with error time-stamp
- No errors during beam off times detected



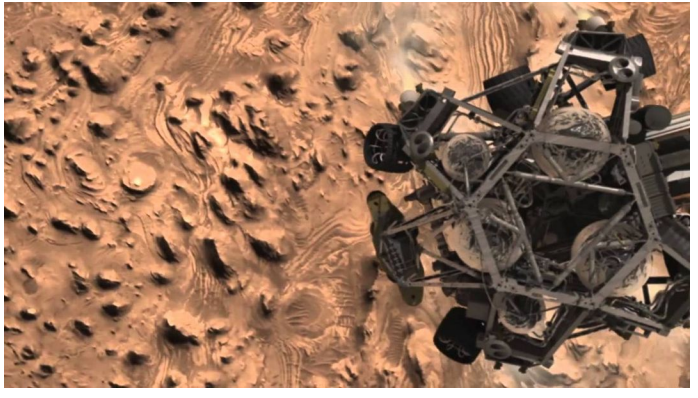
FTLMC Software Challenges

- EPICS is a distributed control system
- Supports every well known operative system
- Uses Channel Access, a network protocol for monitoring and control
- Soft real time capabilities
  - Real Time Executive Multiprocessor System RTEMS
  - Deadline priority based operative system for time constraint app.
  - Necessary in industrial environments with critical variables

RTEMS

- Developed by US military for rockets in the 70's decade
- 2012
  - EADS/Astrium states all projects in DE/UK/FR use RTEMS
  - Curiosity lands on Mars with RTEMS
- 2011
  - RTEMS orbits moon on-board ARTEMIS
  - OAR is a sponsor of the Flight Software Workshop
- 2010
  - RTEMS File System (RFS) added for NASA MMS

source: https://devel.rtems.org/wiki/History/Timeline



RTEMS

- Was ported to FTLMC for better EPICS integration

Galvanic isolated UART RS-485

Galvanic isolated 2 x CANBUS

1Mb/s UART → RS-232

I^2C, SPI, 7 ADC Inputs, 85 GPIO's

Ethernet capability