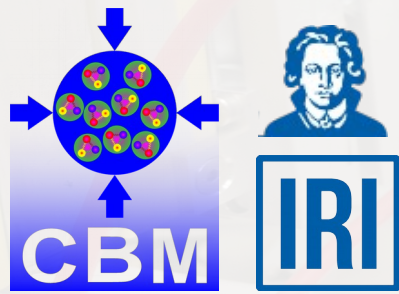
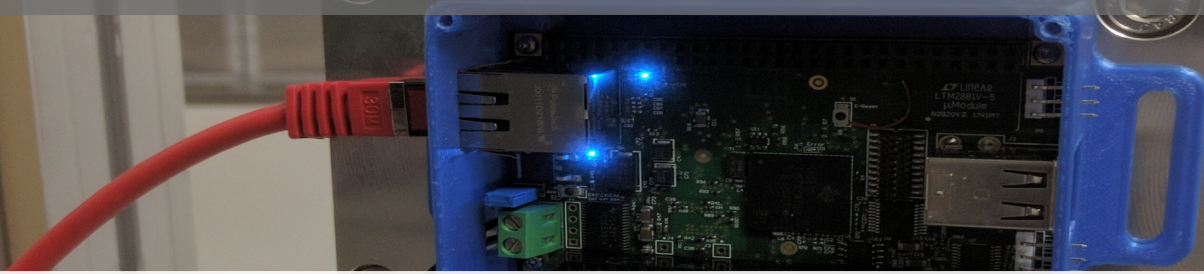


A new Fault Tolerant Local Monitoring Control Board with SEU mitigation and execution redundancy commercial micro-controller



José Antonio Lucio Martínez
Research group Prof. Udo Kebschull
Infrastructure and Computer Systems in Data Processing
Goethe Universität Frankfurt

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Outline

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- Radiation Problem: Single Event Effects
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- Cortex-R at Beam Test
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 - Real time issue
 - Software Status
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Detector Control System Overview

- Monitor sensors and establish actuators values
- Ensures integration of digital / analog sensor data
- Provides connectivity with friendly end- user graphical interface
- Interconnects with FEE-DAQ
- Provides a finite state machine for detector status
- Prevents critical situations and issues alarms
- Provides database for archiving
- Input Output Controller (IOC) needed everywhere, also in radiation environments

Radiation Problem: Single Event Effects

- Some SEE's, like SEU's don't cause permanent damage in electrical equipment, TID seems to be bigger issue
- Cross section (SEU/SEE sensitive area) appears to be small
 - Even if the MCU is directly inside a particle beam (Details shown later on), SEU incidence is not constantly high
 - There are plenty of examples of ordinary equipment running control software in high energy physics facilities around the world without apparent anomalies in function

Severity of errors

- Multiple bits can be flipped depending on:
 - the transistor technology,
 - Linear Energy Transfer (LET)
- CPU unpredictable behavior and Corrupted data
- Logic is affected by Single Event Transients (SET)
- Memory is affected by Single Event Effects
- Unrecoverable data loss
- Erroneous values transmitted to critical actuators can have catastrophic consequences



MCU Architectures

- SEE's are problematic enough that can result in serious malfunction
- An additional problem is the anecdotal perception of low malfunction incidence
- Approach: ARM produces intellectual property processors that fit very specific needs
 - Find one that focuses in safety and redundancy: arm7v4 **Cortex R5F**
 - Find the vendor that bought the rights to produce such a chip for sales: **TI- TMS570**
 - Build a control board based on that chip: **FTLMC**

Cont. MCU Architectures

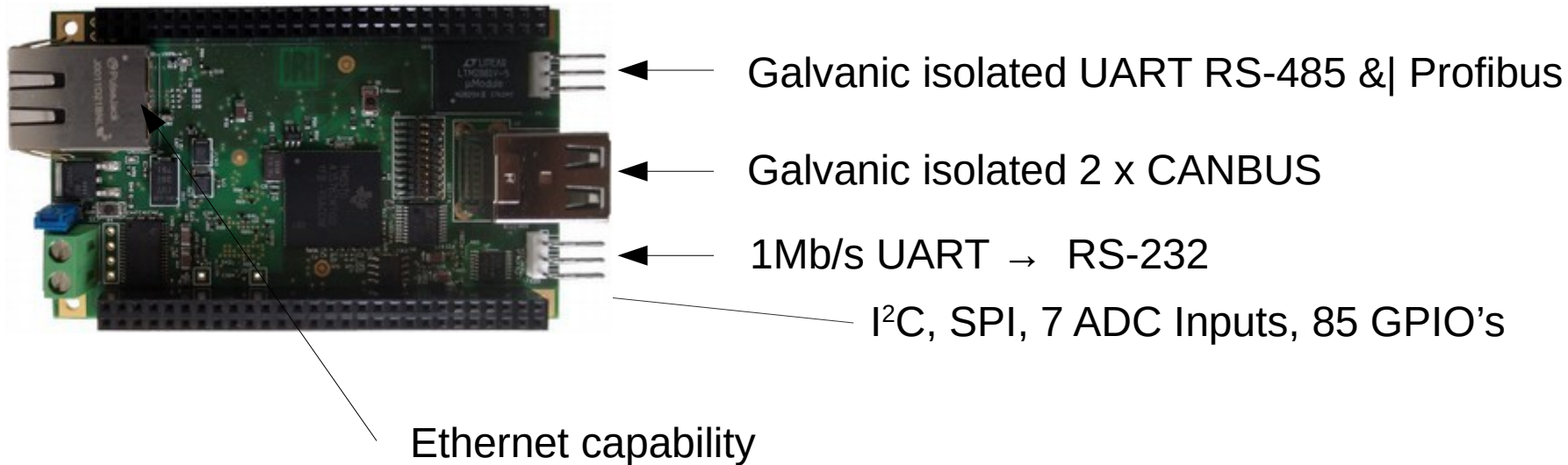
- Such a commercial device is not radiation hard specified
- But has ECC check when reading and writing to any memory inside MCU which allows us to implement a scrubbing daemon
- Runs same instruction in two different CPU's and compares the result to prevent Single Event Transients

Beam test of the Cortex-R (TI-TMS570 Eval Board)

- Exposed MCU directly to beam during: 13 hours
- Beam: 2Gev Protons
- Total detected and corrected SEU's:
 - in Bank A: 718
 - In Bank B: 686
- No multiple bit errors, (no unrecoverable errors)
- Failure registers continuously monitored
- Database with error time-stamp
- No errors during beam off times detected

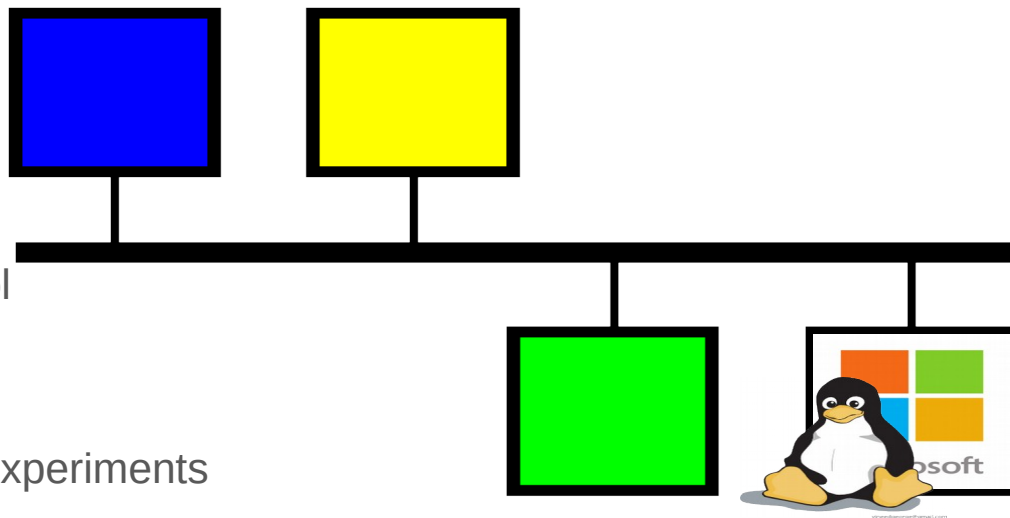


FTLMC Prototype, 53 x 89 mm



EPICS SCADA

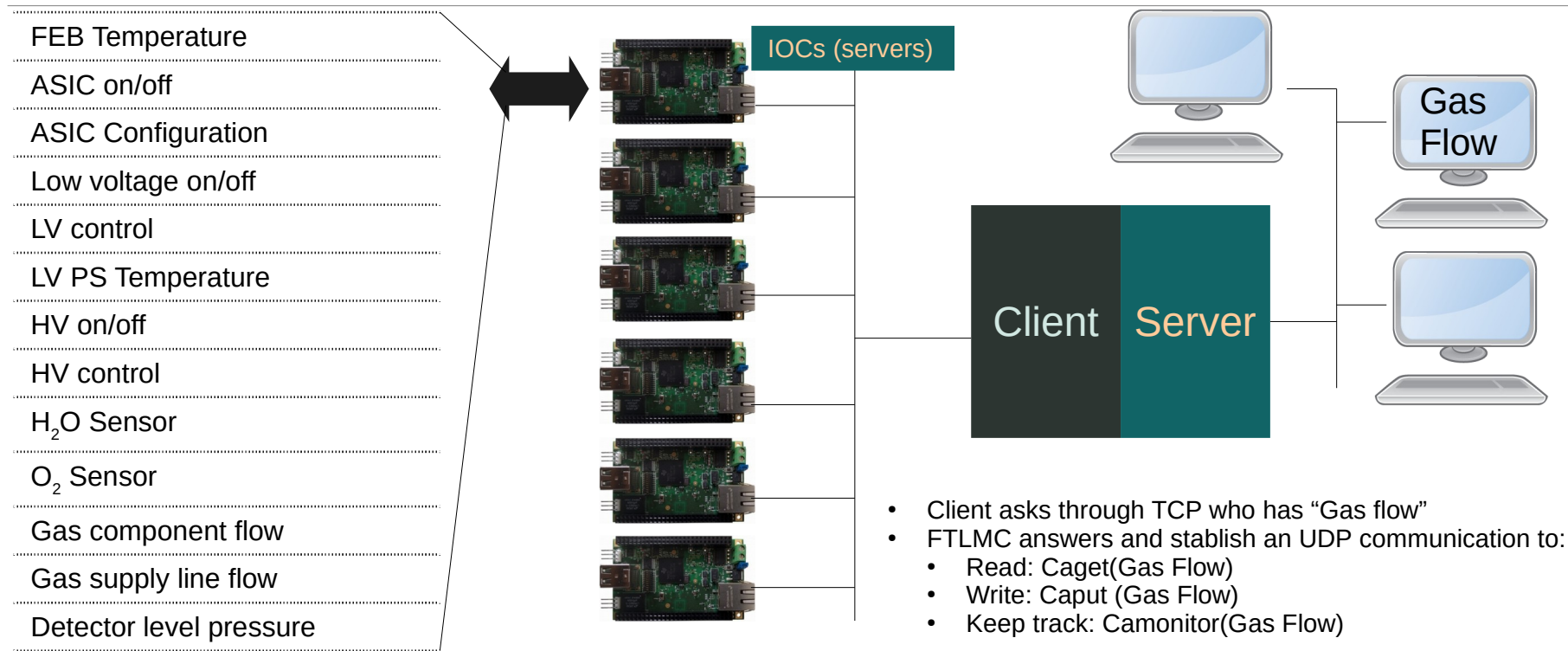
- Up-Scalable
- Open Source
- Supports many platforms
- Support for ethernet protocol
 - Python
 - Java, etc
- Large trajectory in physics experiments
- Multiple motif graphical interface options
- Version compatibility with board is still in progress, RTEMS 5 Compatibility needed



EPICS in DCS

- EPICS is considered for the CBM experiment:
 - (IOC) Input Output Controller → FTLMC
 - (CA) Channel Access TCP/UDP based protocol
 - (PV) Process Variables are any kind of value
 - Databases describe what variables are controlled by which IOC, how often are they probed and how are they interpreted

Channel Access



EPICS Database Records

Records Database

Parameters in an IOC
Gas Flow 1
Gas Flow 2
Low Voltage
ThermRawData
Magnet Temperature

Record's PV and their fields

LowVoltage
DTYP = Digital Input
SCAN = 1 Second
EGU = Volt

ThermRawData
DTYP = Analog Input
SCAN = Passive
EGU = RAW from ADC
VAL = 0x----

Each Record has its own driver
Where details such as GPIO
Control signals for Interfaces
are managed

MagnetTemperature
DTYP = Calc
SCAN = 1 Second
EGU = °C (degC)
INPA = ThermRawData
CALC = 5*A^2+3*A+1

- Each IOC contains a database of all records and their PV's that are under their tasks

RTEMS OS

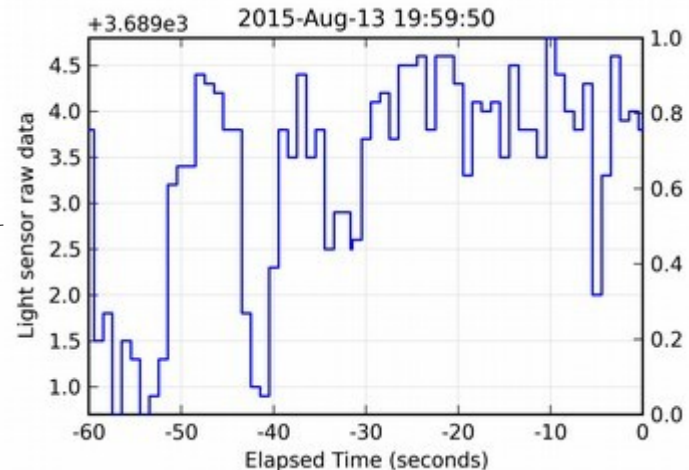
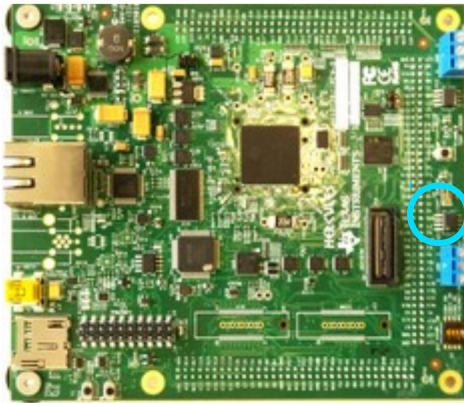
- Real Time capability
- Supports open standard application programming interfaces such as Posix
- Large community of developers and users
- Straight forward compiling toolchain
- Open source, own code and drivers can be integrated easily
- Memory scrubbing task daemon easily implemented as low priority task

RTEMS: The Real Time issue in control

- The task scheduling method defines if an operative system is real time or not
- Non real time OS normally assign a priority based on which was scheduled first or which has the less executing time
- Real time OS schedule tasks based on the deadline: earliest deadline means higher priority
- Preemption is important for optimal performance
- It is important when maintaining or updating values with critical timing constrains

Software Status

- EPICS supports RTEMS ≤ 4.10
- TMS570 Support was introduced in RTEMS until 4.11
- Own modifications in EPICS code allowed to make an RTEMS / EPICS / TMS570 demonstration in 2015 with a light sensor



Software Status

- Preliminary demonstration with EPICS 3.16.1 and RTEMS 4.11 is around the corner
- Final software version will be available when EPICS upgrades support for RTEMS 5

Summary



Single Event Effects can cause severe malfunction

Micro processor industry is very diverse and has safety features implemented in some micro- processors



Investing in a high radiation tolerant device is too costly but the ECC/Redundancy approach can provide low cost additional fault tolerance aspects



Board based on a commercial redundant architecture device was built. Scrubbing works and RTEMS based EPICS is being ported